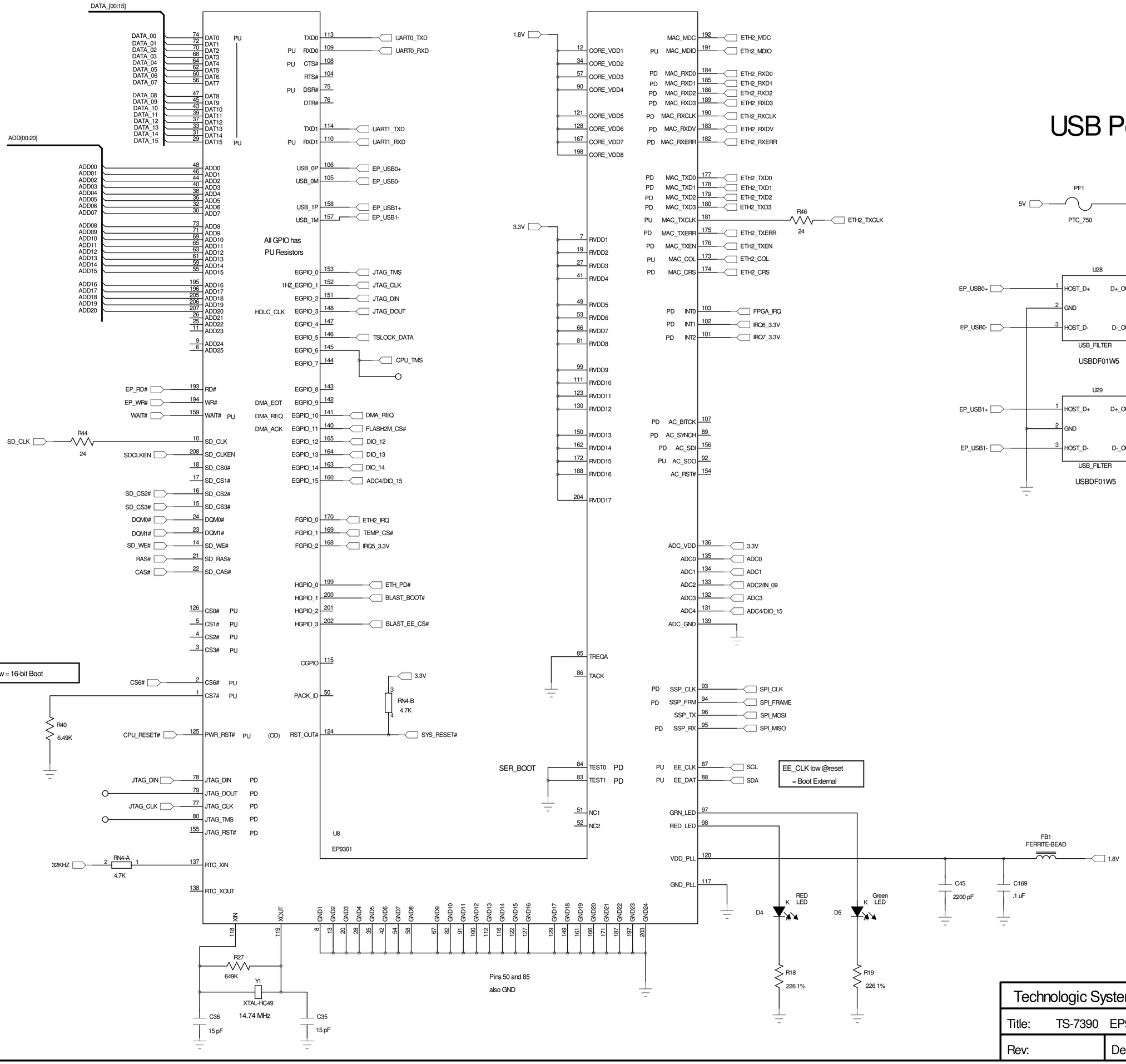
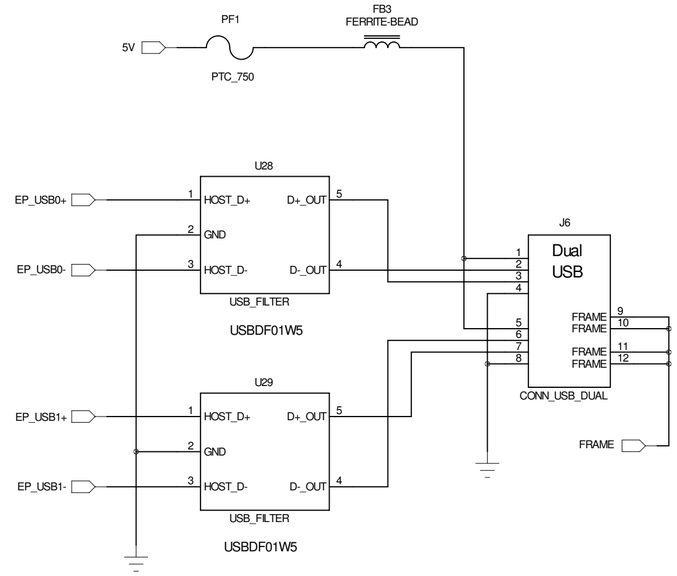
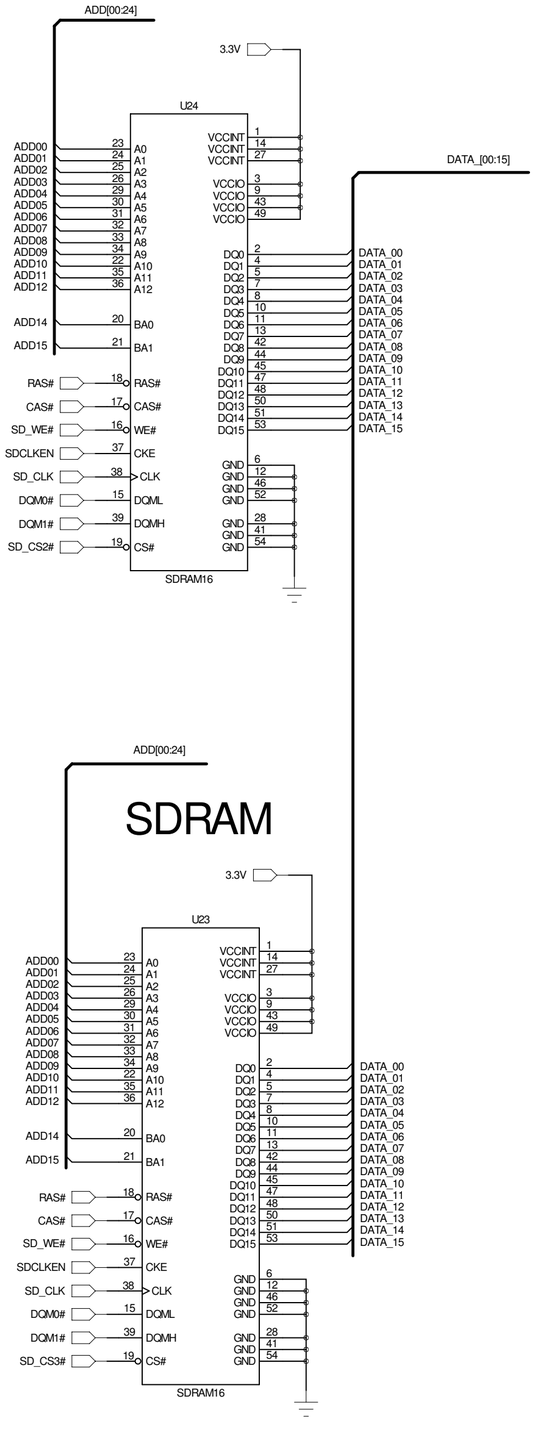


USB Ports

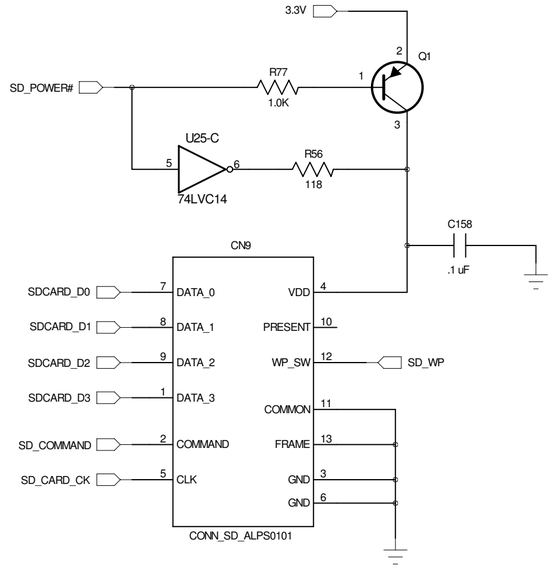


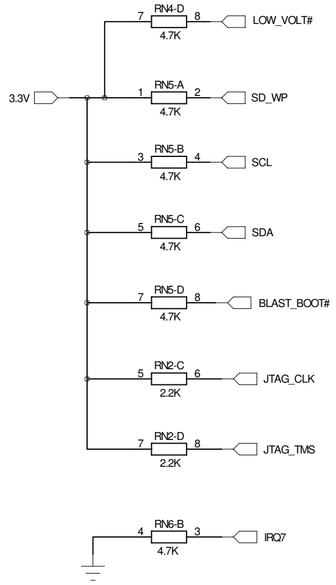
Technologic Systems	Date Oct. 7, 2008	
Title: TS-7390 EP9302 CPU, USB		
Rev:	Designer RLM	Sheet 1 of 8

SDRAM



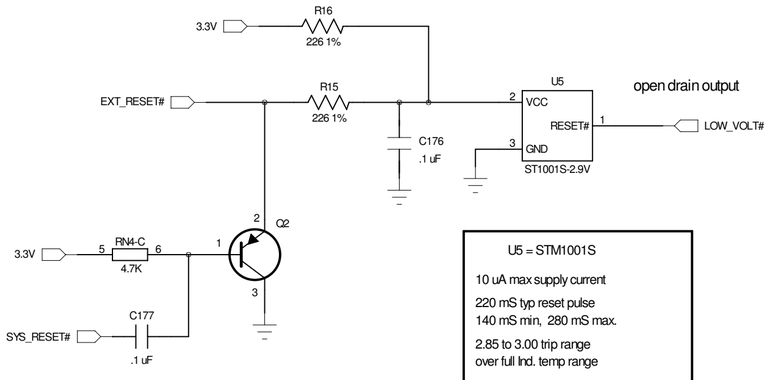
SD Card Socket





Temp Sensor

Power On Reset



U5 = STM1001S

10 uA max supply current

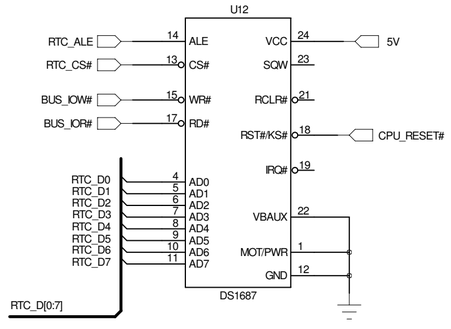
220 mS typ reset pulse
140 mS min, 280 mS max.

2.85 to 3.00 trip range
over full Ind. temp range

guaranteed output low
down to 1V Vcc

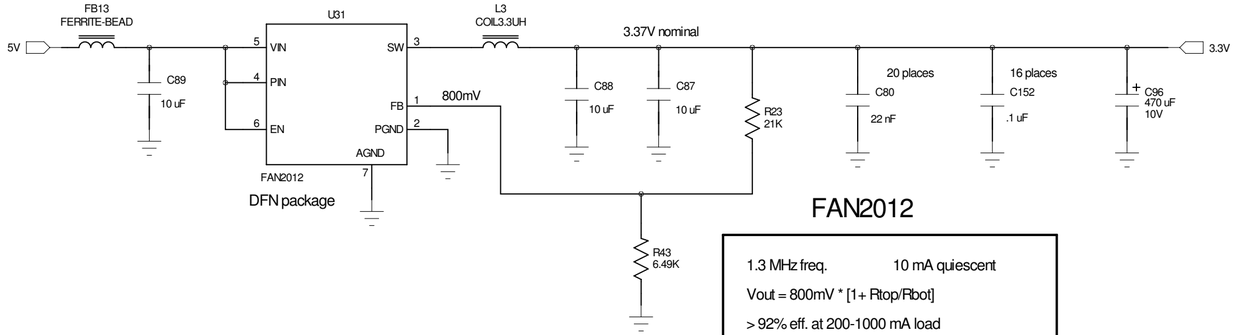
but can only sink 1.2 mA

Battery-Backed Real Time Clock



Technologic Systems		Date Oct. 7, 2008
Title: TS-7390 SDRAM, Flash, RTC, POR		
Rev:	Designer RLM	Sheet 2 of 8

3.3V Switching Regulator



FAN2012

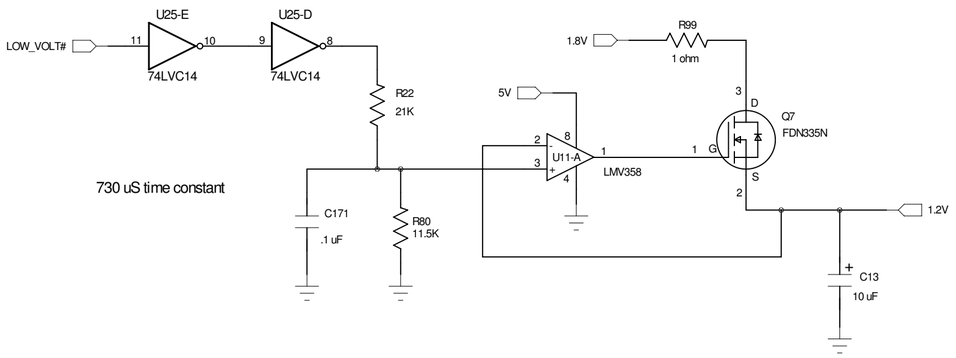
1.3 MHz freq. 10 mA quiescent

Vout = 800mV * [1+ Rtop/Rbot]

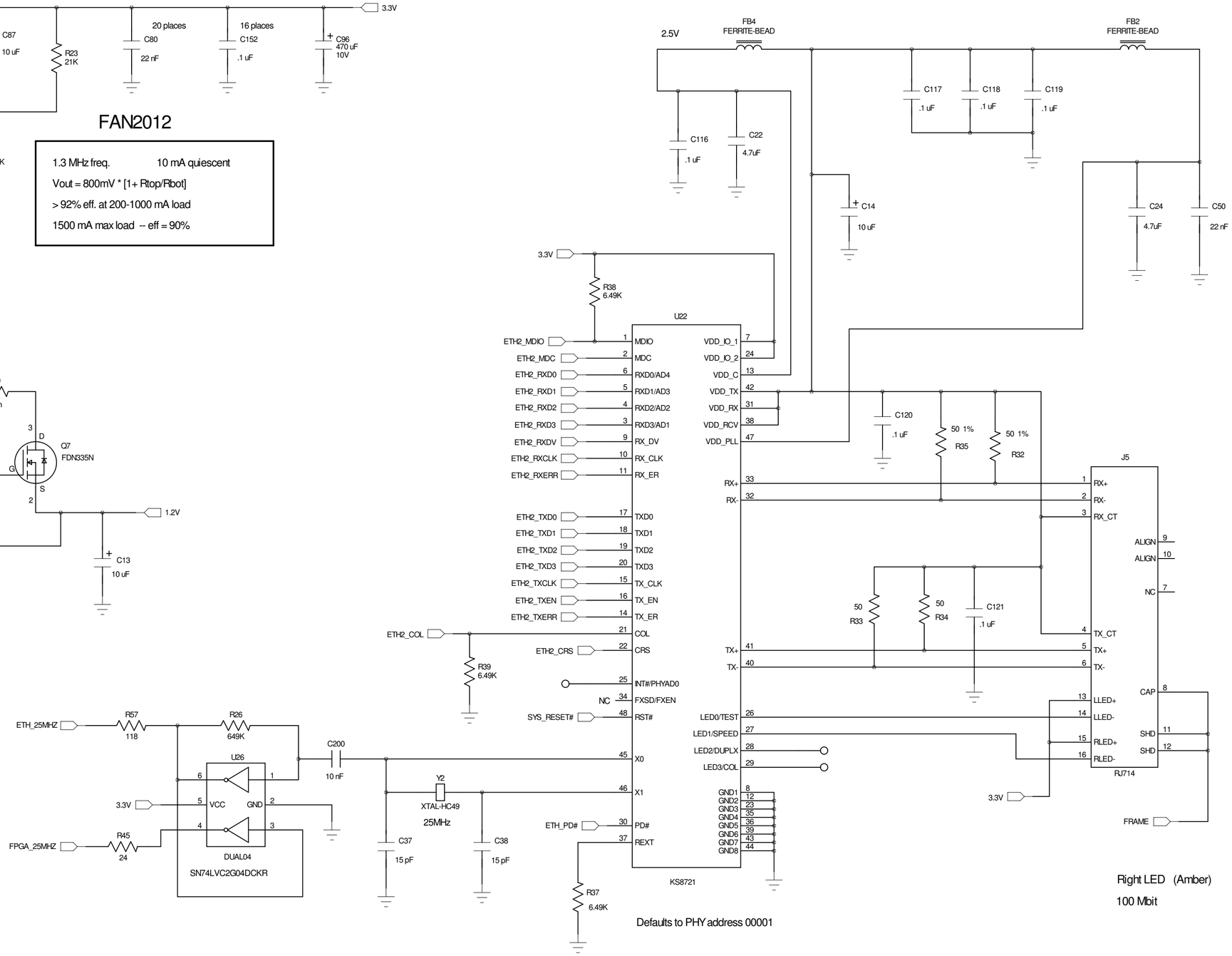
> 92% eff. at 200-1000 mA load

1500 mA max load -- eff = 90%

1.2V Regulator



10/100 Ethernet



Defaults to PHY address 00001

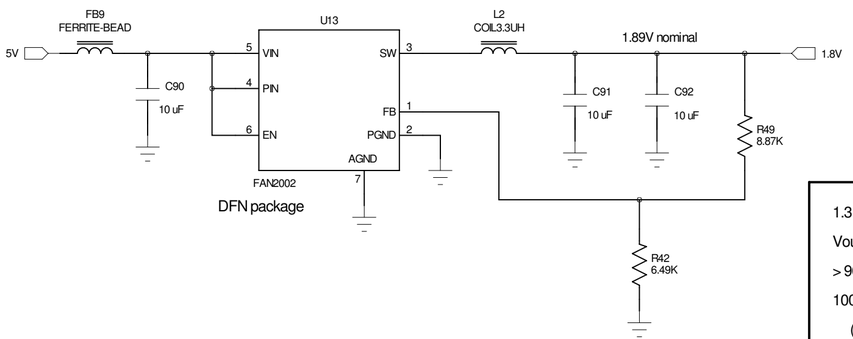
Right LED (Amber)

100 Mbit

Left LED (Green)

Link / Activity

1.8V Switching Regulator



FAN2002

1.3 MHz freq. 50 uA quiescent

Vout = 800mV * [1+ Rtop/Rbot]

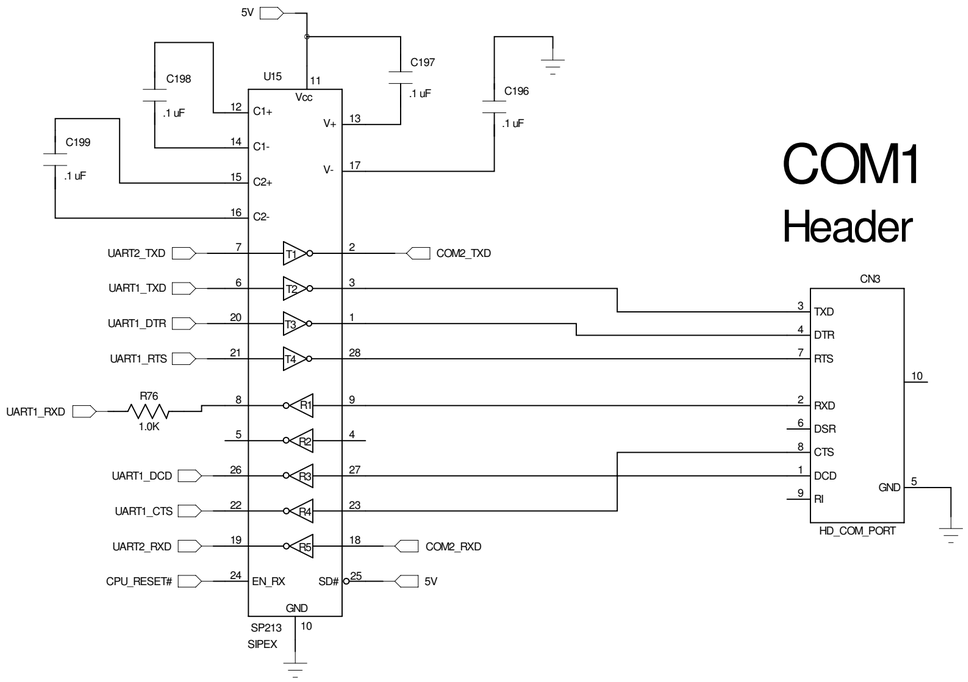
> 90% eff. at 100-400 mA load

1000 mA max load; eff. = 80%

(at 5V --> 1.8V)

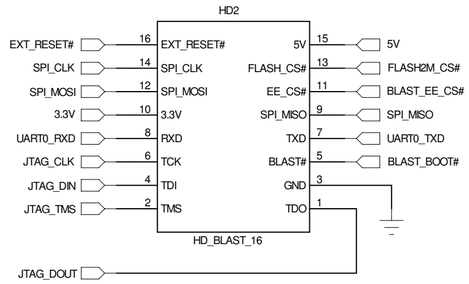
Technologic Systems		Date Oct. 7, 2008
Title: TS-7390 Power Supplies, Ethernet		
Rev:	Designer RLM	Sheet 3 of 8

RS-232 Transceiver



COM1 Header

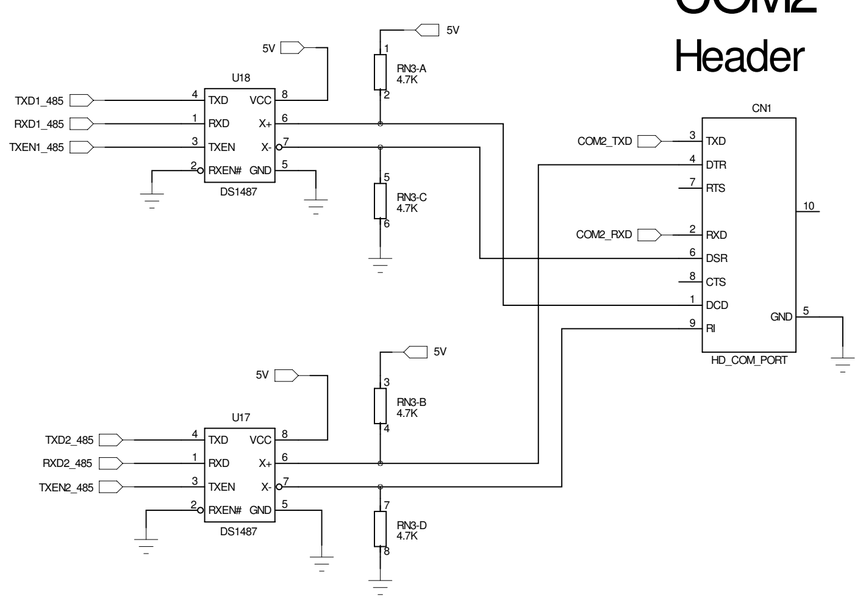
JTAG Header



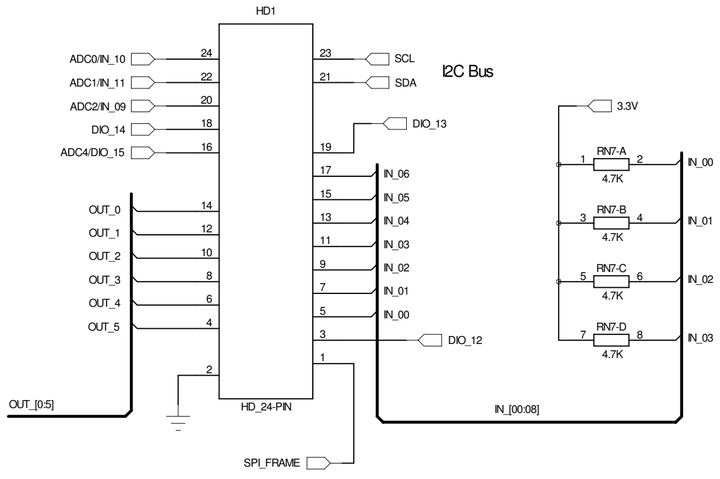
BLAST_EE_CS# is not used
for booting -- FPGA Boot
code has capability to boot
from 2MB Serial Flash directly

Logic "0" on "BLAST_BOOT#"
signal indicates Boot
using TS-9444 2MB Flash

RS-485 Drivers



COM2 Header



24-pin Header

24 + 16 = 40-pin Header

4 ADC
ADC lines in parallel with
IN_09, IN_10, IN11, DIO15

2 I2C

1 GND

6 Latched Outputs (OUT0-OUT5)

7 Buffered Inputs (IN0-IN6)

3 DIO_12, DIO_13, DIO_14

1 SPI_FRAME

Technologic Systems		Date Oct. 7, 2008
Title: TS-7390 COM Ports DIO JTAG Headers		
Rev:	Designer	Sheet 4 of 8

Lattice XP2 FPGA

8 MB Video SDRAM

XP2-5 has:
5K LUTS 2 PLLs
9 blocks of 1Kx18 Block RAM
12 18x18 Multipliers
146 I/O with 208 pin package
"instant ON" = about 1.5 mS
input PLL clock = 10 MHz min

Make sure these signals are on CLK inputs:
SDRAM_CLK
FPGA_25MHz

PROGRAM#, DONE, and INIT# are dedicated configuration pins when CFG0 is low. When CFG0 is high they are "general purpose I/O"
Page 4 of TN1141

During JTAG Flash programming the PROGRAM# pin should be high else it can inhibit Flash --> SRAM

DONE likewise must be high
These do have weak PU resistors

Pins 28 and 29 must be pulled up ! 3.3V suggested

When CFG0 = 1 then always uses SDM
SDM = Self Download Mode
SDM uses on-chip Flash --> SRAM
CFG0 PU resistor uses VCC core (1.2V)

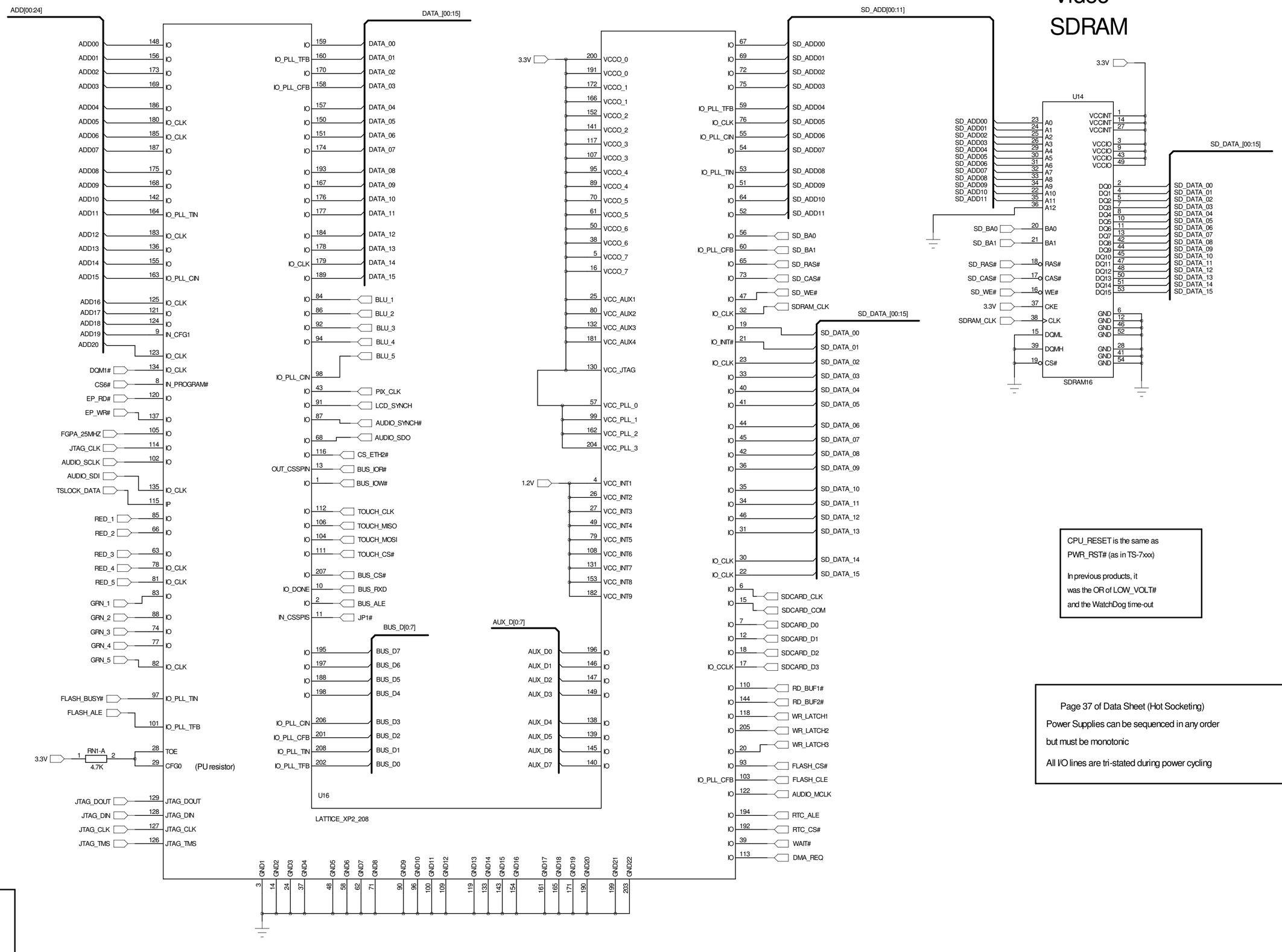
TAG Memory is 79 bytes of Flash (XP2-5)
Always available thru JTAG port
can not be Write or Read protected
perfect for: MAC, birth date, Revision #
TAG memory can be accessed from fabric

Set CONFIG_MODE to NONE
This allows all pins to be used

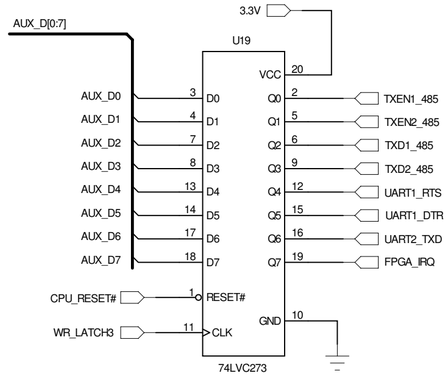
CPU_RESET is the same as PWR_RST# (as in TS-7xxx)
In previous products, it was the OR of LOW_VOLT# and the WatchDog time-out

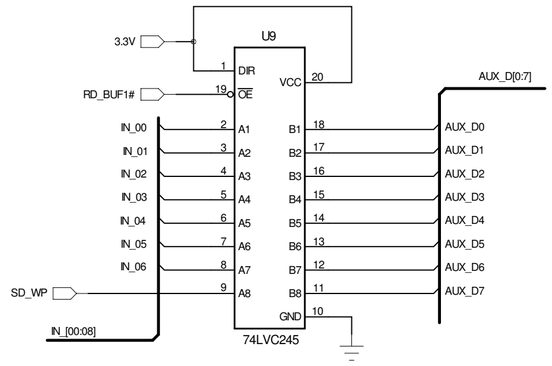
Page 37 of Data Sheet (Hot Socketing)
Power Supplies can be sequenced in any order but must be monotonic
All I/O lines are tri-stated during power cycling

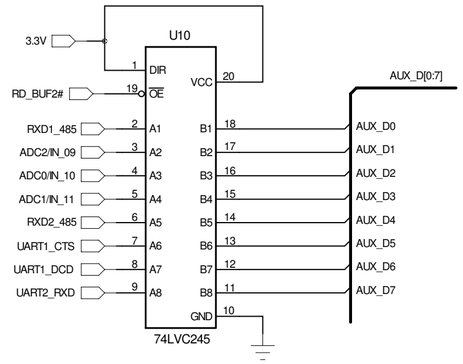
Pull-up and pull-down resistors are 6 to 30K ohms

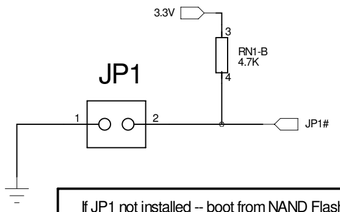


Technologic Systems		Date Oct. 7, 2008
Title: TS-7390 FPGA and Frame Buffer		
Rev:	Designer	Sheet 5 of 8



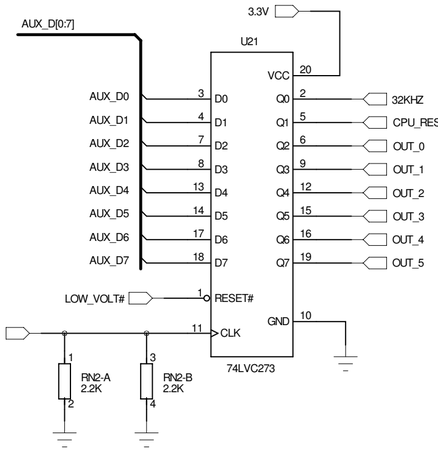


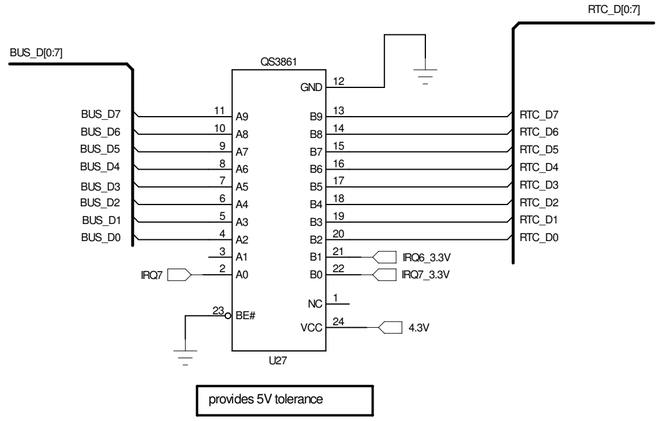




If JP1 not installed -- boot from NAND Flash

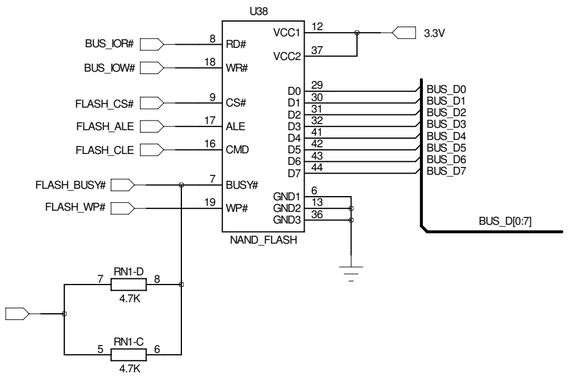
If JP1 is installed, attempt to boot from SD card
If SD card is not present then boot from NAND

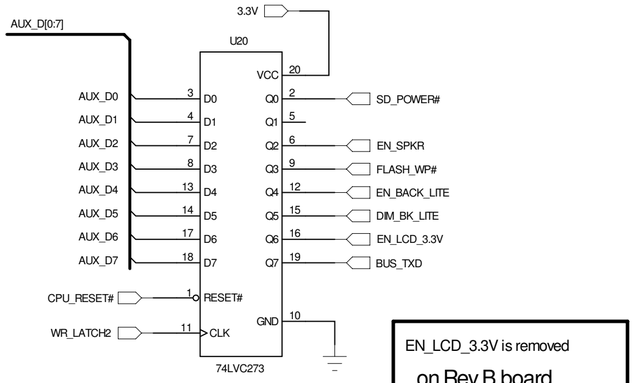




provides 5V tolerance

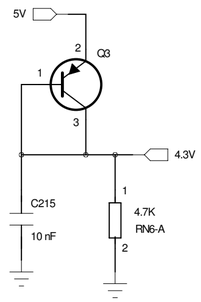
NAND Flash



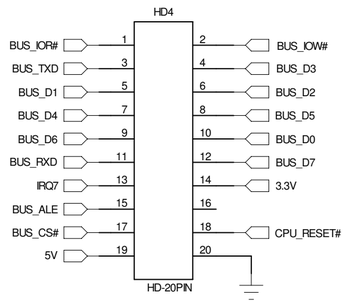


EN_LCD_3.3V is removed
on Rev B board

4.3V Power Supply



Expansion Bus



Technologic Systems		Date Oct. 7, 2008
Title: TS-7390 AUX Bus		
Rev:	Designer	Sheet 6 of 8

Hysteretic Switching Power Supply

5V @ (2.5 Amps)

5-28V
Power In

CN2
CONN_POWER_2P

BLM21PG221SN1D
FB6
FERRITE-BEAD
220 ohm @100MHz
50 milliohm DC

C174
.1 uF

5V_28V

D1
TVS-26V
1SMB26AT3G

FB7
FERRITE-BEAD

8x11.5 mm
493-1899-ND

C95
100 uF
50V
230 mohms

C99
2.2 uF
50V

C81 and R98
control soft start
and current limit

C81
22 nF

R98
76.8K

Q5
FDS9435

30V = VDS max
65/80 mohms @ Vgs = 4.5V
42/50 mohms @ Vgs = 10V

U7
LM3489
I_ADJ
VIN
EN
PGATE
I_SENSE
FB
PGND
GND

L1 = MSS1038-223
L1
22 uH

D2
2A, 50V

5.06V nominal

C94
1000 pF

R21
20K

R41
6.49K

C97
470 uF
10V
120 mohm
493-1743-ND
10 cents

FB8
FERRITE-BEAD

C175
.1 uF

5V

FB5 and FB7 removed
on Rev B board

Zener knee at 29-32V
for 1 mA of current
14 Amps @ 42V

2.2 uF @ 50V 10%
Murata GRM31CR71H225K
0.10 @ 2K Reel Digikey

1.8V

FB11
FERRITE-BEAD

C26
4.7 uF

C191
.1 uF

C190
.1 uF

C194
.1 uF

C25
4.7uF

C188
.1 uF

C187
.1 uF

C186
.1 uF

FB10
FERRITE-BEAD

3.3V

C192
.1 uF

C193
.1 uF

U77
AX88796B

3.3V

RN6-D
4.7K

R36
6.49K

CPU_RESET#

ETH2_IRQ

ETH2_CS#

BUS_IOR#

BUS_IOW#

ADD[00:05]
ADD05
ADD04
ADD03
ADD02
ADD01
ADD00

DATA[00:15]
DATA15
DATA14
DATA13
DATA12
DATA11
DATA10
DATA09
DATA08
DATA07
DATA06
DATA05
DATA04
DATA03
DATA02
DATA01
DATA00

ETH_25MHZ

V18F
EECS
EECK
EEDIO
RST#
PME
IRQ
AEN_PSEN
IOIS16#
CS#
RD#
WR#
SA5_FIFO_SEL
SA4
SA3
SA2
SA1
SA0
SD15
SD14
SD13
SD12
SD11
SD10
SD9
SD8
SD7
SD6
SD5
SD4
SD3
SD2
SD1
SD0
XTALOUT
XTALIN
VCCK
VCCK
VCCK
VCC18A
VCC18A
VCC3A3
VCC3IO
VCC3IO
VCC3R3
TPI+
TPI-
TPO+
TPO-
I_LK/ACT
I_SPEED
I_FULL/COL
RSET_BG
TCLK
TEST_CK_EN
GND3R3
TEST2
TEST1
GND3A3
GND18A
GND18A
GND
GND
GND

ETH2_LINK_ACT#
ETH2_SPEED#

R12
12.1K

R28 51
R29 51
R30 51
R31 51

C182
.1 uF

C183
.1 uF

C185
.1 uF

C184
.1 uF

J100
RJ714
RX+
RX-
RX_CT
TX_CT
TX+
TX-
LLED+
LLED-
RLED+
RLED-
ALIGN
ALIGN
NC
CAP
SHD
SHD

FRAME

Right LED (Amber)
100 Mbit

Left LED (Green)
Link / Activity

5V_28V

R25
649K

R97
76.8K

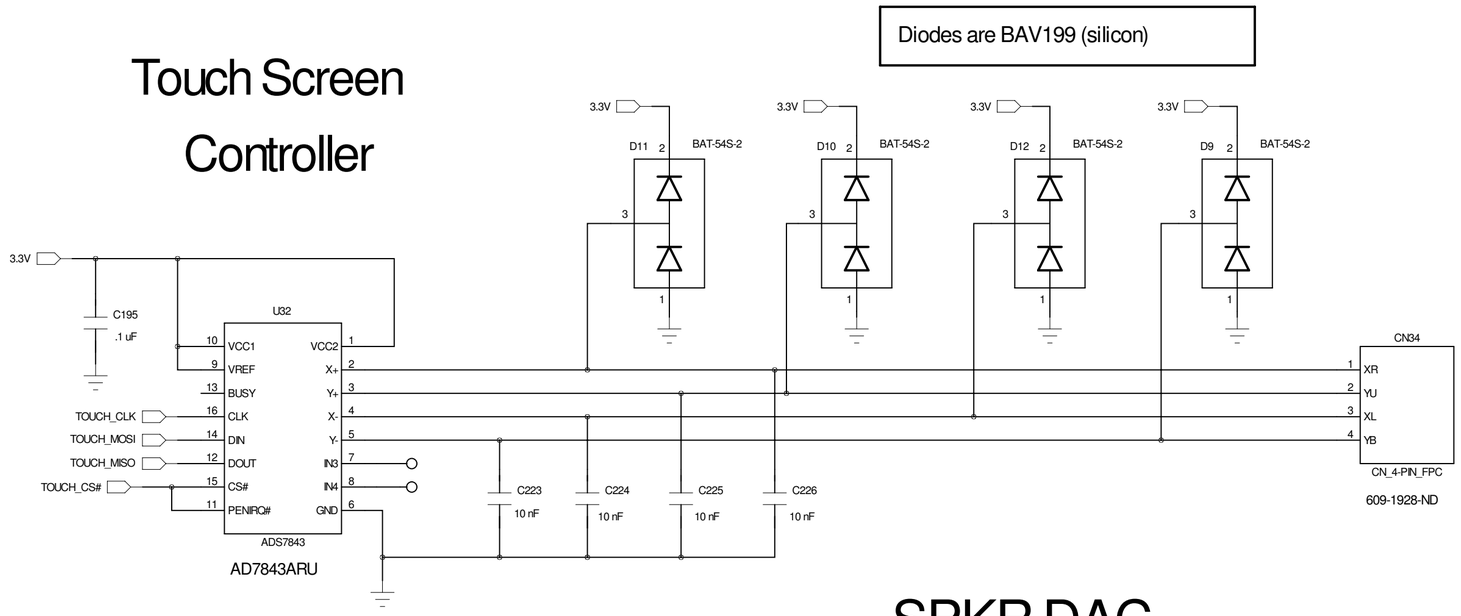
U11-B
LMV358

ADC3

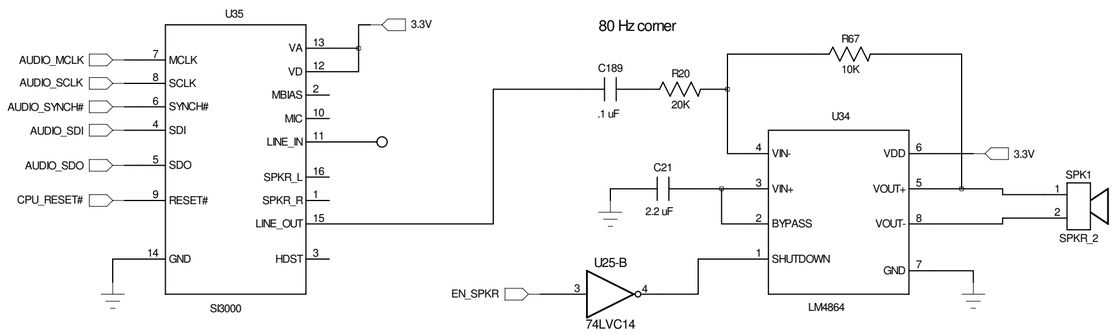
Technologic Systems	Date Oct. 7, 2008	
Title: TS-7390 5V Power Supply		
Rev:	Designer	Sheet 7 of 8

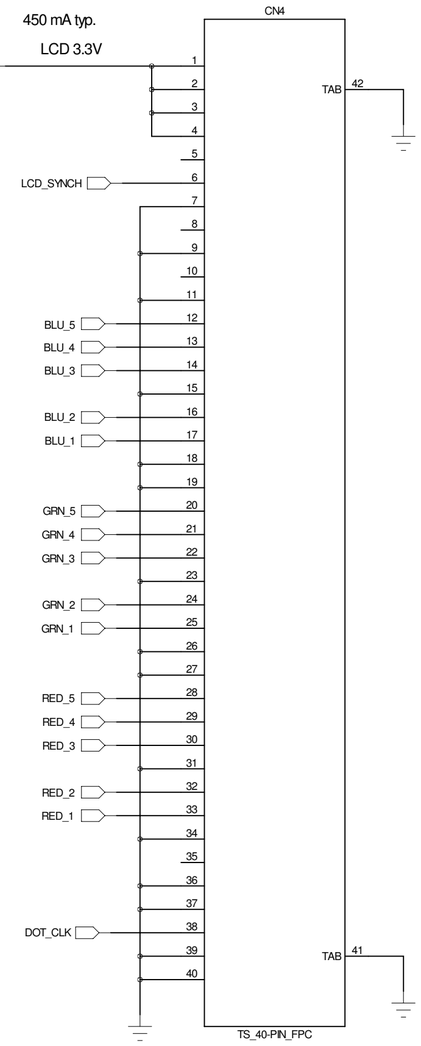
Touch Screen Controller

Diodes are BAV199 (silicon)

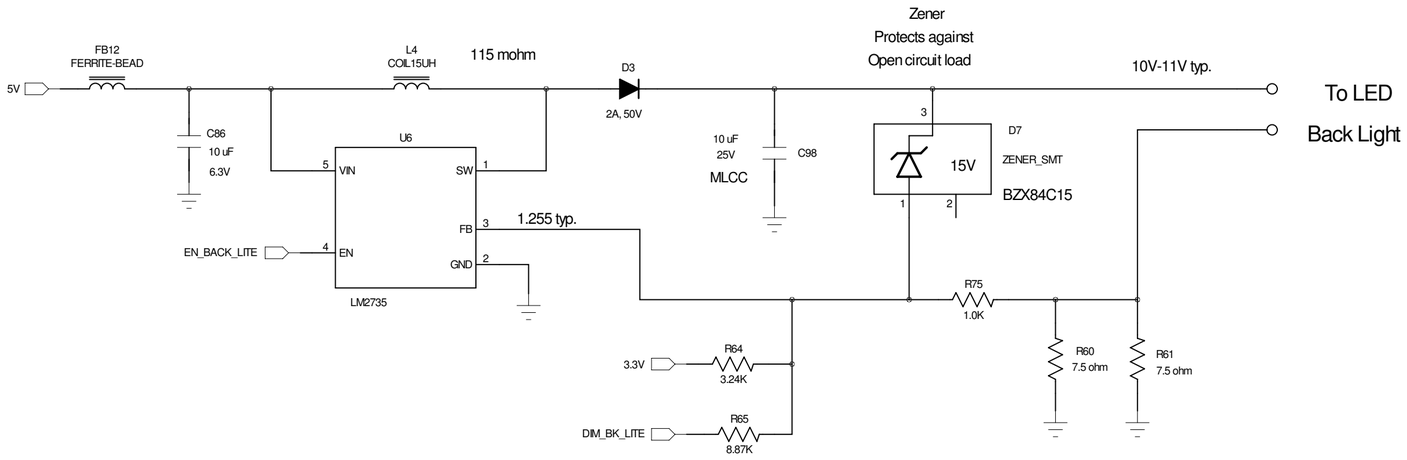


SPKR DAC





BackLight Power



87% typ. eff. at 200 mA load
(12V out) per data sheet

744 mV is high setting (198 mA)
333 mV is low setting (88 mA)

200 mA is maximum continuous
that LED BackLight is rated at.

Technologic Systems	Date Oct. 7, 2008	
Title: TS-7390 LCD, BackLight, Touch, SPKR		
Rev:	Designer	Sheet 8 of 8