TS-3Z-DIO

This board has 5 isolated islands

Two groups of 8 isolated Inputs 0-30V (16 total)

Two groups of 8 isolated Outputs 0-30V, 2A (16 total)

One group of 4 isolated Analog Inputs 0-32V

All groups are isolated from each other
and from the TS-7250-V2 SBC

BOM Issues

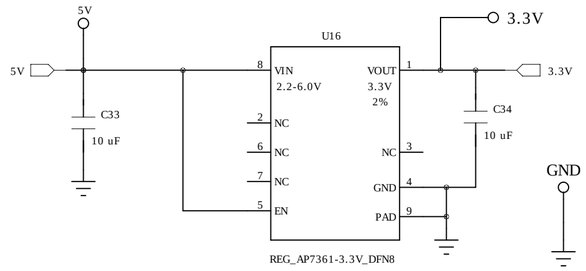
R70-R86 (60.4K) are not populated

These are PU on the Inputs 0-15

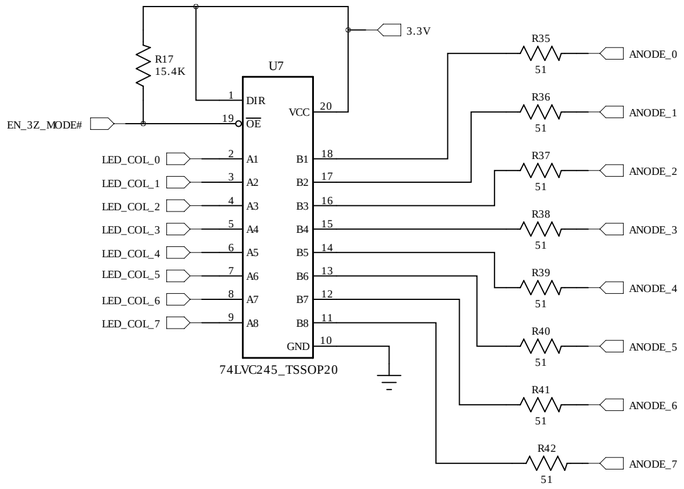
R43 and R44 not populated (only needed if using PU)

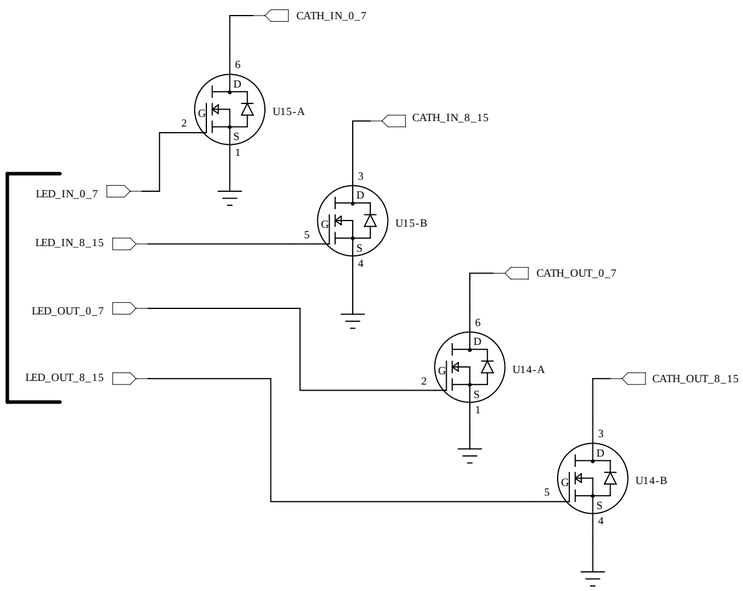
Technologic Systems	Date June 15, 2015	
Title: TS-3Z-DIO		
Rev: P1	Designer RLM	Sheet 1 of 13

Linear 3.3V Reg.



LED Drivers

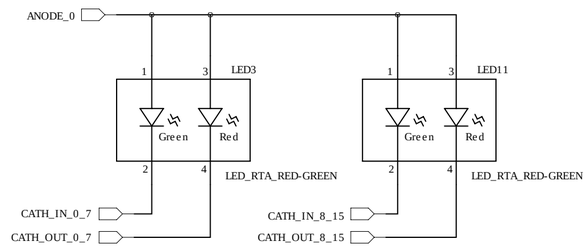


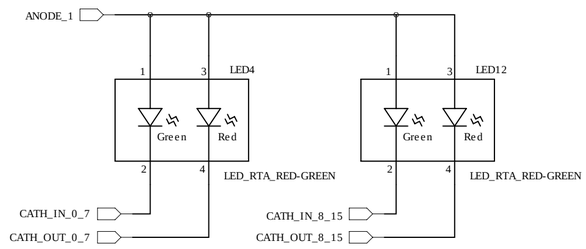


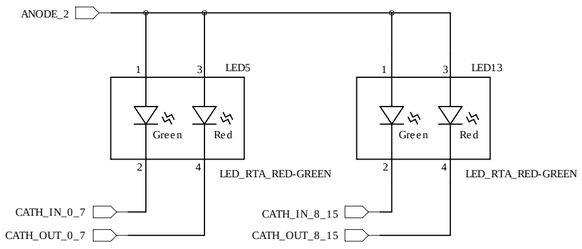
400 Hz

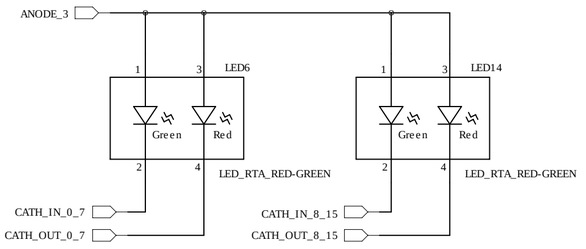
1 of 4 true

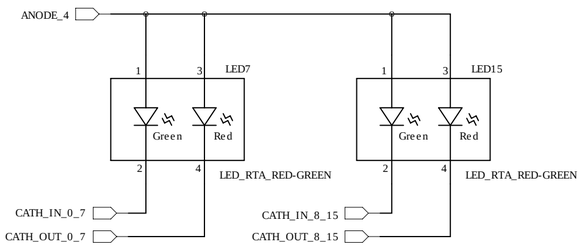
Red/Green LEDs

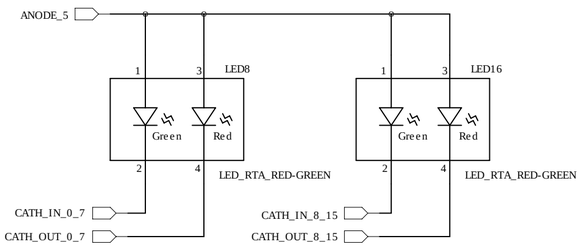


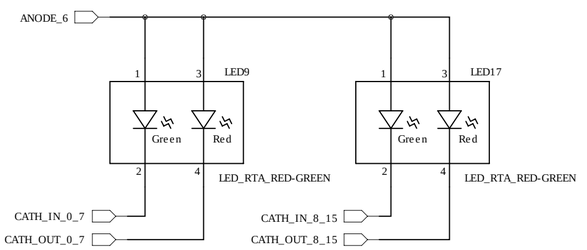


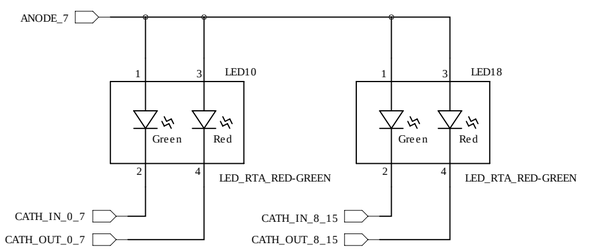










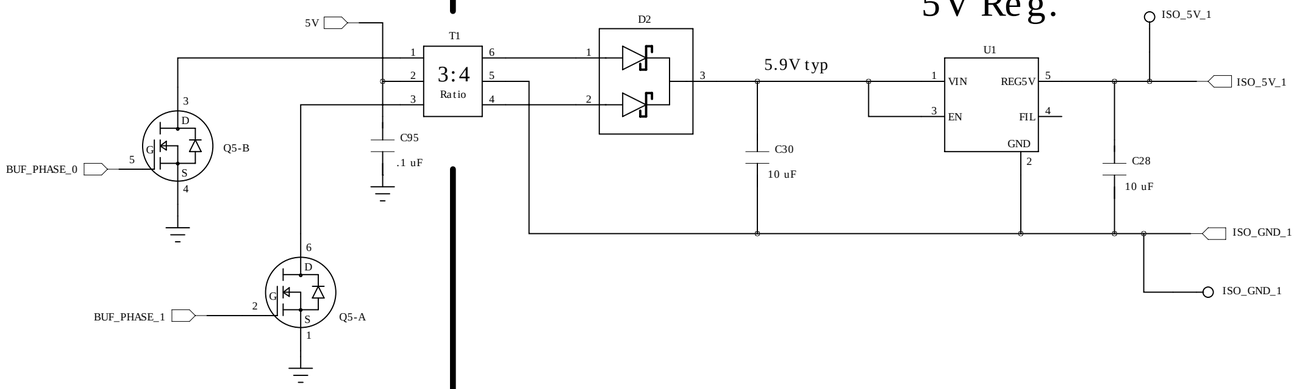


Technologic Systems		Date June 15, 2015
Title: TS-3Z-DIO LEDs		
Rev: P1	Designer RLM	Sheet 2 of 13

Isolated Power

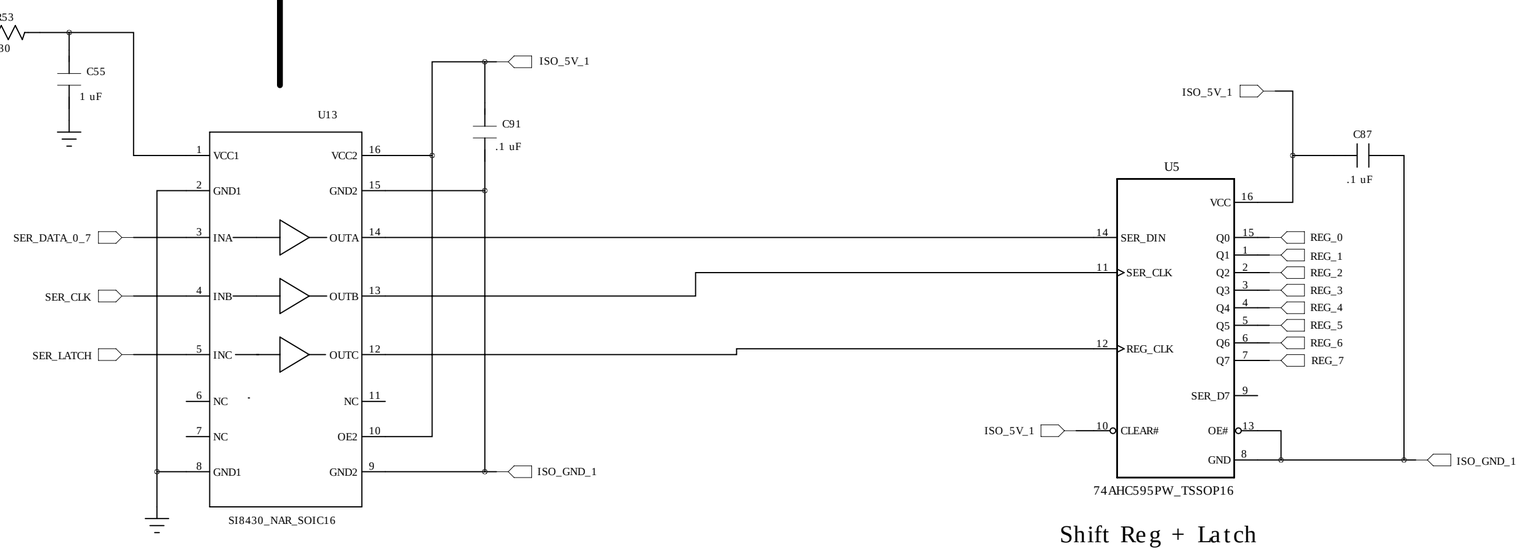
Phase_0# and Phase_1# must
be non-overlapping active high
51% low; 49% high duty cycle
and nominal 250 KHz
40 ns both off (low) at edges

5V Reg.



8 bit Shift Reg.

Outputs 0-7



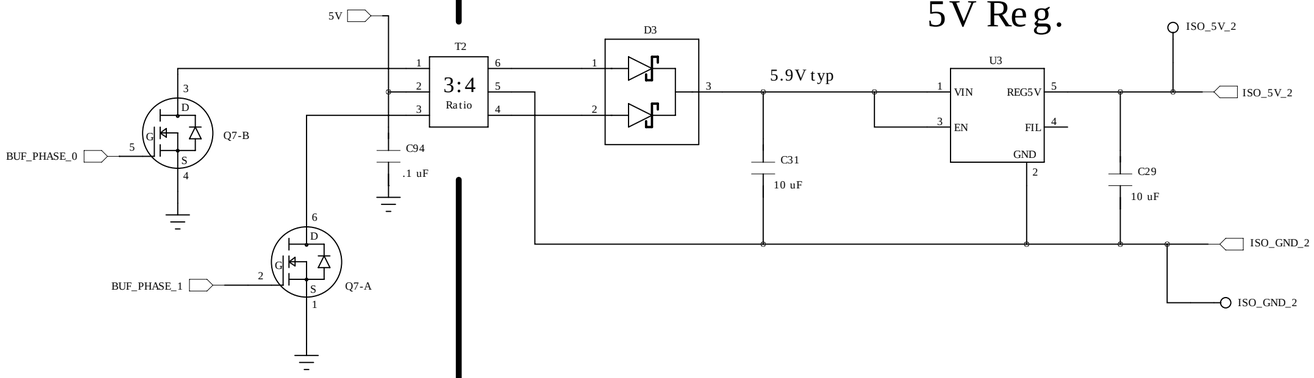
Shift Reg + Latch

Technologic Systems	Date June 15, 2015	
Title: TS-3Z-DIO Isolated Outputs 0-7		
Rev: P1	Designer	Sheet 3 of 13

Isolated Power

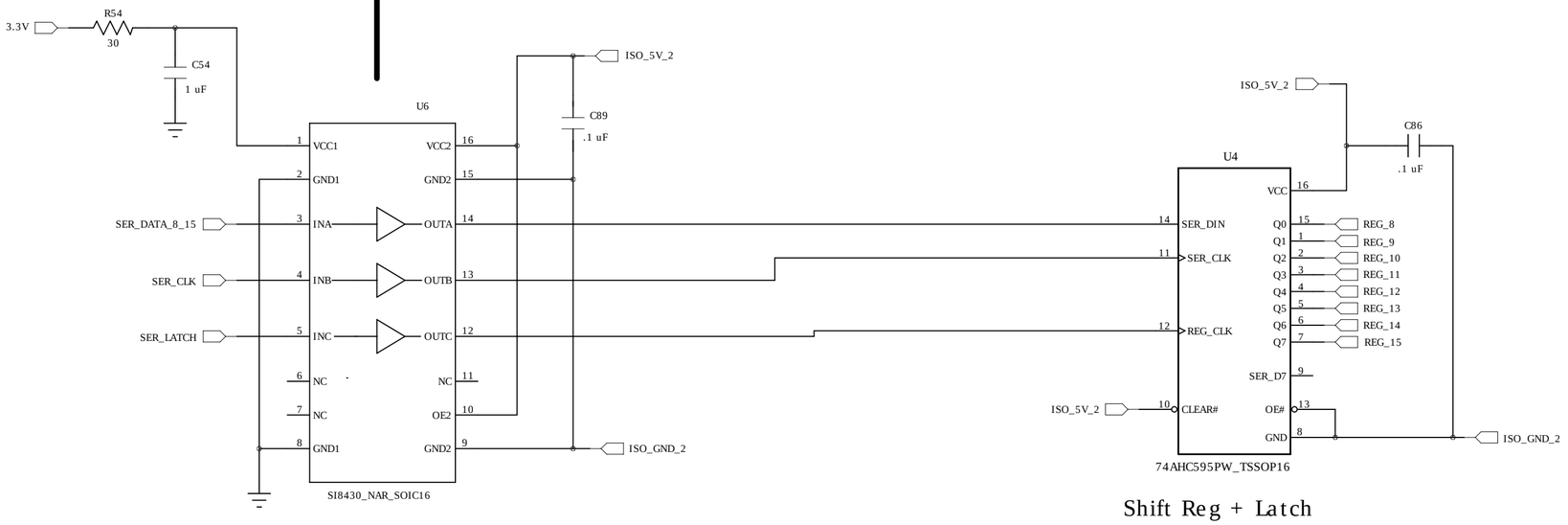
Phase_0# and Phase_1# must
be non-overlapping active high
51% low; 49% high duty cycle
and nominal 250 KHz
40 ns both off (low) at edges

5V Reg.



8 bit Shift Reg.

Outputs 8-15



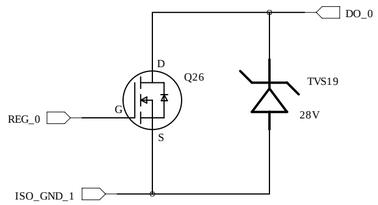
Shift Reg + Latch

Technologic Systems		Date June 15, 2015
Title: TS-3Z-DIO Isolated Outputs 8-15		
Rev: P1	Designer	Sheet 4 of 13

Dig. Outputs (30V Open Drain)

2A sink for each Output

0



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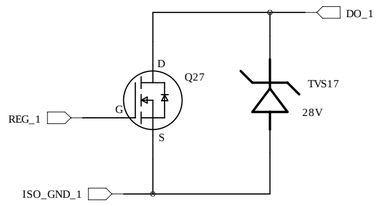

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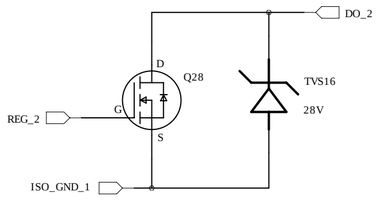

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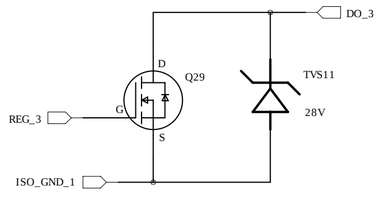

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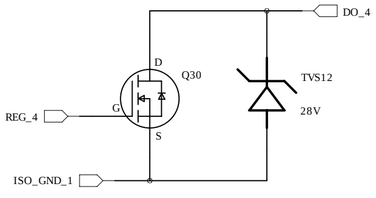

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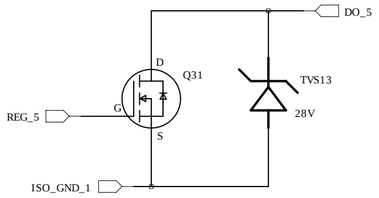

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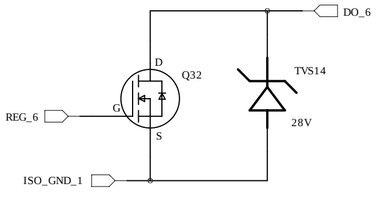

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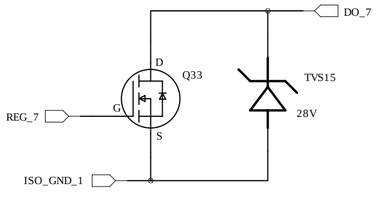
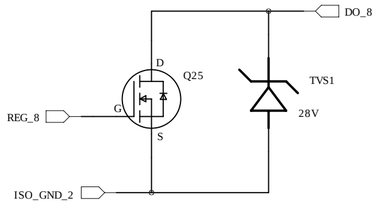


Technologic Systems	Date June 15, 2015	
Title: TS-3Z-DIO Isolated Outputs 0-7		
Rev: P1	Designer	Sheet 5 of 13

Dig. Outputs (30V Open Drain)

2A sink for each Output

#8



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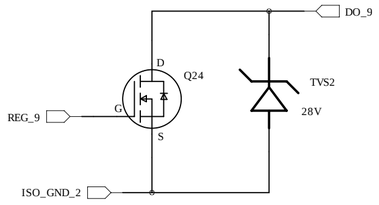

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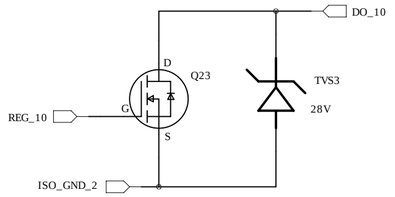

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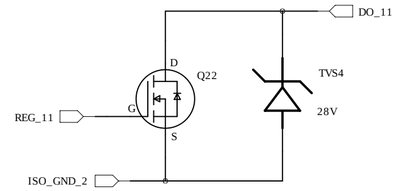

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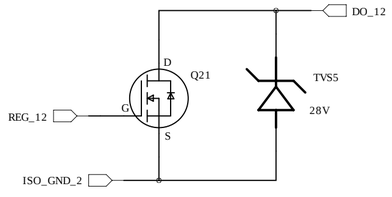

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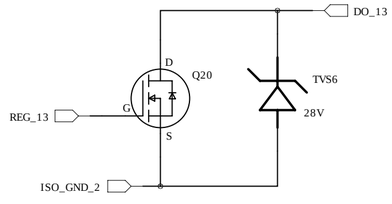

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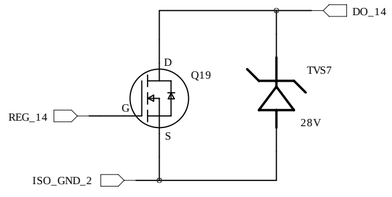

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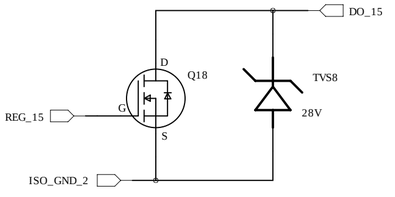
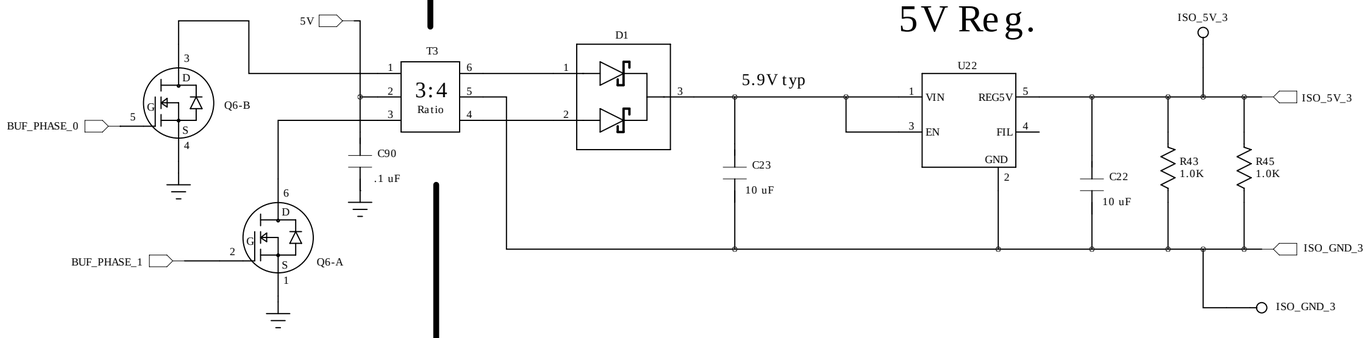


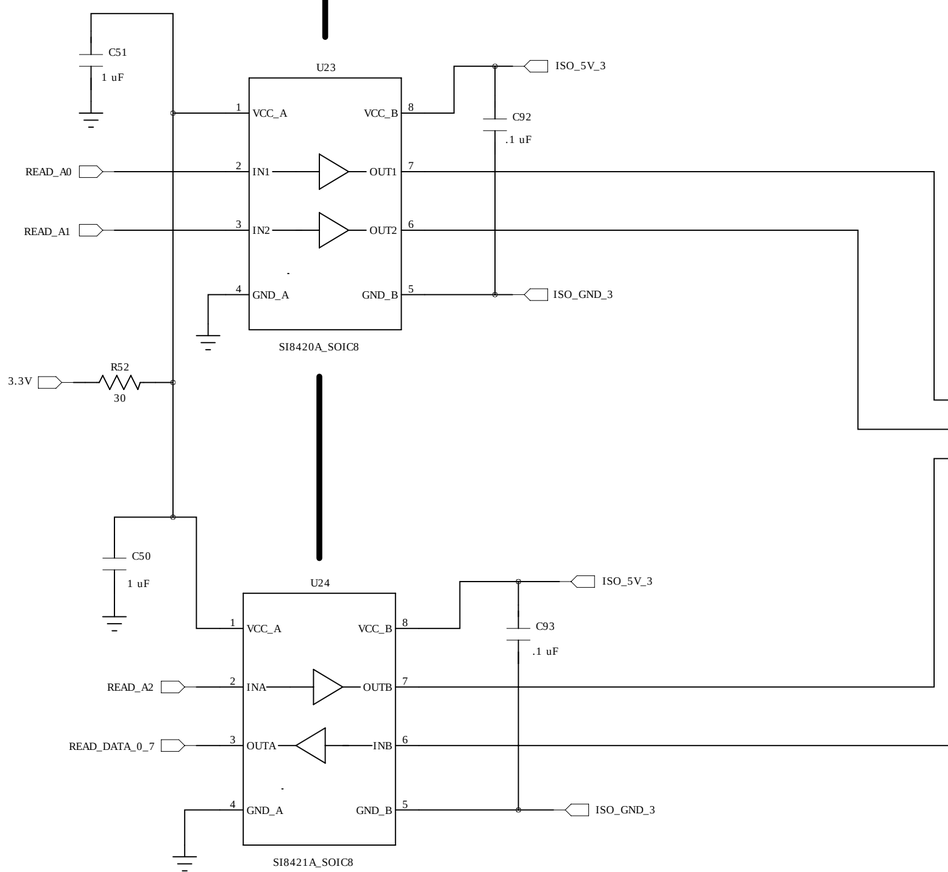
Technologic Systems		Date June 15, 2015
Title: TS-3Z-DIO Isolated Outputs 8-15		
Rev: P1	Designer RLM	Sheet 6 of 13

Isolated Power

Phase_0# and Phase_1# must
be non-overlapping active high
51% low; 49% high duty cycle
and nominal 250 KHz
40 ns both off (low) at edges

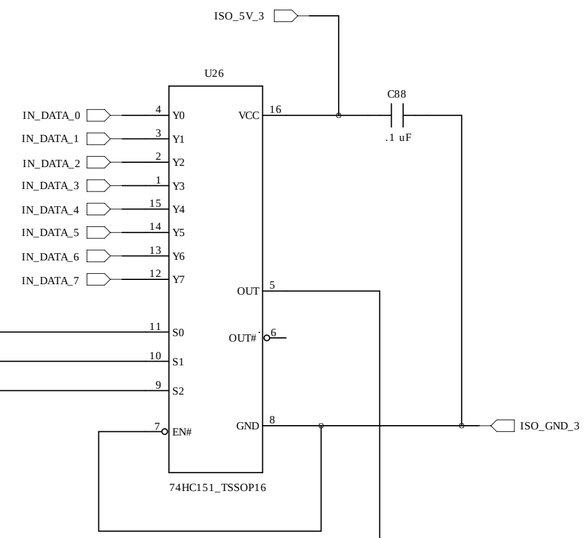
5V Reg.





Read MUX

Read Data 0-7



Technologic Systems	Date June 15, 2015	
Title: TS-3Z-DIO Isolated Inputs 0-7		
Rev: P1	Designer	Sheet 7 of 13

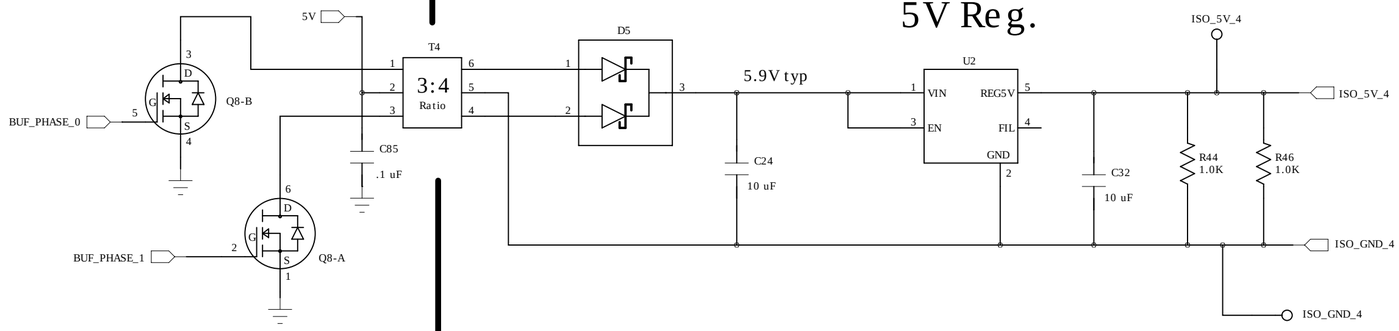
Isolated Power

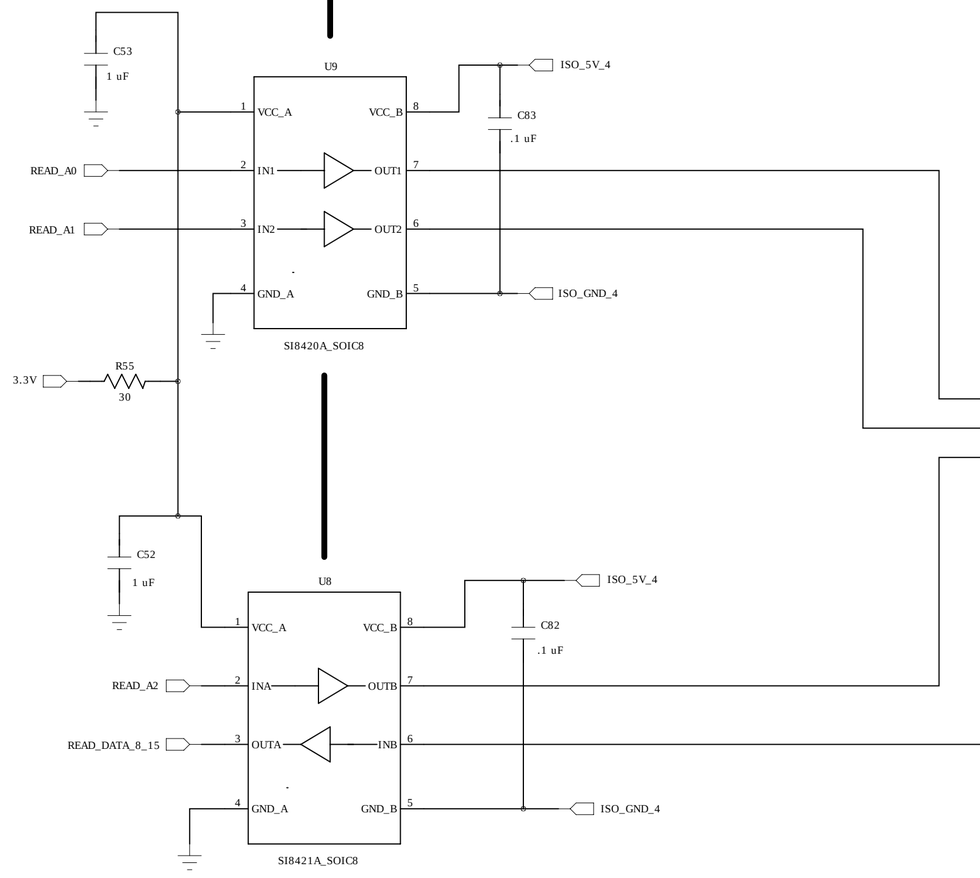
Read MUX

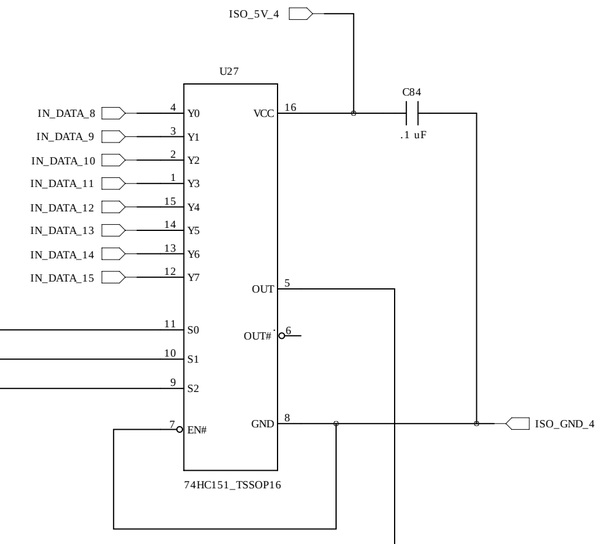
Read Data 8-15

Phase_0# and Phase_1# must
be non-overlapping active high
51% low; 49% high duty cycle
and nominal 250 KHz
40 ns both off (low) at edges

5V Reg.





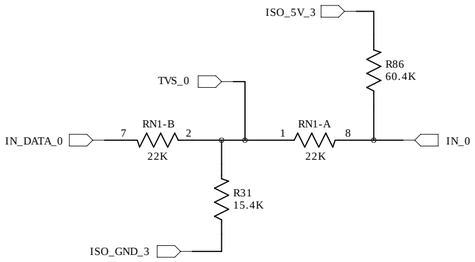


Technologic Systems	Date June 15, 2015	
Title: TS-3Z-DIO Isolated Inputs 8-15		
Rev: P1	Designer	Sheet 8 of 13

Dig. Inputs

0-30V range, 6V typ Threshold

0



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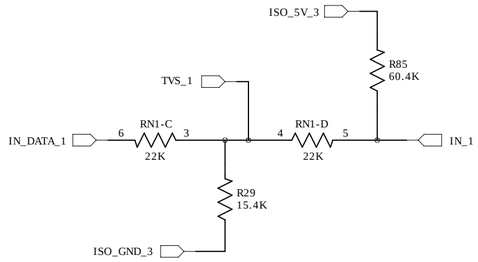

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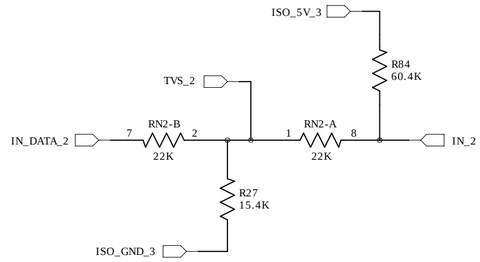

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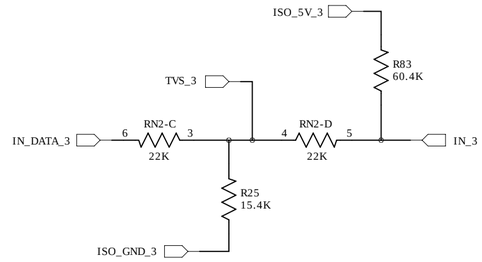

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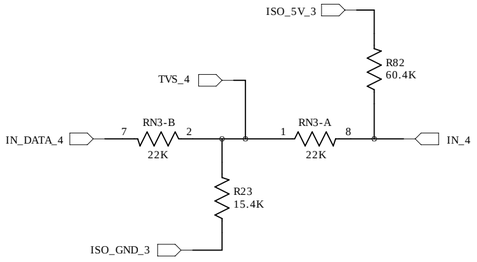

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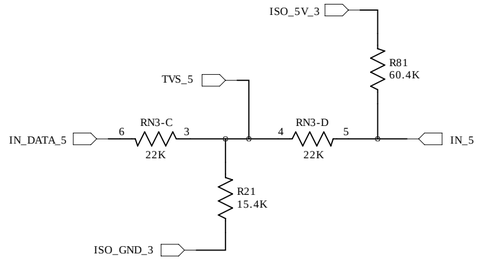

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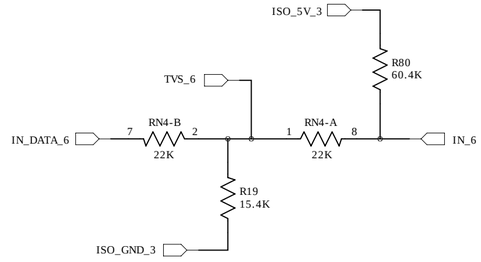

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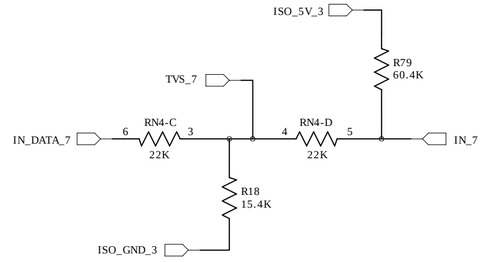
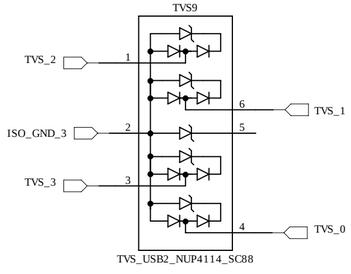
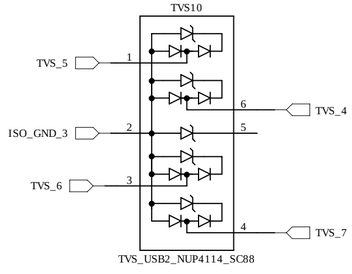




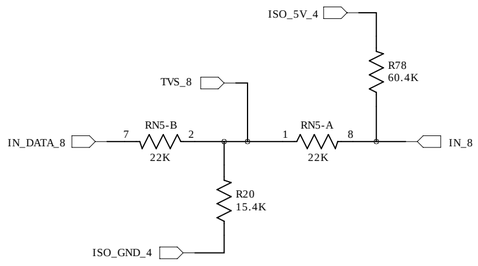


Technologic Systems	Date June 15, 2015	
Title: TS-3Z-DIO Isolated Inputs 0-7		
Rev: P1	Designer	Sheet 9 of 13

Dig. Inputs

0-30V range, 6V typ Threshold

#8



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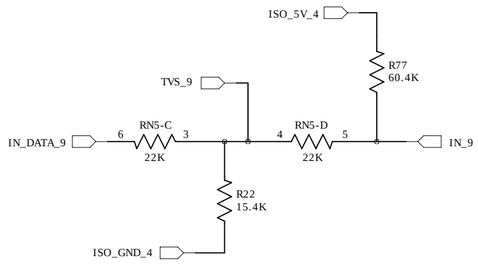

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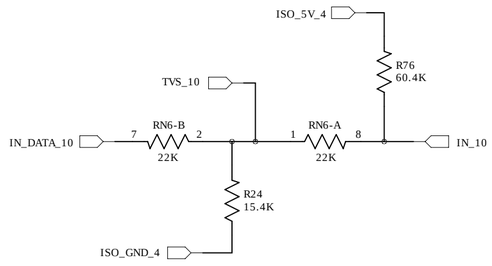

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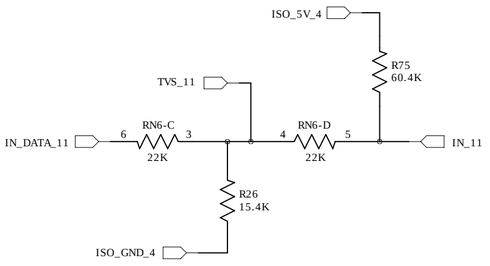

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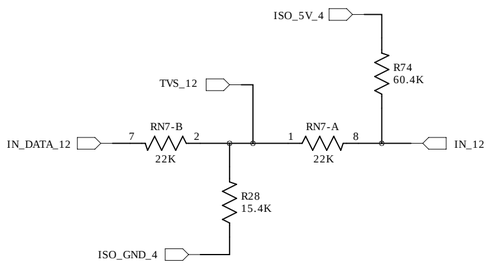

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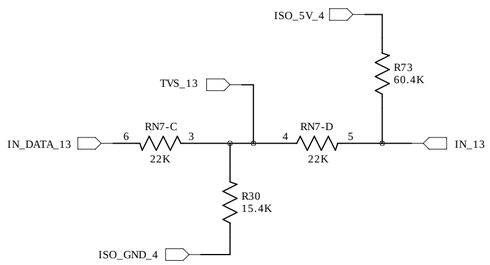

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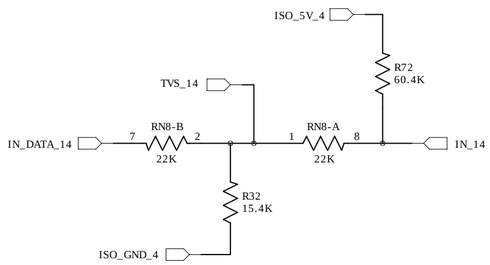
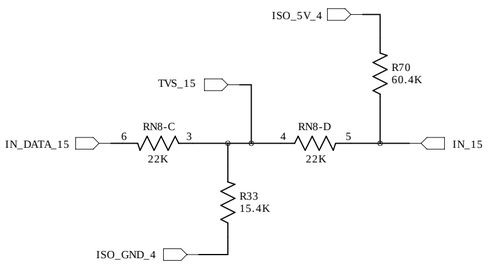
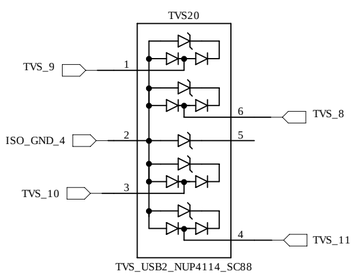
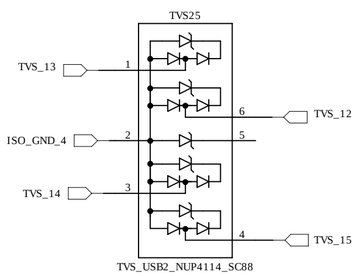


#15







Technologic Systems	Date June 15, 2015	
Title: TS-3Z-DIO Isolated Inputs 8-15		
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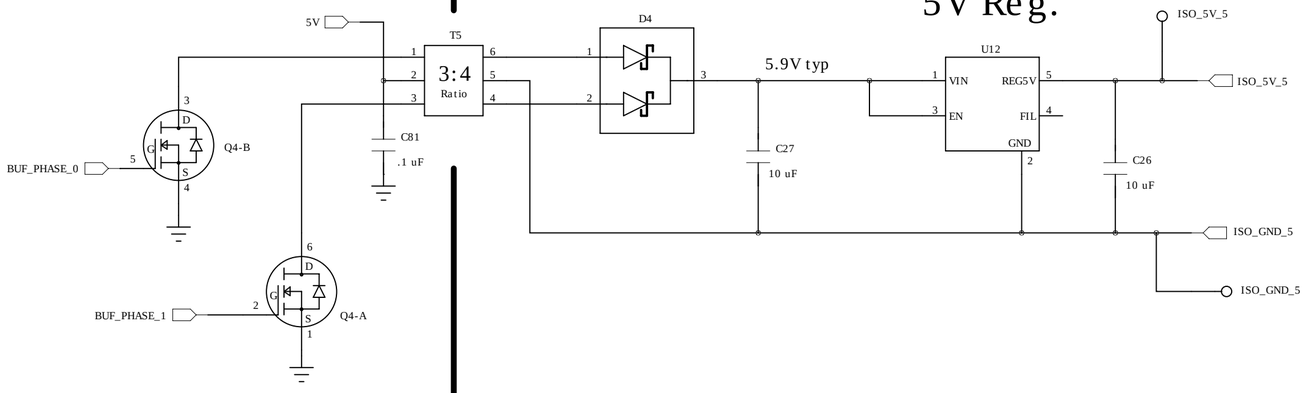
Phase_0# and Phase_1# must
be non-overlapping active high
51% low; 49% high duty cycle
and nominal 250 KHz
40 ns both off (low) at edges

Isolated Power

5V Reg.

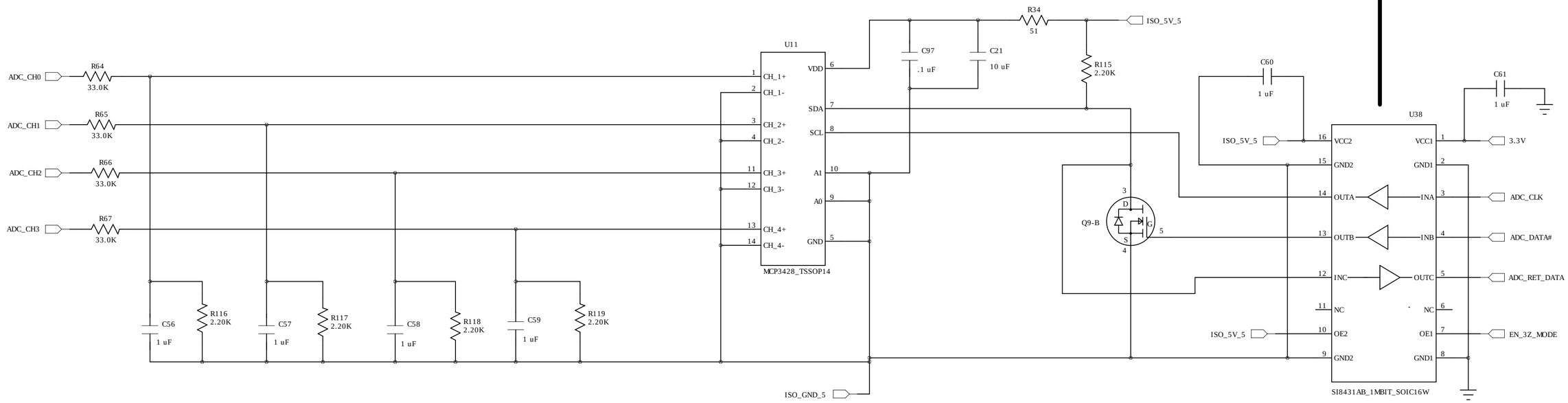


Analog Channels 0-3

0-30V range or 4-20 mA

TS-8100 uses this ADC chip

16-bit A/D



ADC notes

Input Impedance = 28 Kohm

45 Hz bandwidth
4 ms Time Con.

Technologic Systems	Date June 15, 2015	
Title: TS-3Z-DIO Isolated Analog Inputs 0-3		
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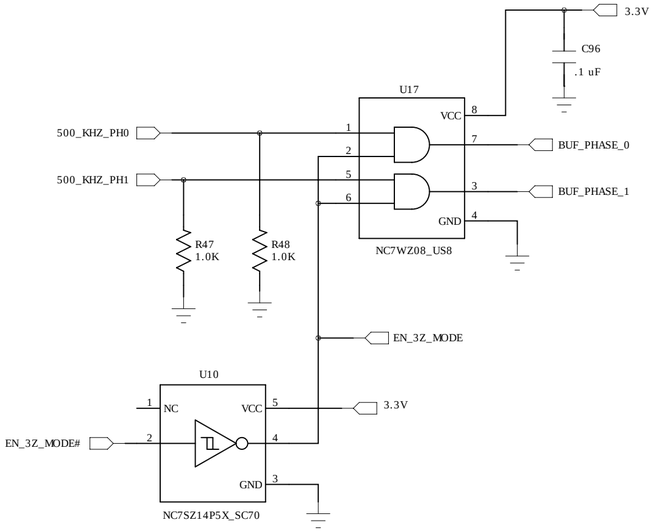
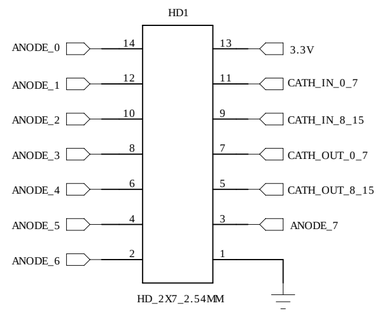
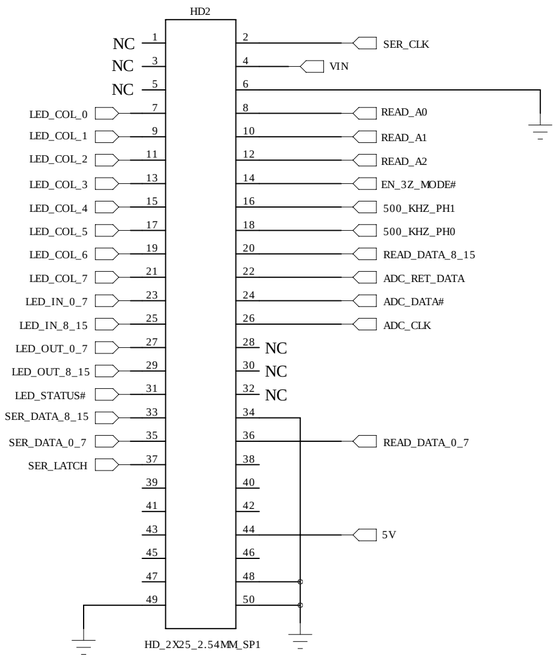
500 KHz Buffer

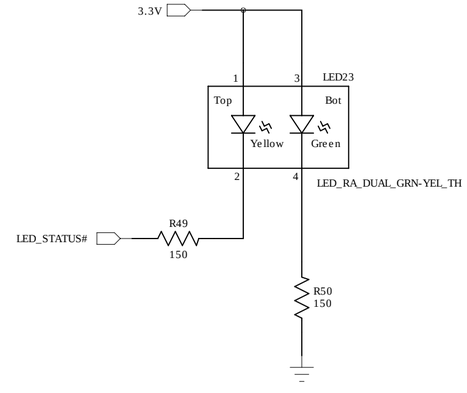




PC/104 Bus Connector



Status - Power



Technologic Systems	Date June 15, 2015	
Title: TS-3Z-DIO PC/104 bus and Misc.		
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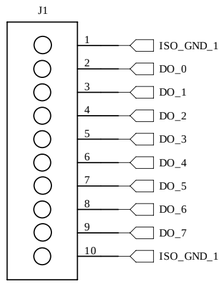
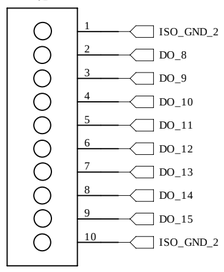
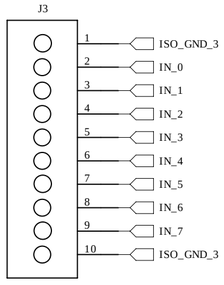
4 x 10 and 1 x 6 Screw Term. Connectors



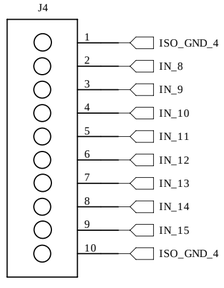
Outputs 0-7



Outputs 8-15

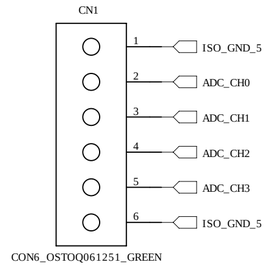


Inputs 0-7

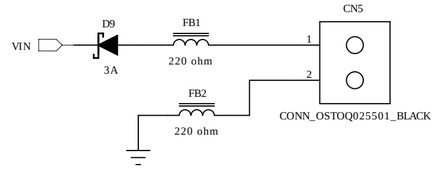


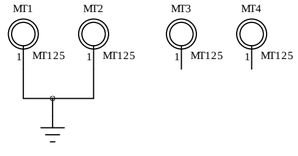
Inputs 8-15

Analog 0-3



8-28 VDC Power Input





Technologic Systems	Date June 15, 2015	
Title: TS-3Z-DIO Screw term. Conn.		
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