

TS-3Z-DIO

Designed for use with TS-7250-V2

This board has 5 isolated islands

Two groups of 8 isolated Inputs 0-30V (16 total)

Two groups of 8 isolated Outputs 0-30V, 2A (16 total)

One group of 4 isolated Analog Inputs 0-32V

All 5 groups are isolated from each other
and from the TS-7250-V2 SBC

BOM Issues

R71-R86 (60.4K) are not populated

These are PU on the Inputs 0-15

R43 and R44 not populated (only needed if using PU)

Rev.A to Rev.B Changes

High side FET switches added to all 16 outputs

All 16 outputs can be low-side switches to GND
or High-side switches to V-High

V-High source is the screw term connector (STC)

The left most position on STC is now V-High

V-High Max is 28VDC

Note: On Rev.A there were two GND STC positions

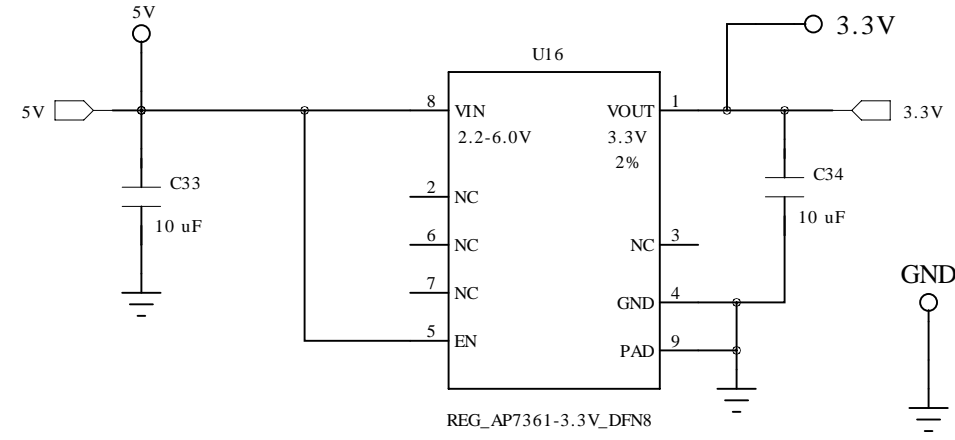
On Rev.B there is only one position

For each Output, if High-side FET ON, it forces Low-side FET OFF

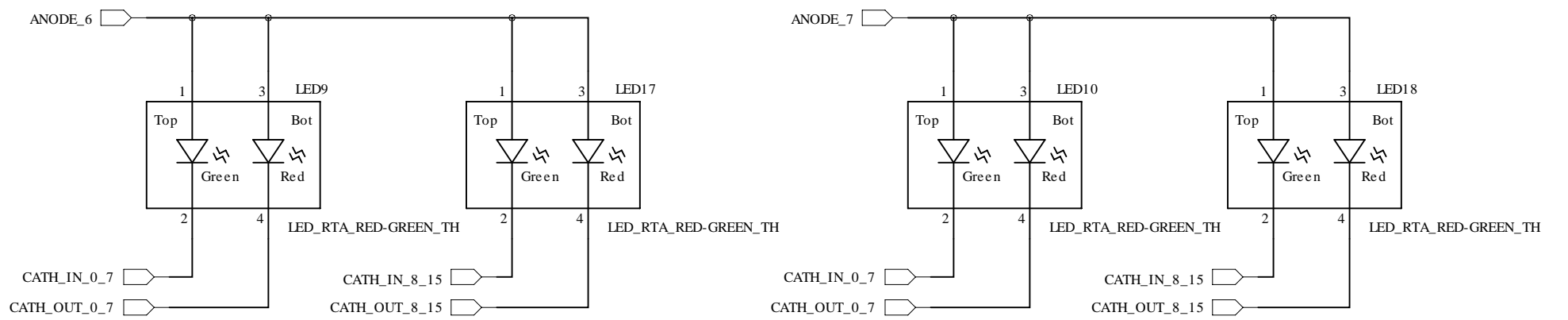
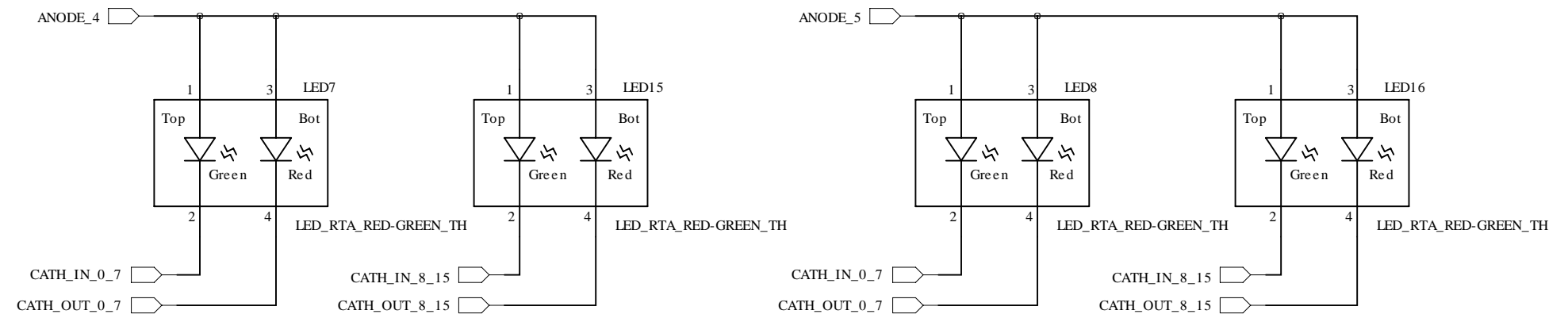
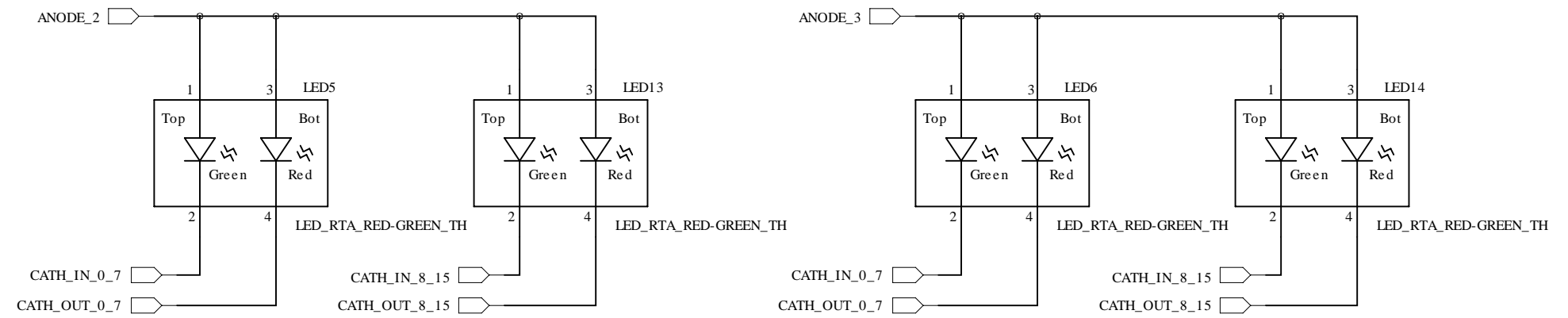
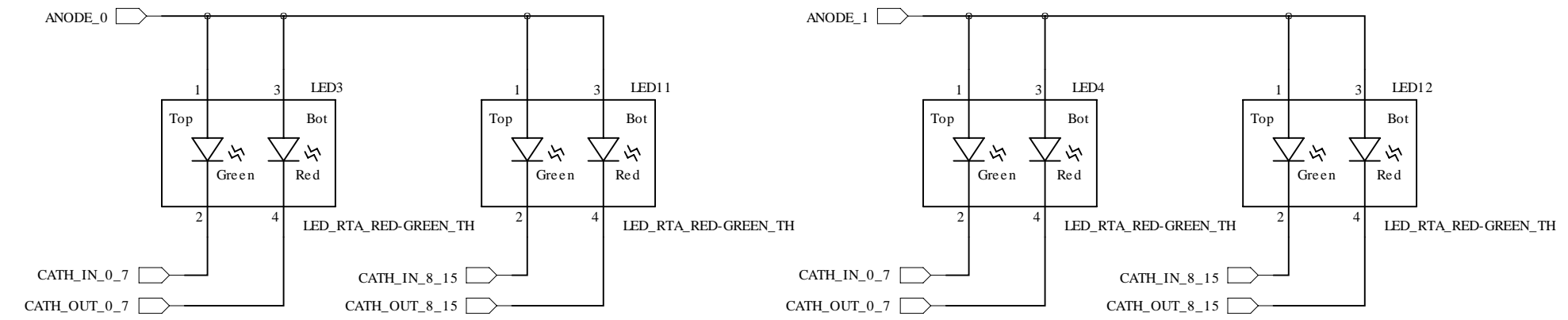
This prevents both ON - which would cause very high current

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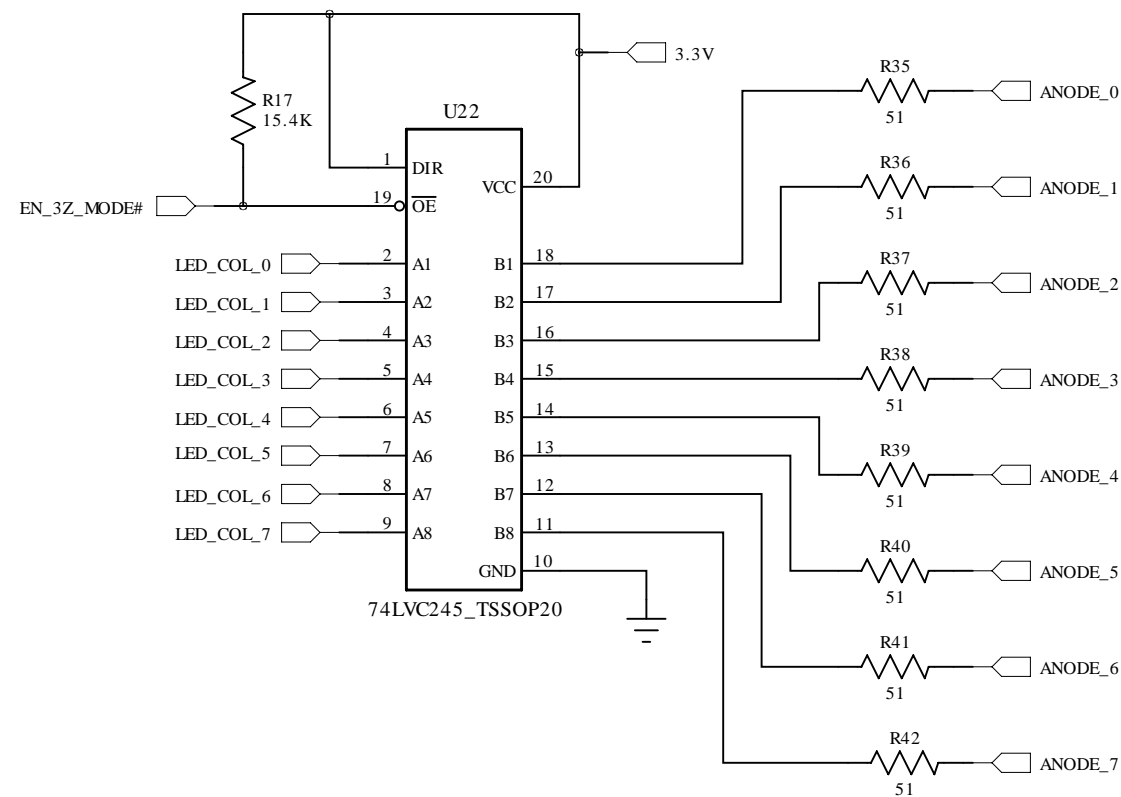
Linear 3.3V Reg.



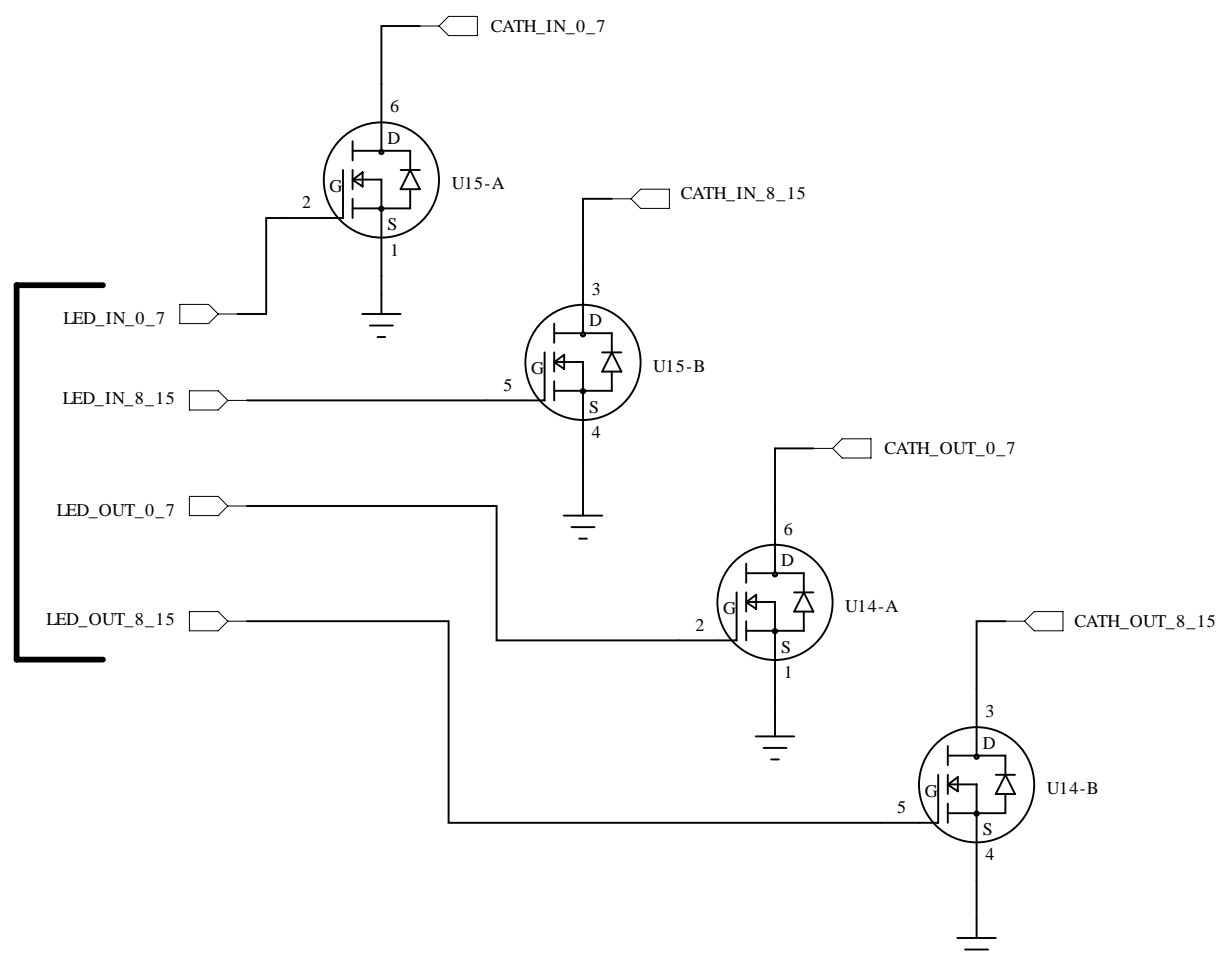
Red/Green LEDs



LED Drivers



400 Hz
1 of 4 true

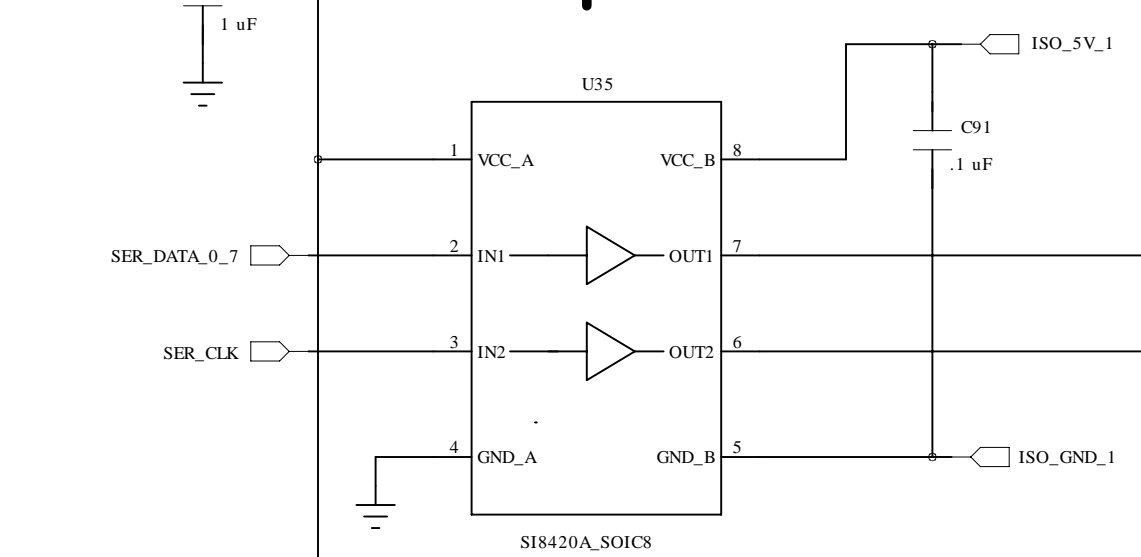
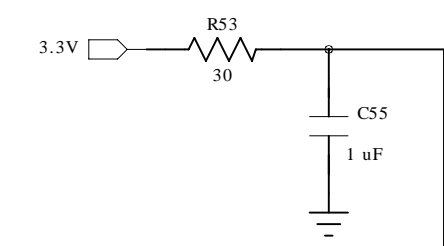
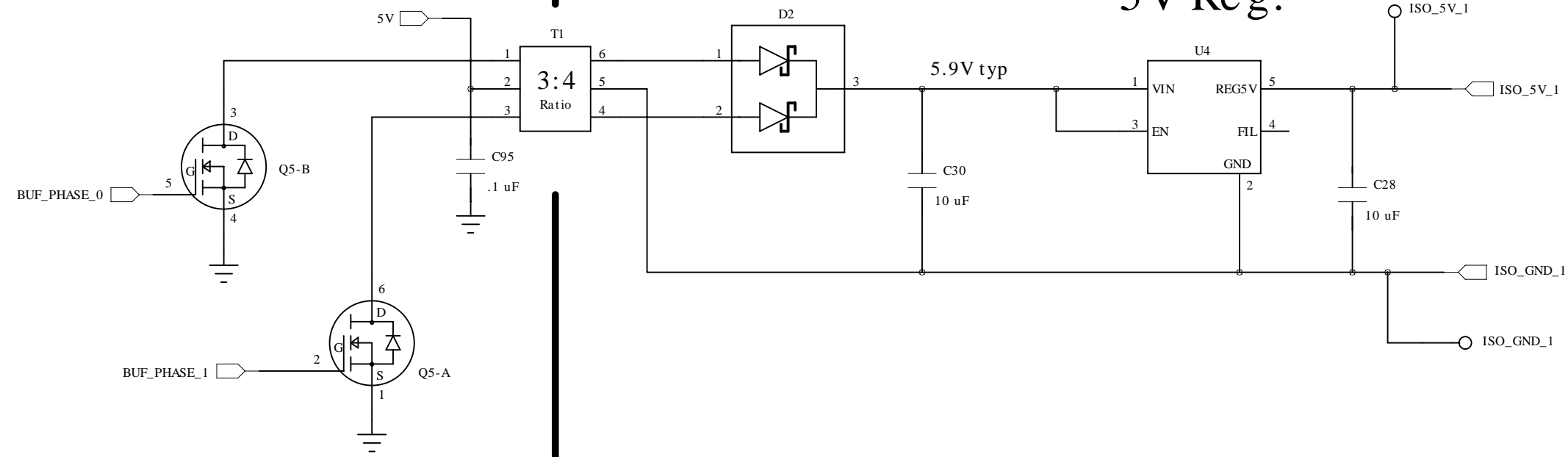


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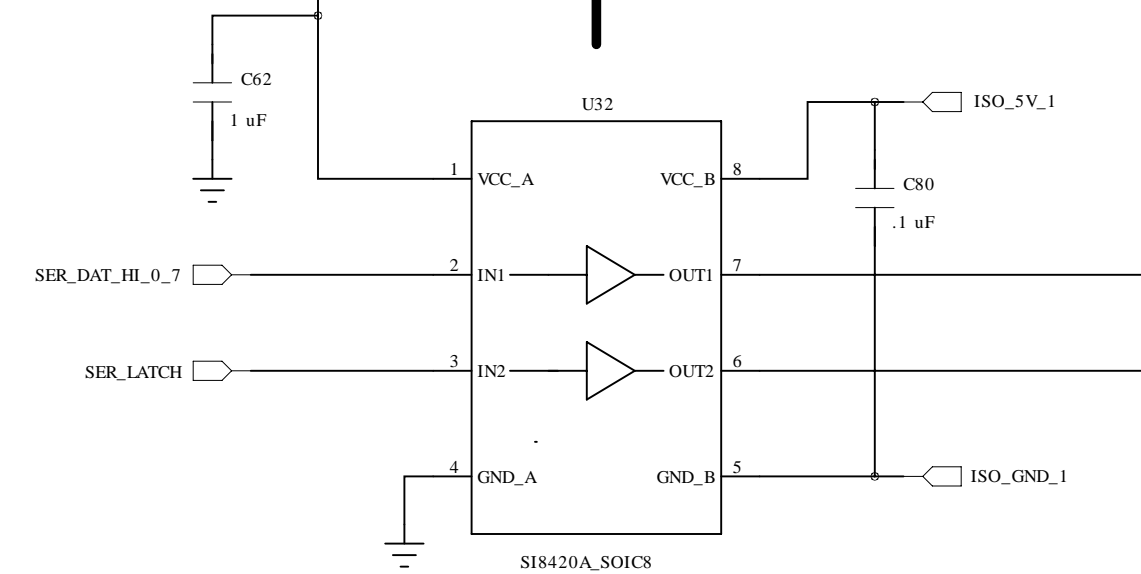
Phase_0# and Phase_1# must be non-overlapping active high 51% low; 49% high duty cycle and nominal 250 KHz 40 ns both off (low) at edges

Isolated Power

5V Reg.



8 bit Shift Reg.
Outputs 0-7



8 bit Shift Reg.
High side Outputs 0-7

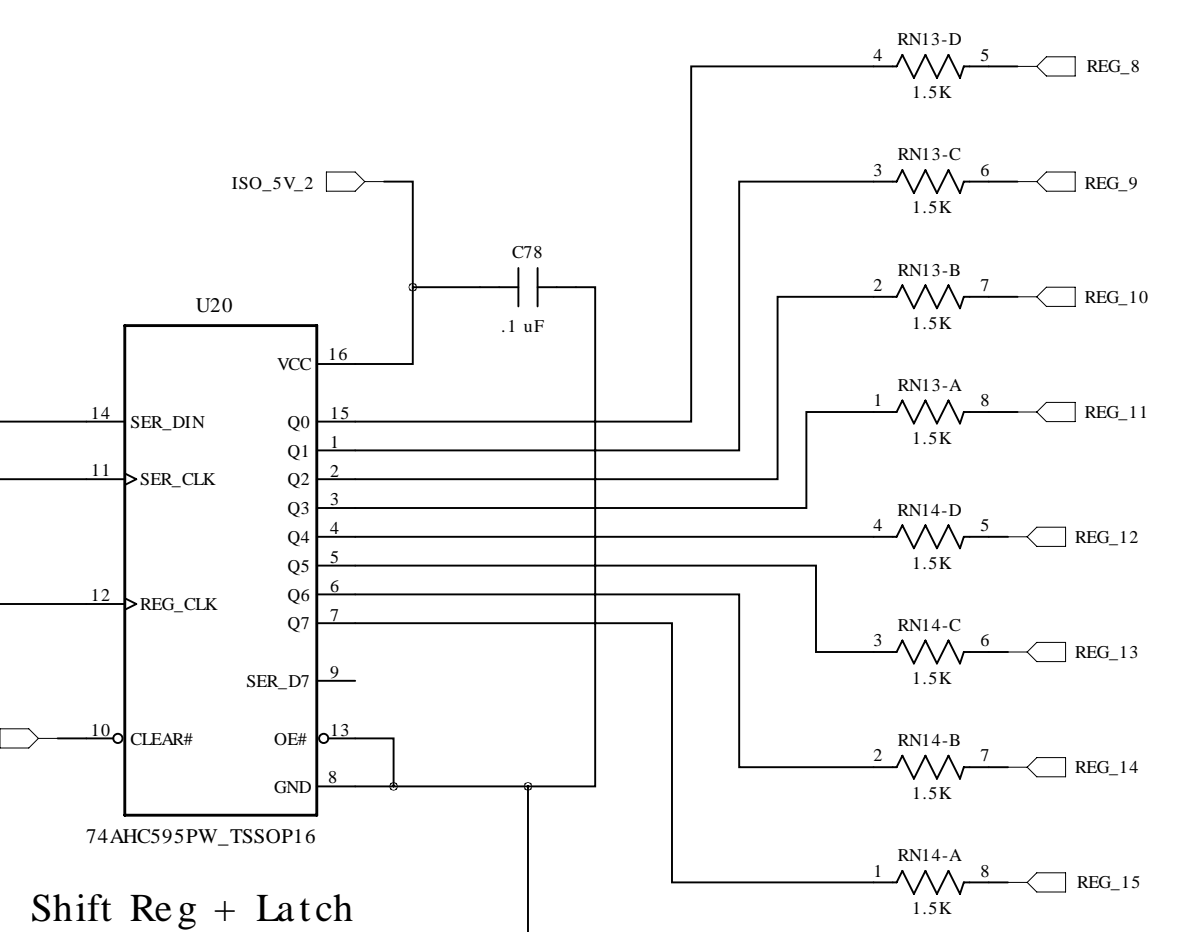
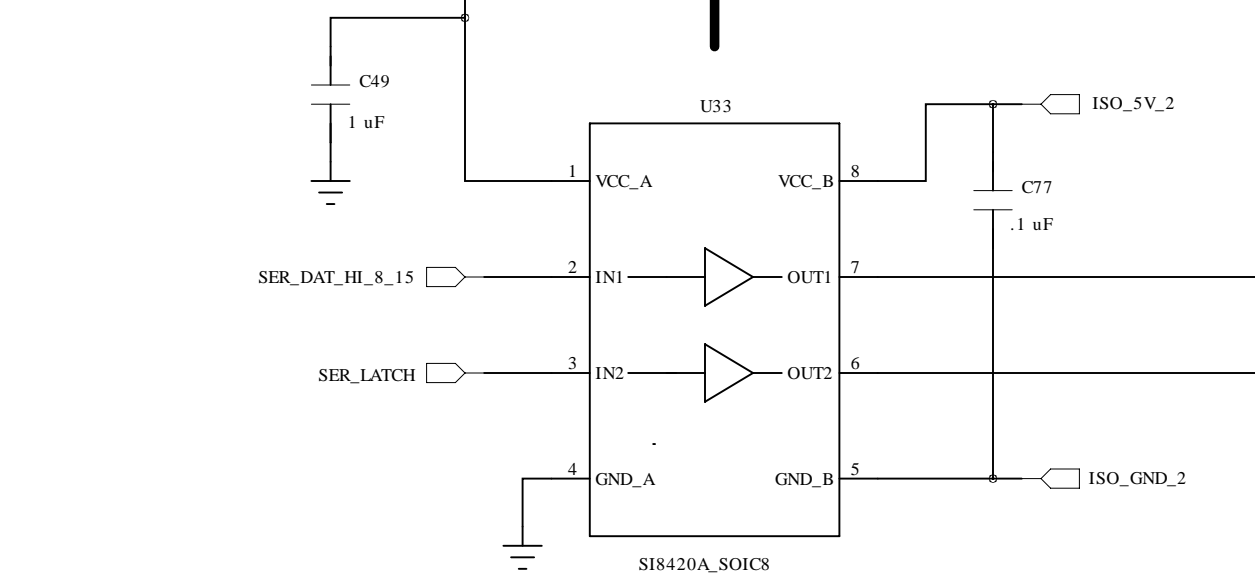
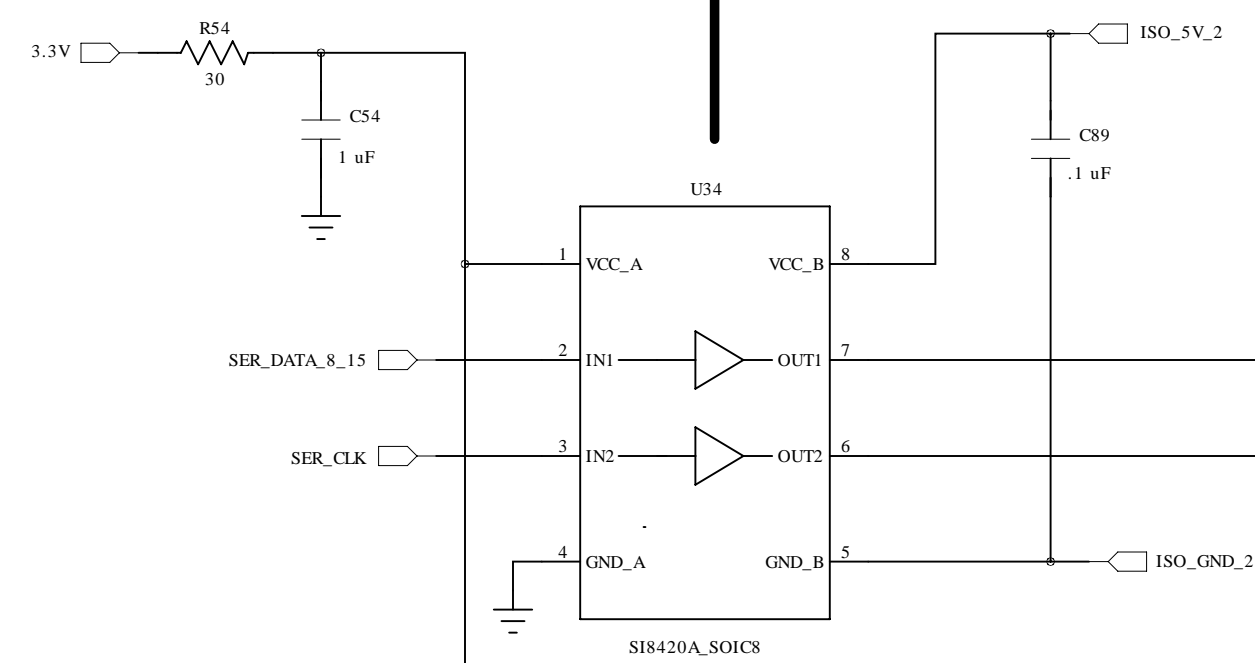
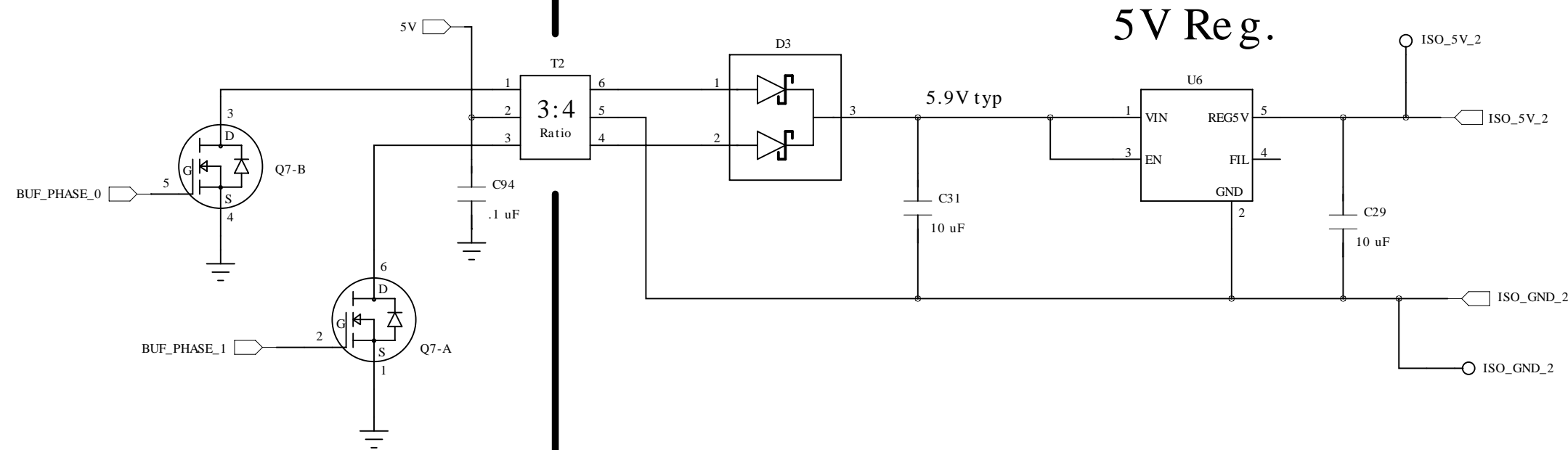
Shift Reg + Latch

Shift Reg + Latch

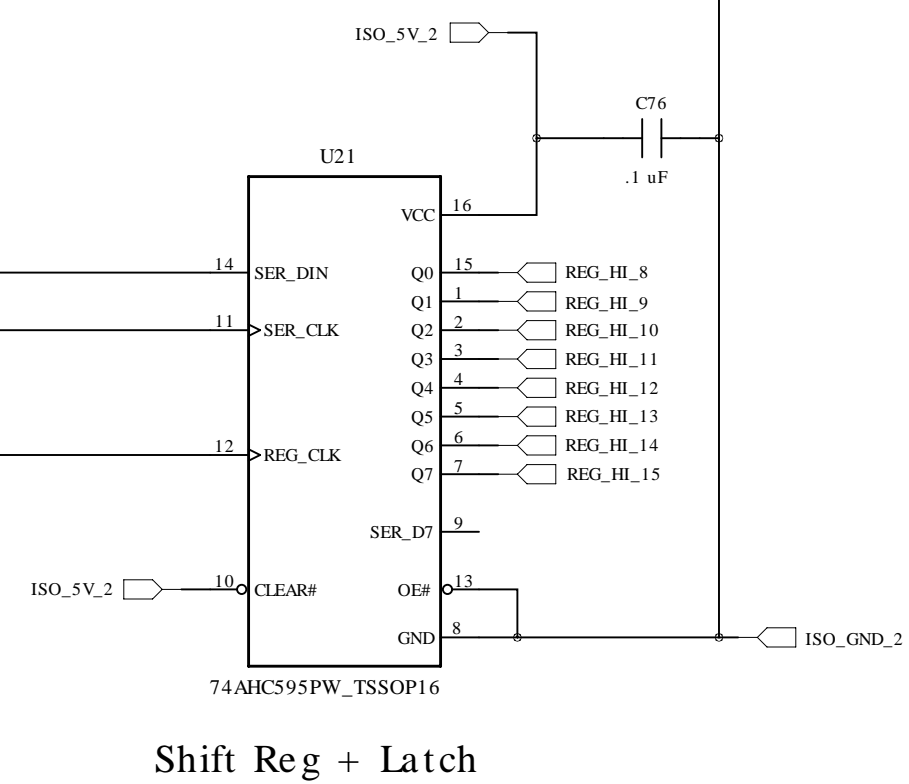
Technologic Systems	Date May 15, 2016
Title: TS-3Z-DIO Isolated Outputs 0-7	
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Phase_0# and Phase_1# must be non-overlapping active high
51% low; 49% high duty cycle
and nominal 250 KHz
40 ns both off (low) at edges

Isolated Power



8 bit Shift Reg.
Outputs 8_15

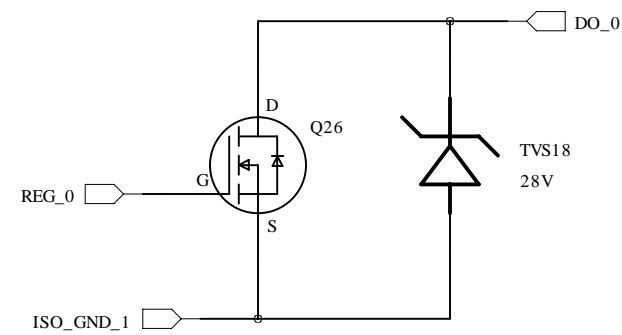


8 bit Shift Reg.
High side Outputs 8_15

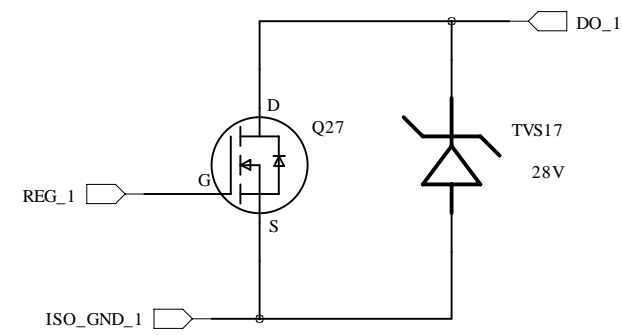
Dig. Outputs (30V Open Drain)

2A sink for each Output

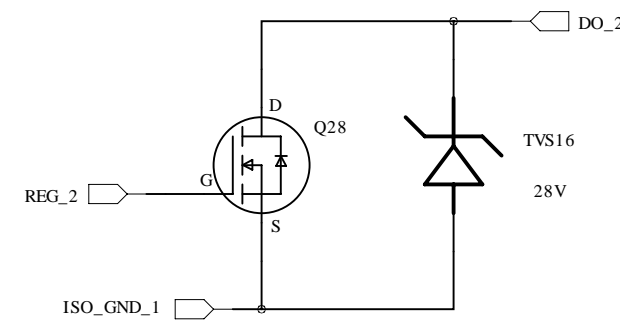
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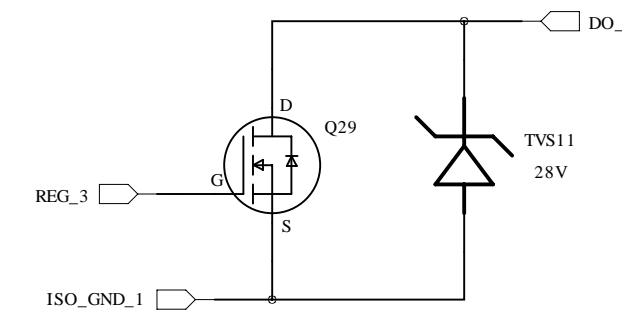
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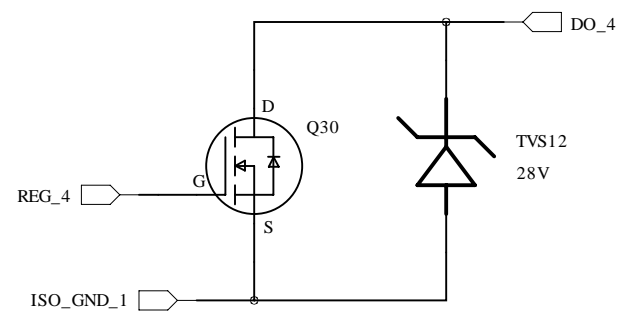
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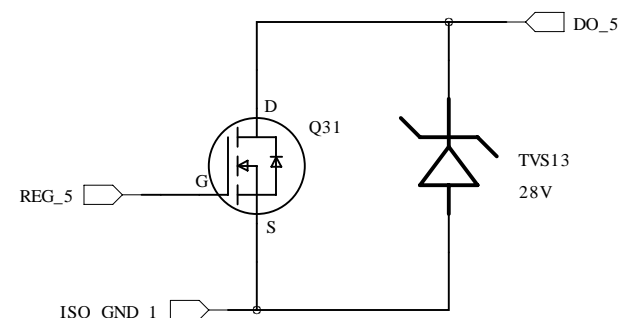
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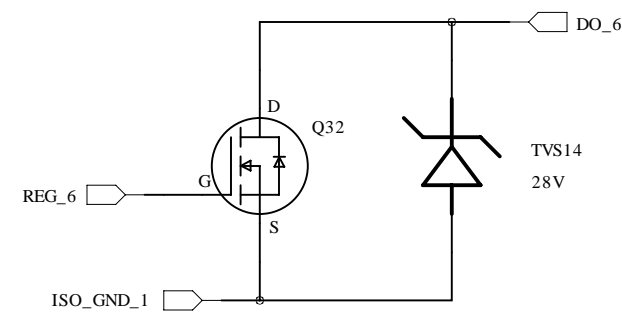
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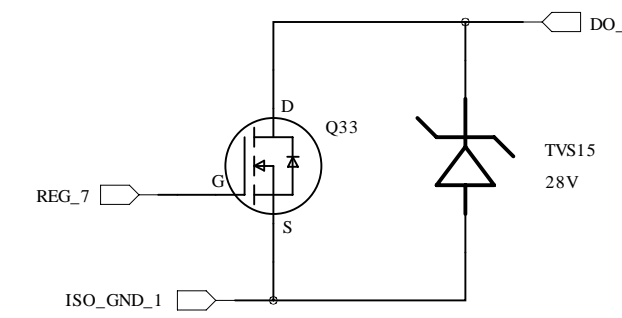
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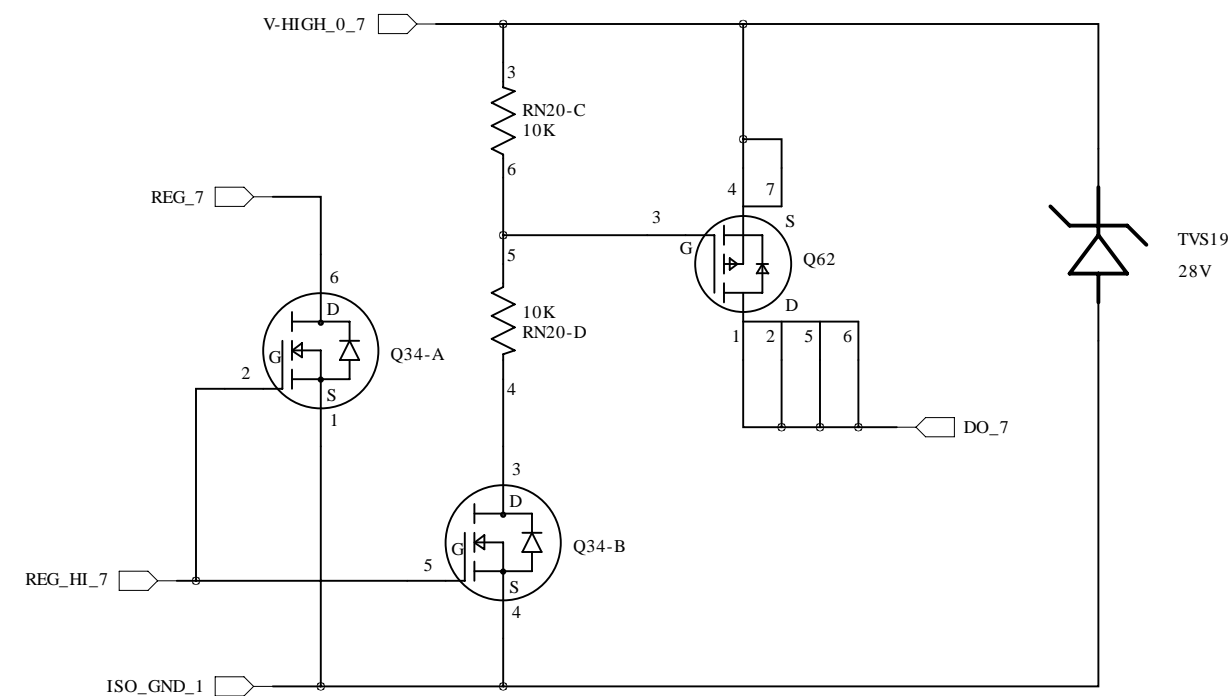
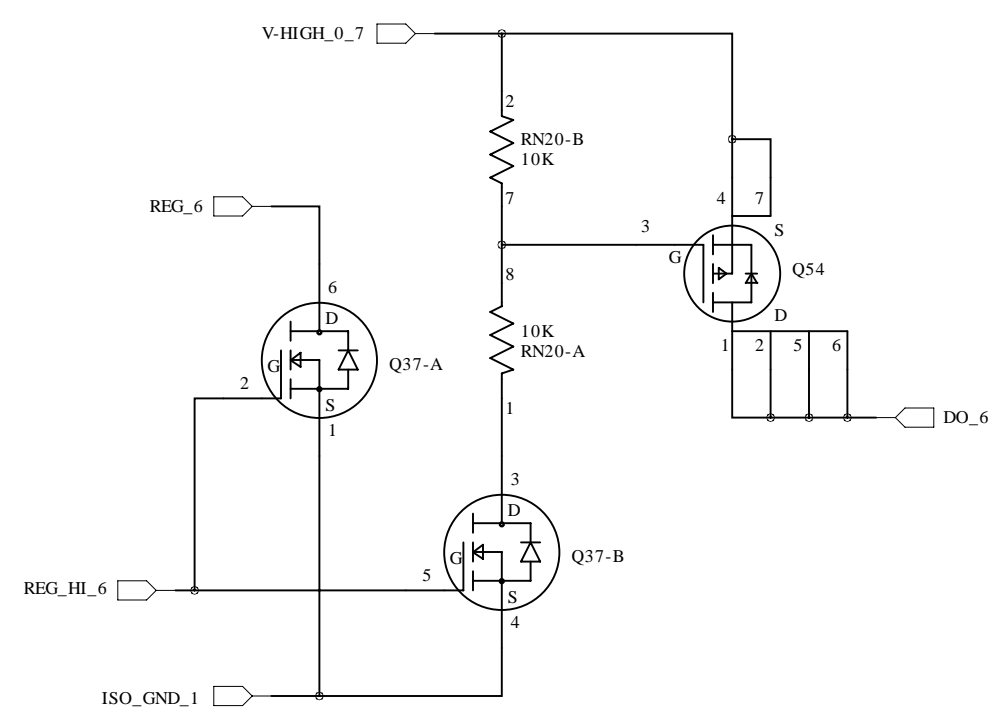
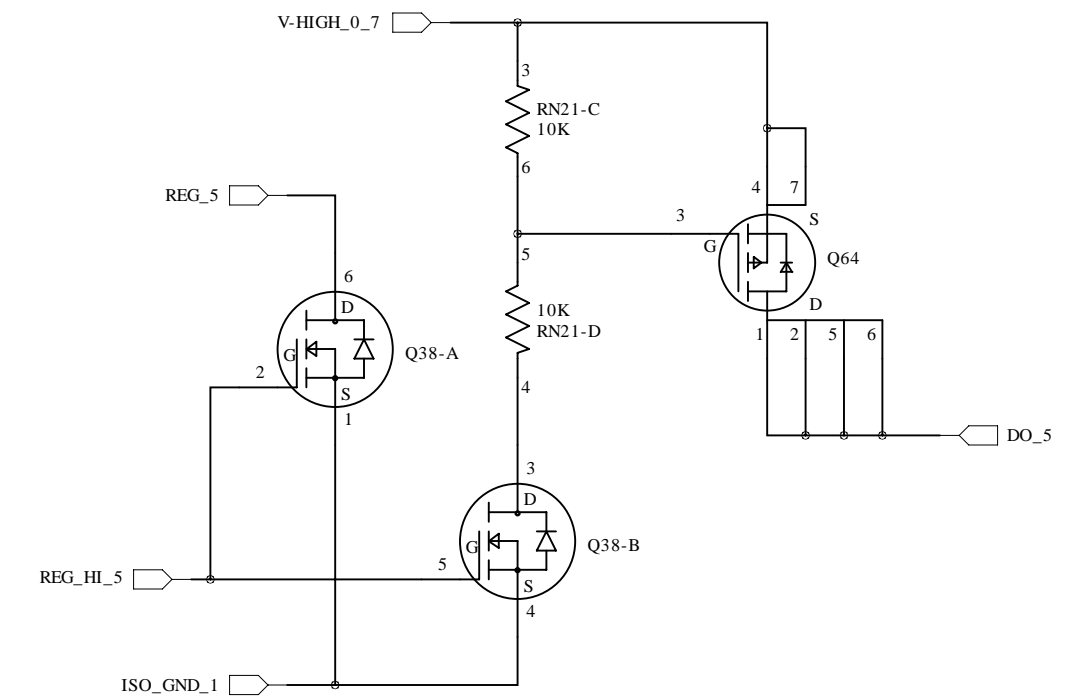
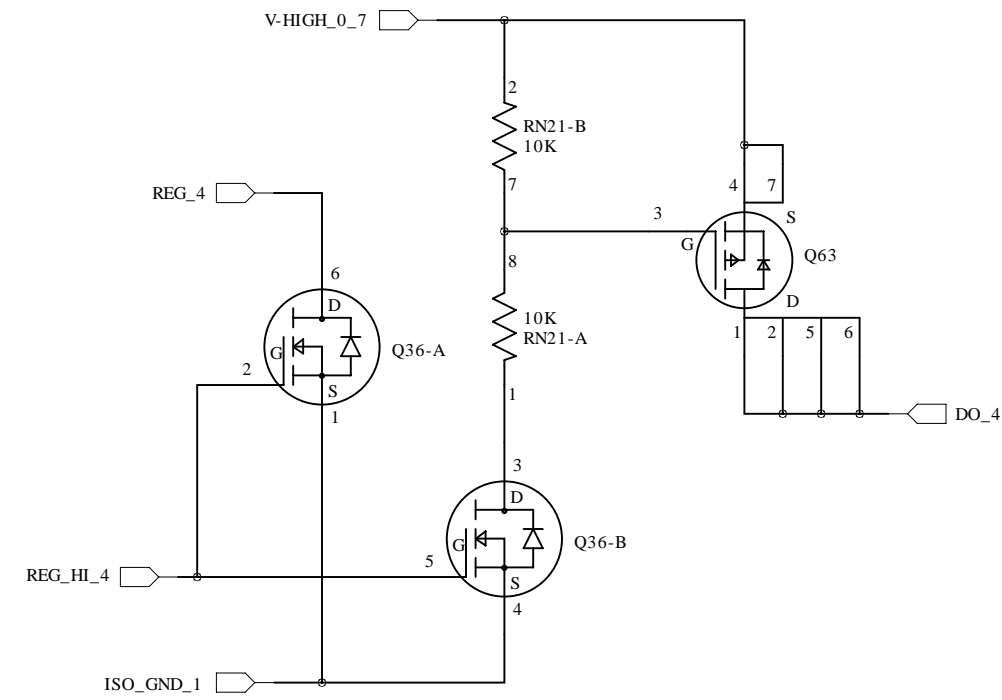
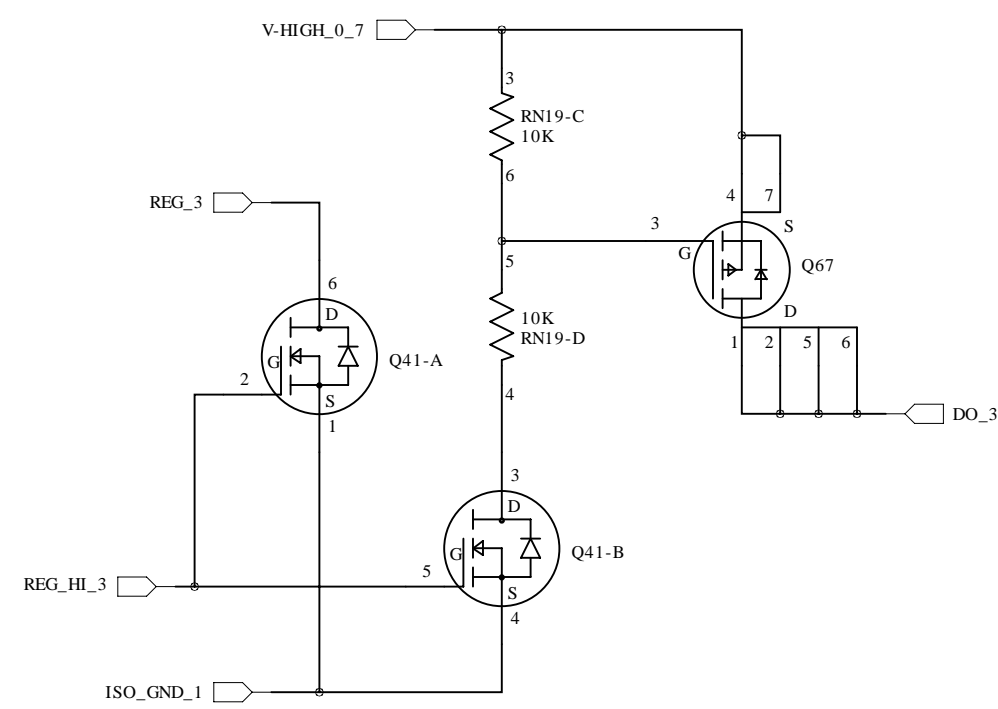
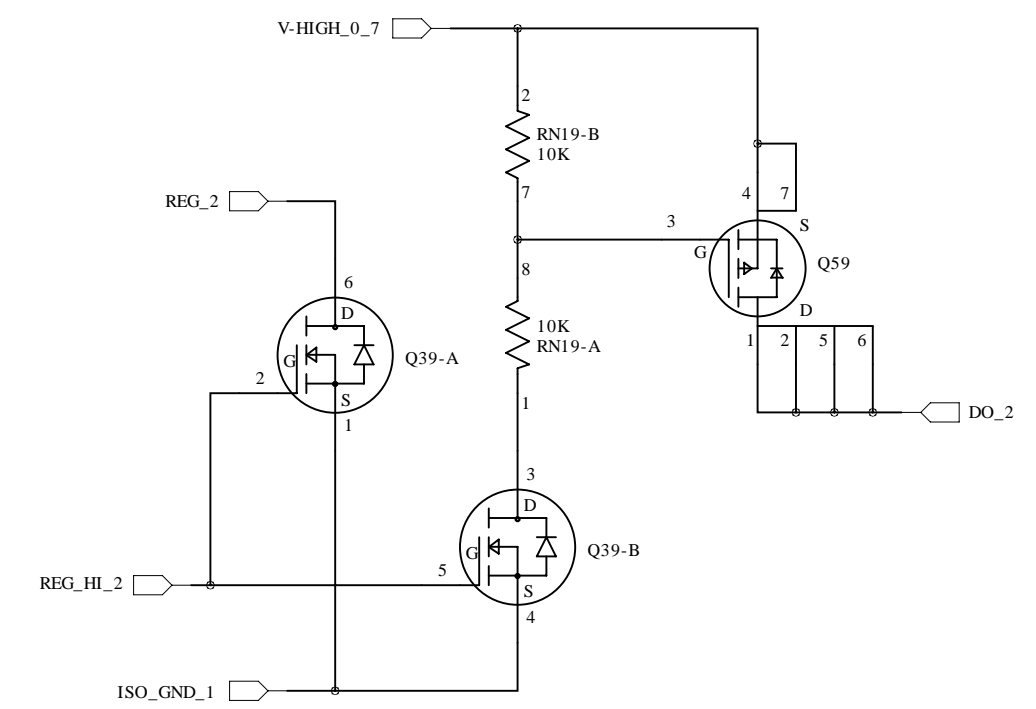
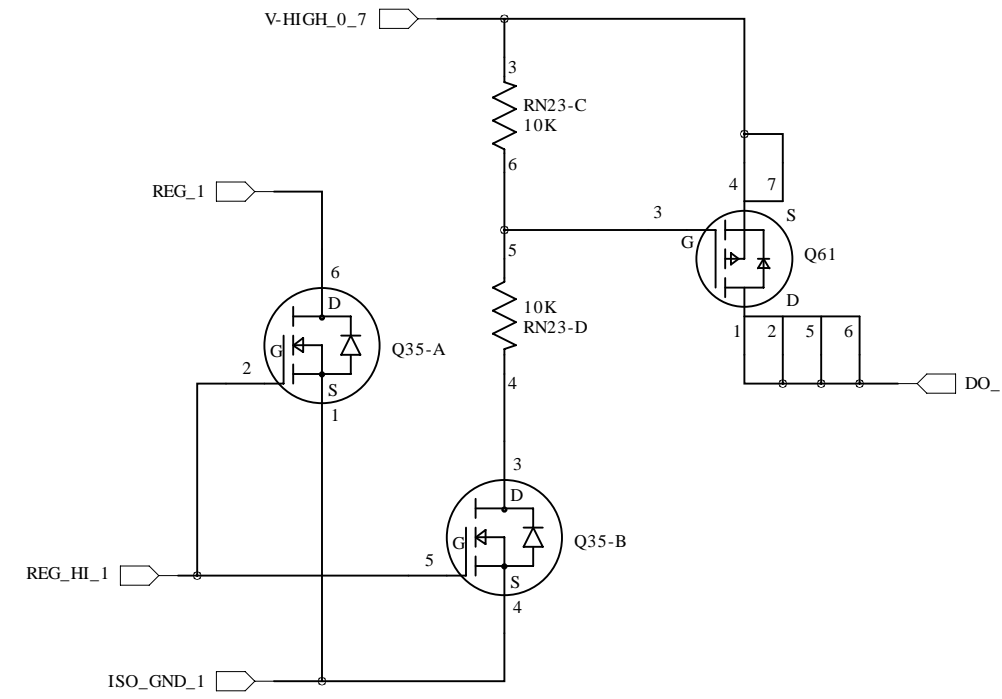
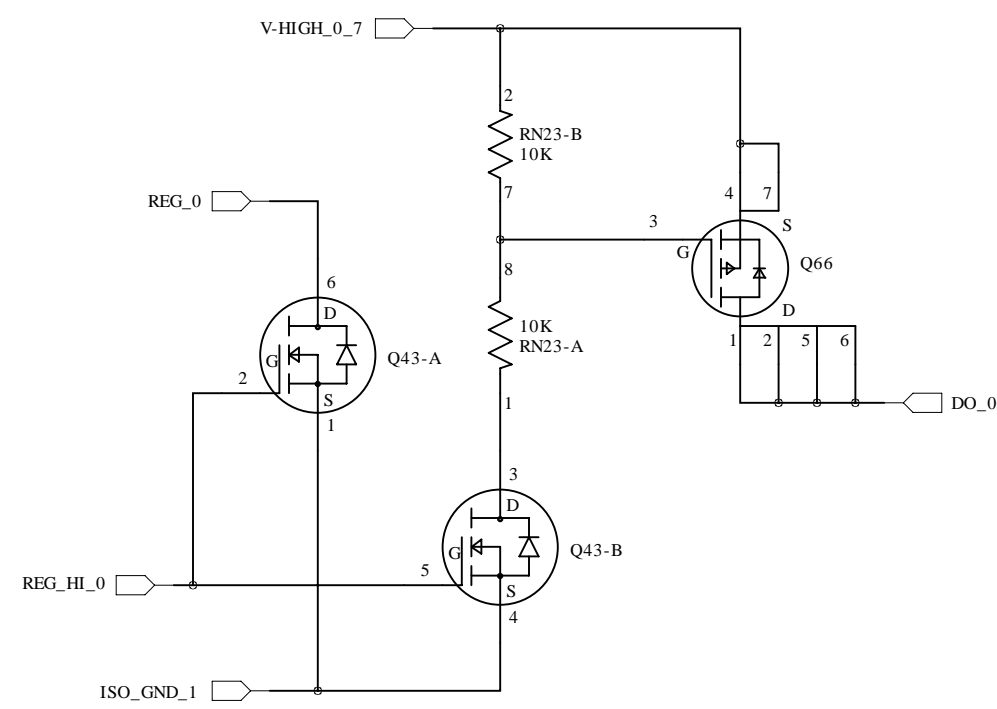


7



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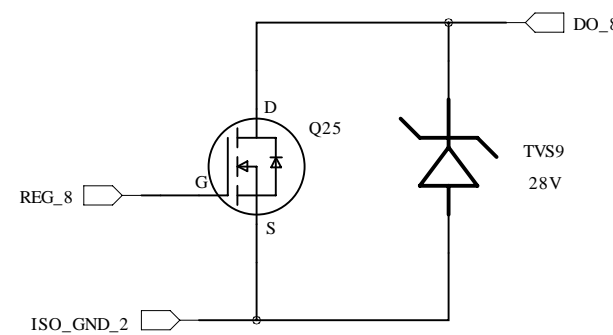
High Side FETs 0-7



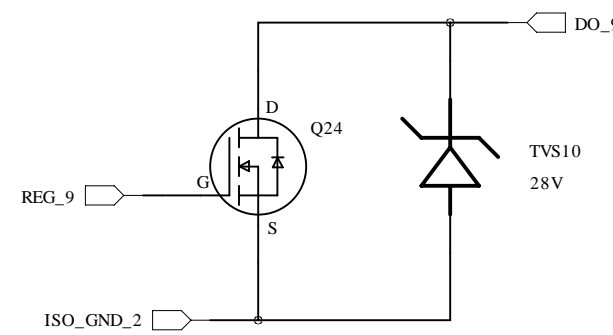
Dig. Outputs (30V Open Drain)

2A sink for each Output

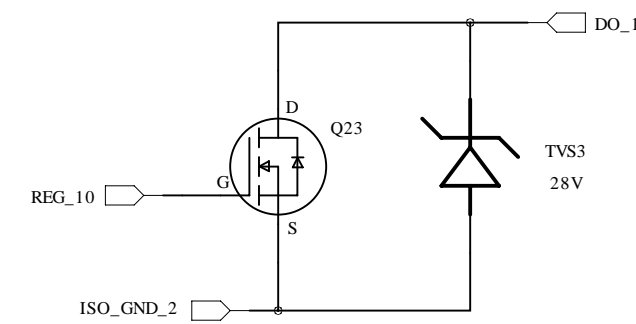
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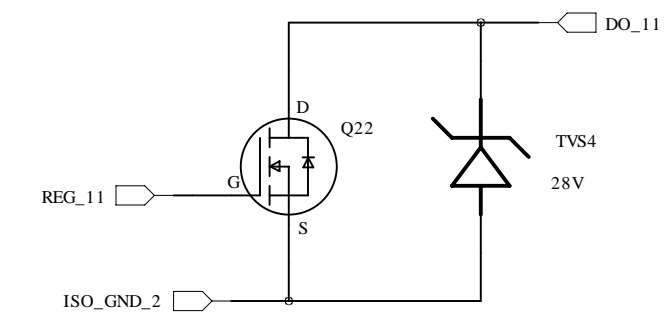
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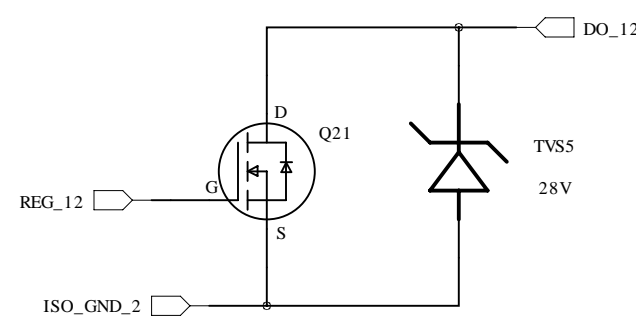
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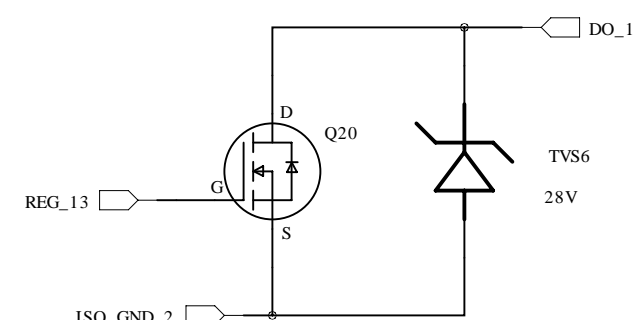
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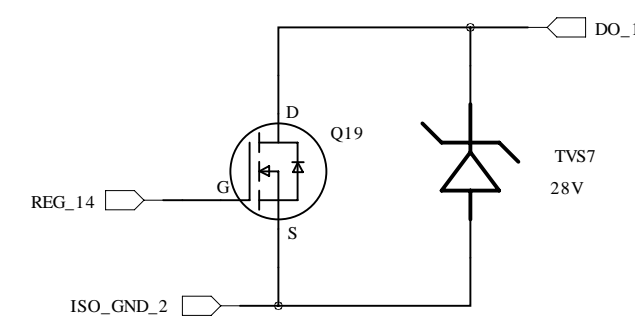
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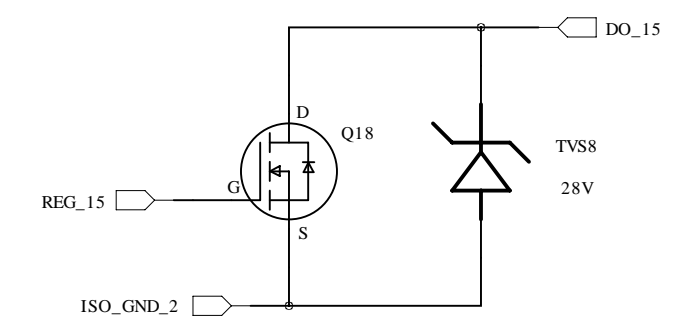
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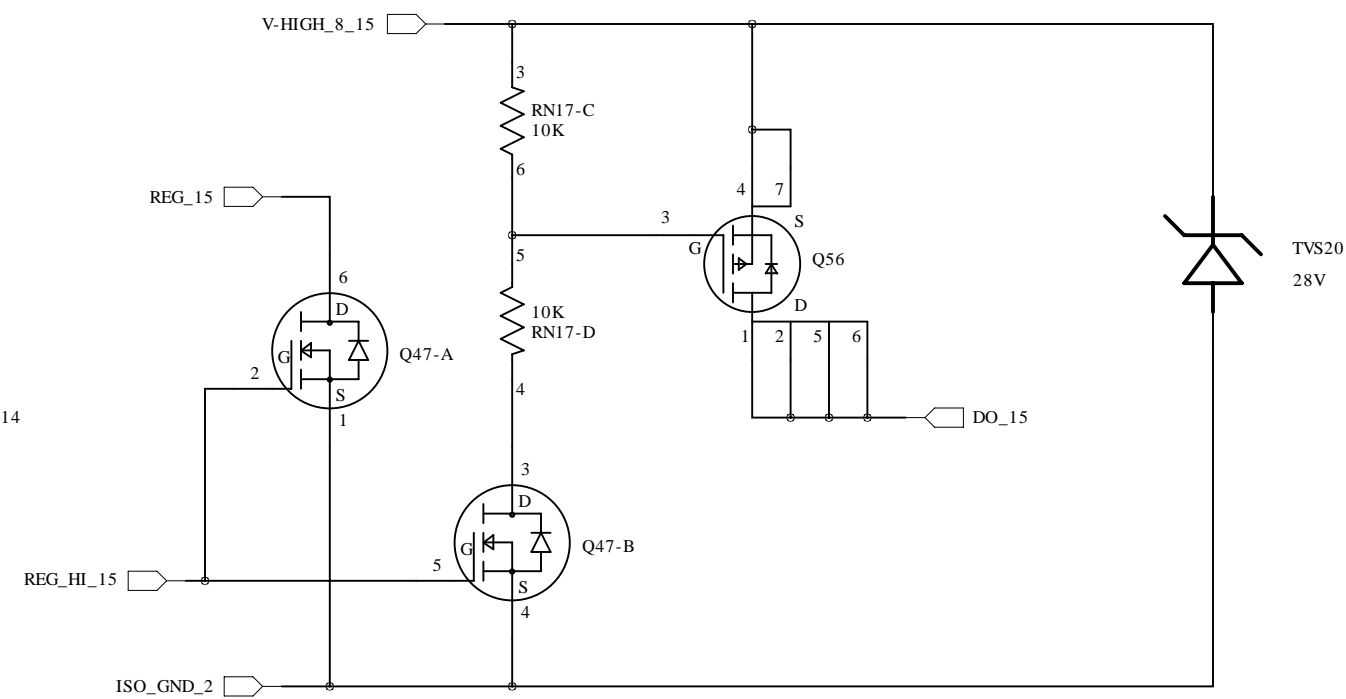
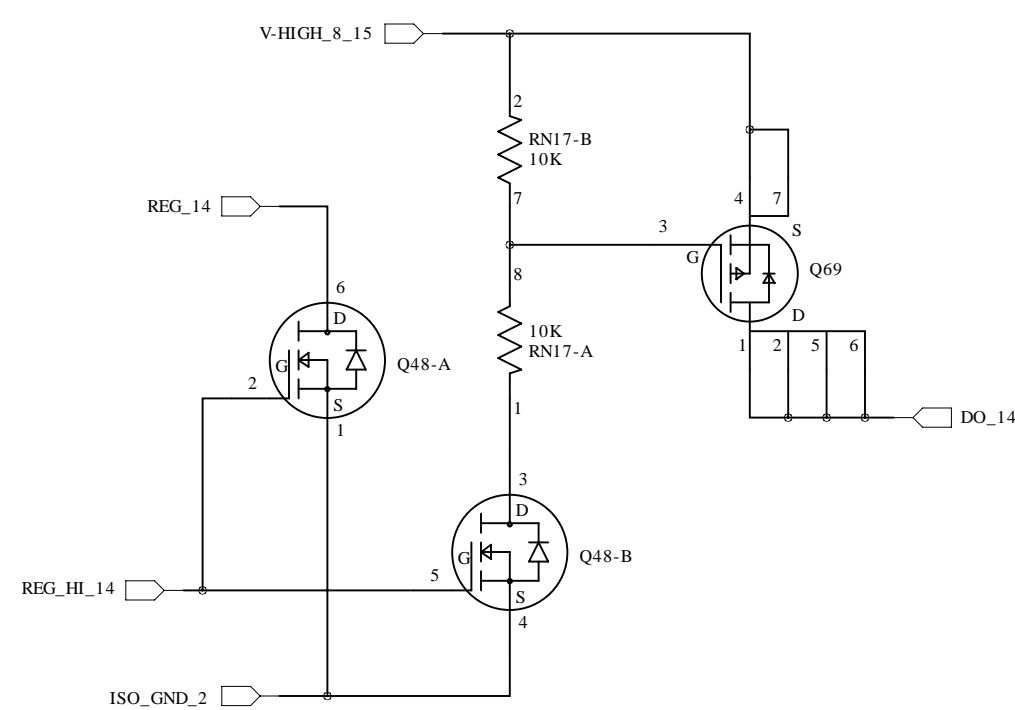
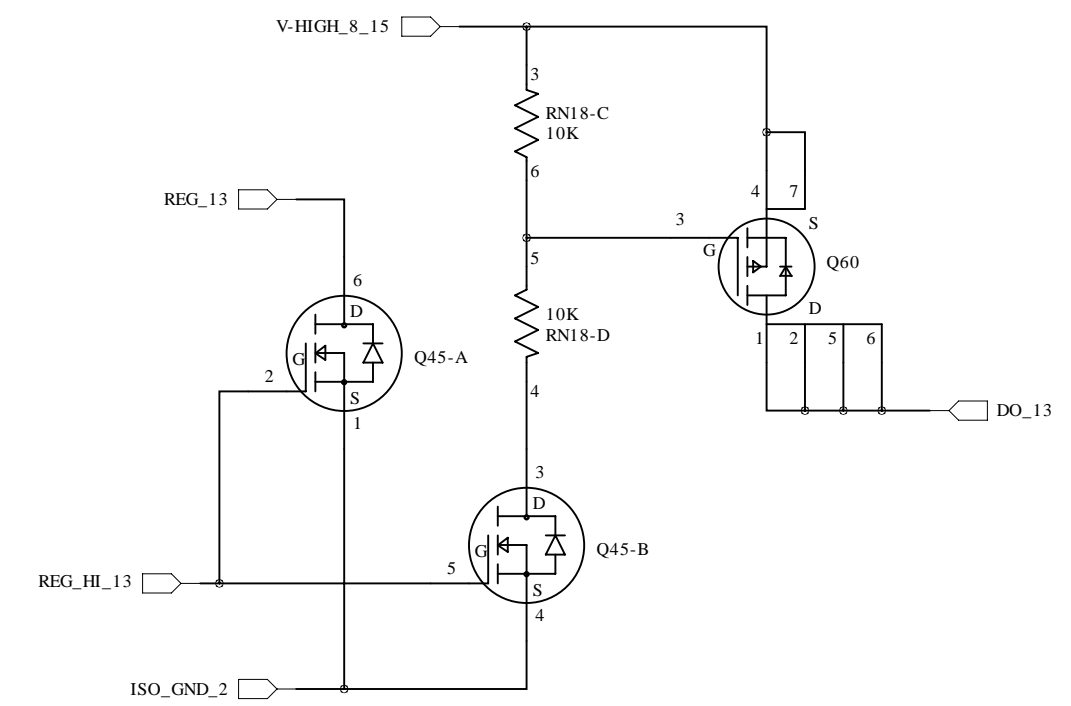
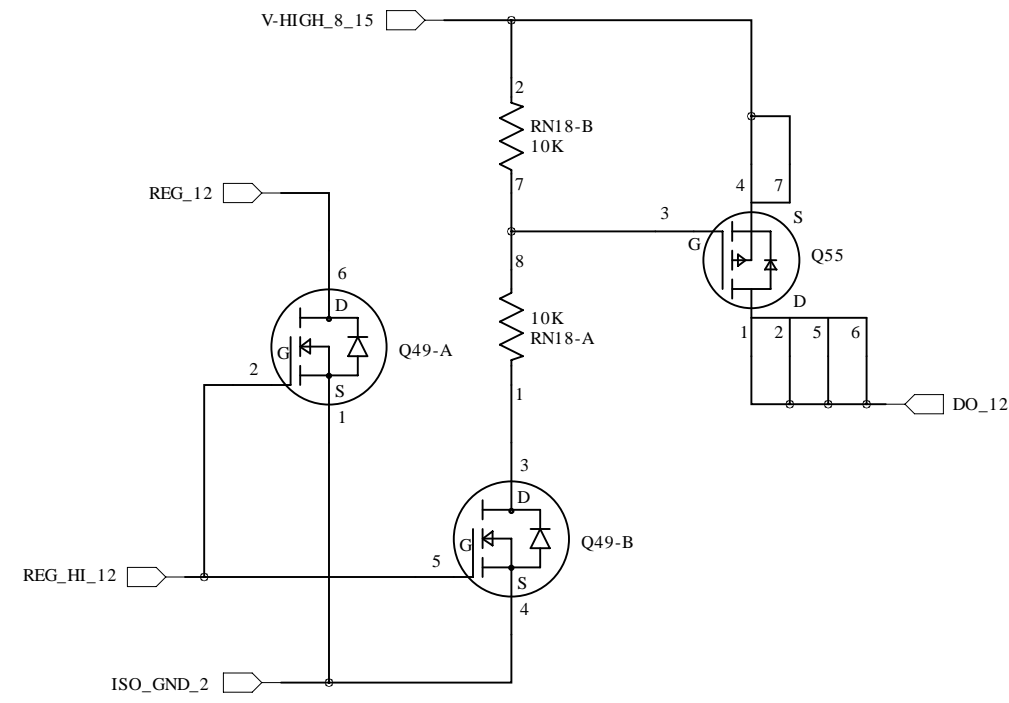
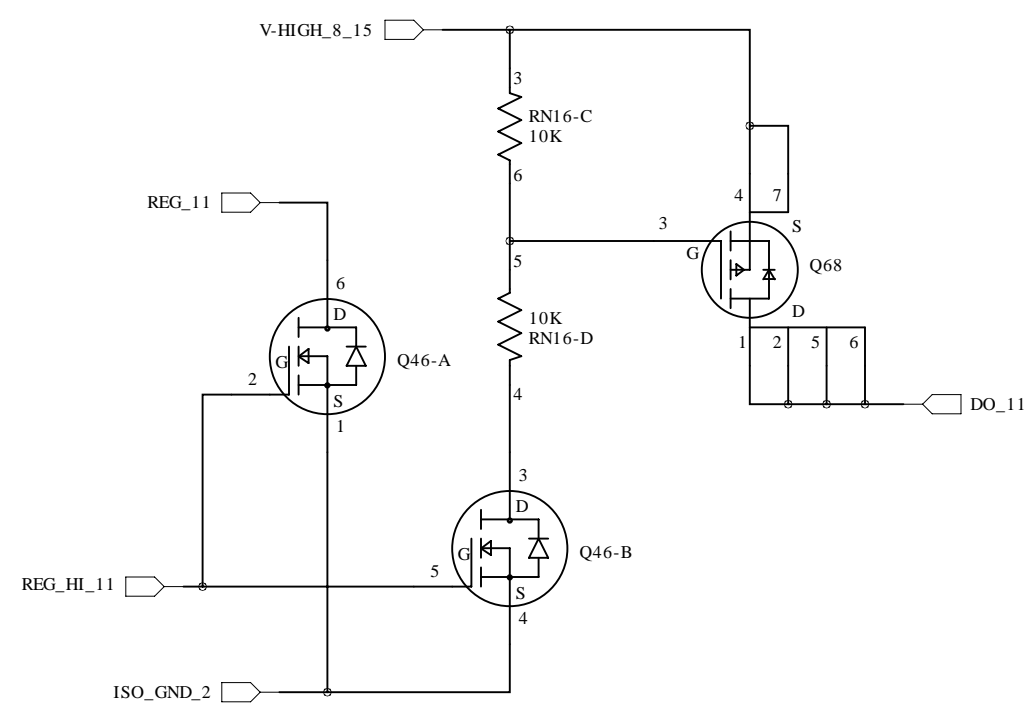
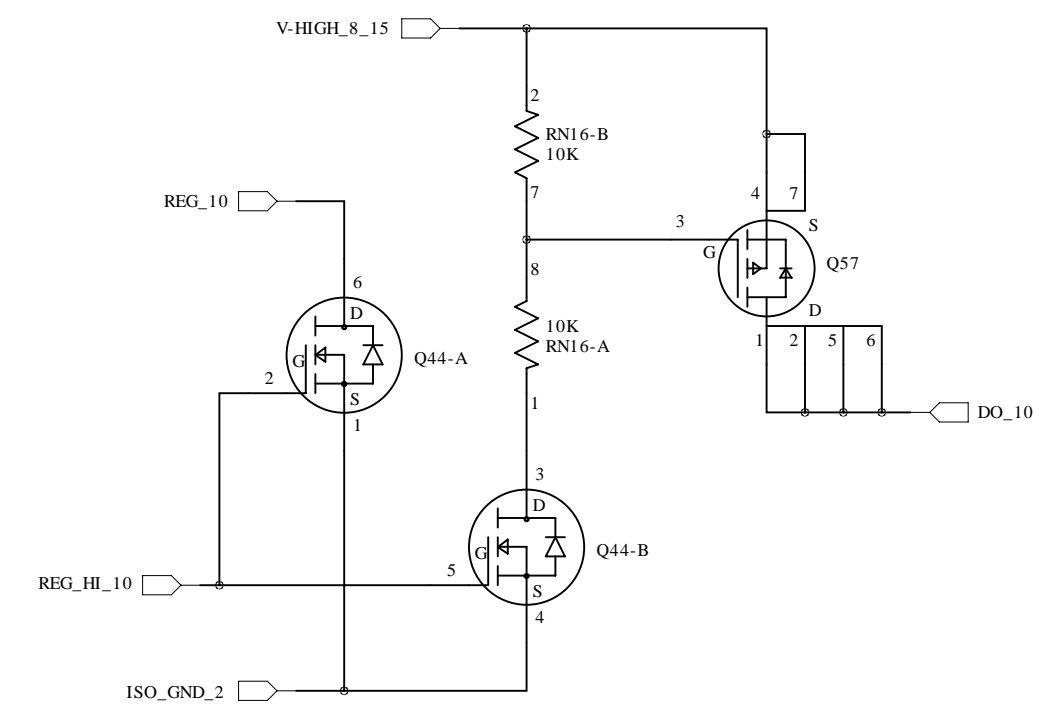
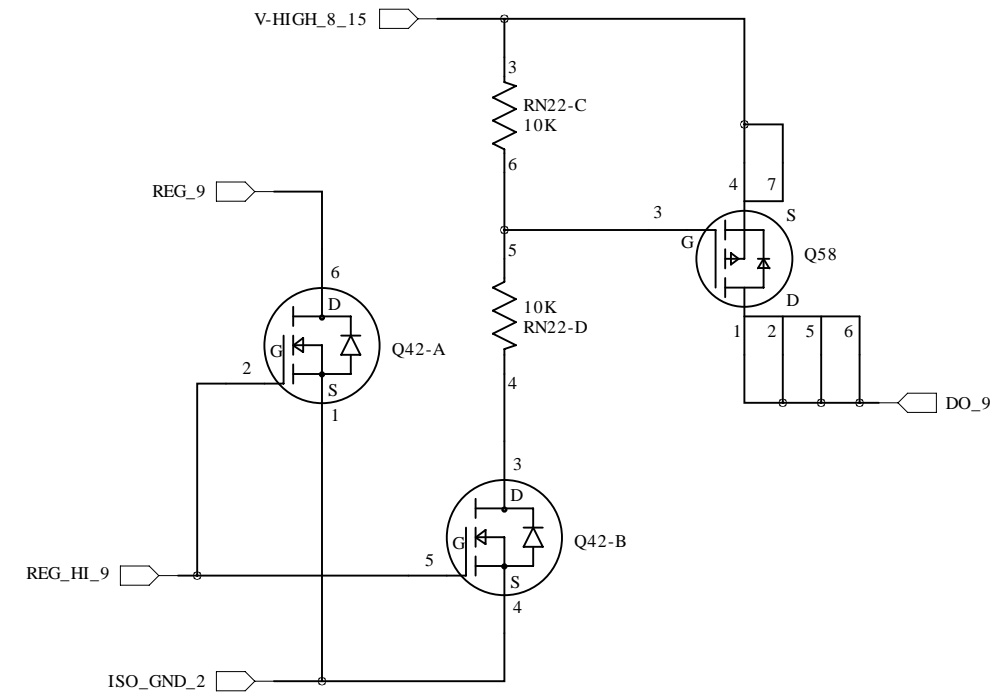
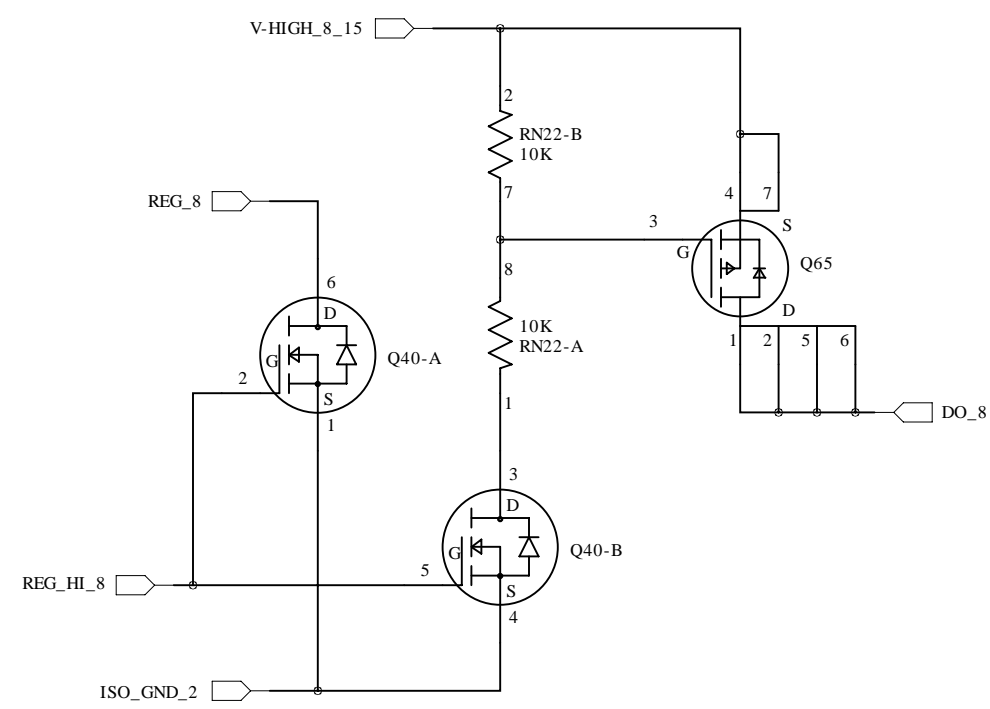
14



15



High Side FETs 8-15

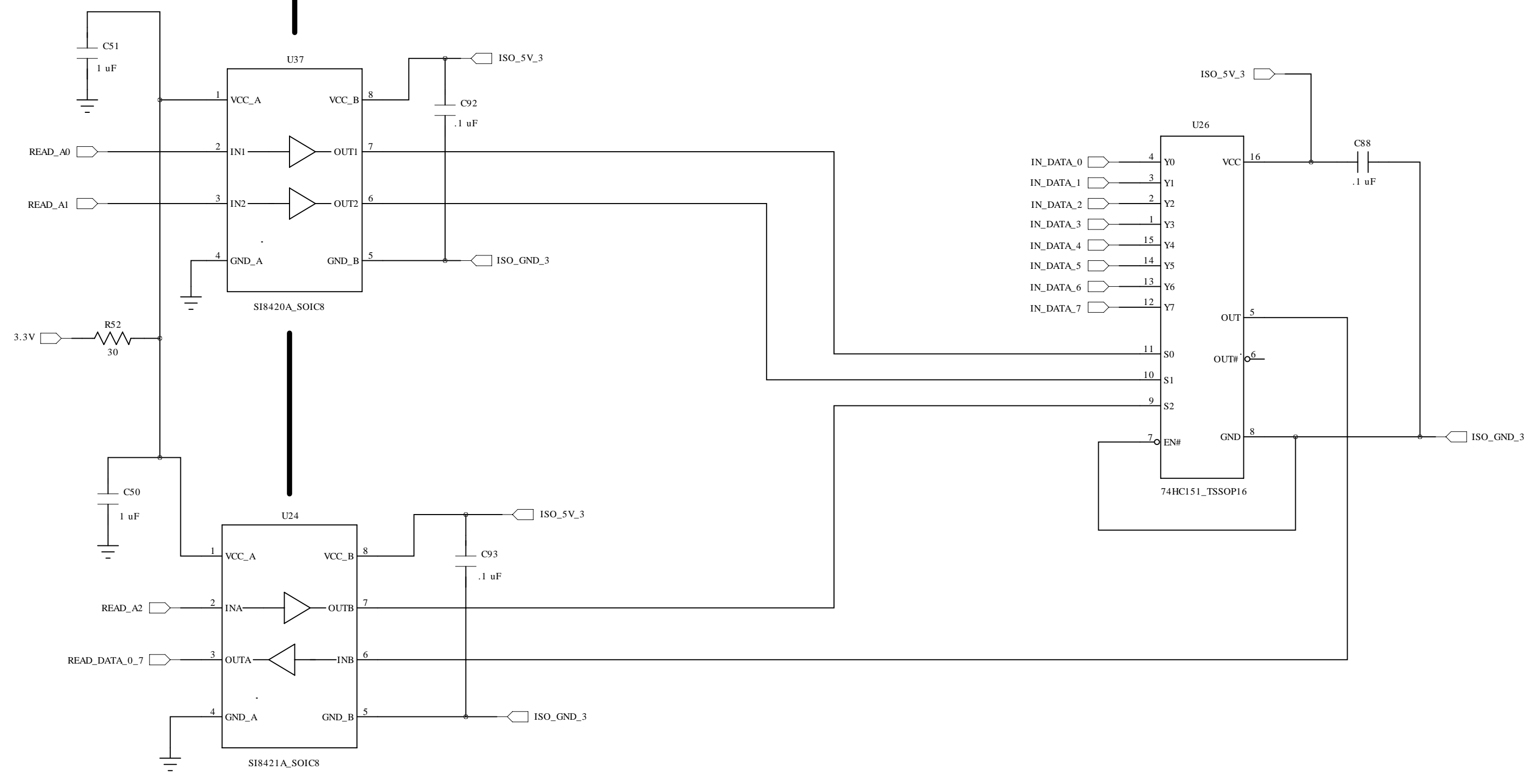
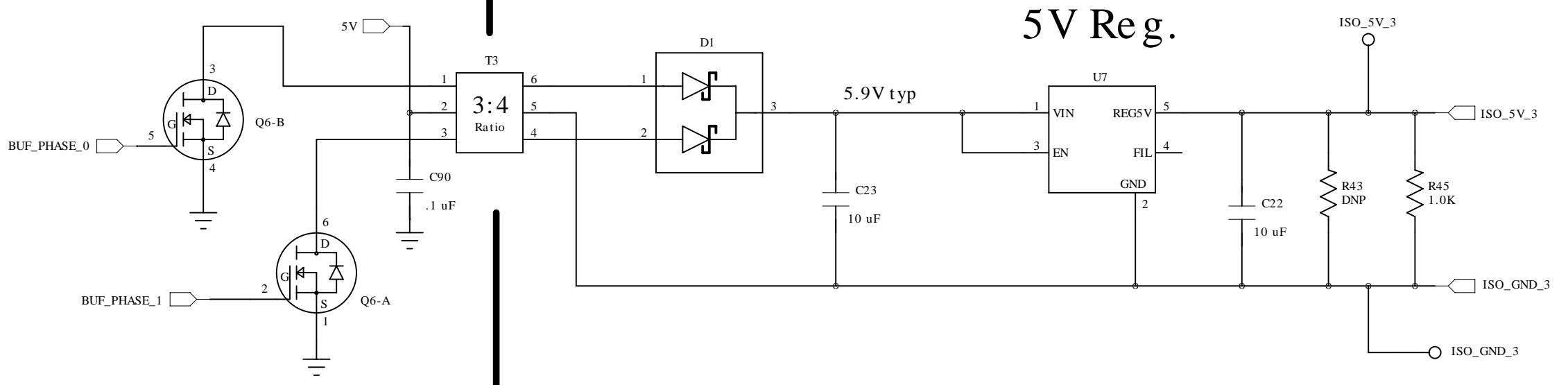


Phase_0# and Phase_1# must be non-overlapping active high
 51% low; 49% high duty cycle
 and nominal 250 KHz
 40 ns both off (low) at edges

Isolated Power

Read MUX

Read Data 0-7

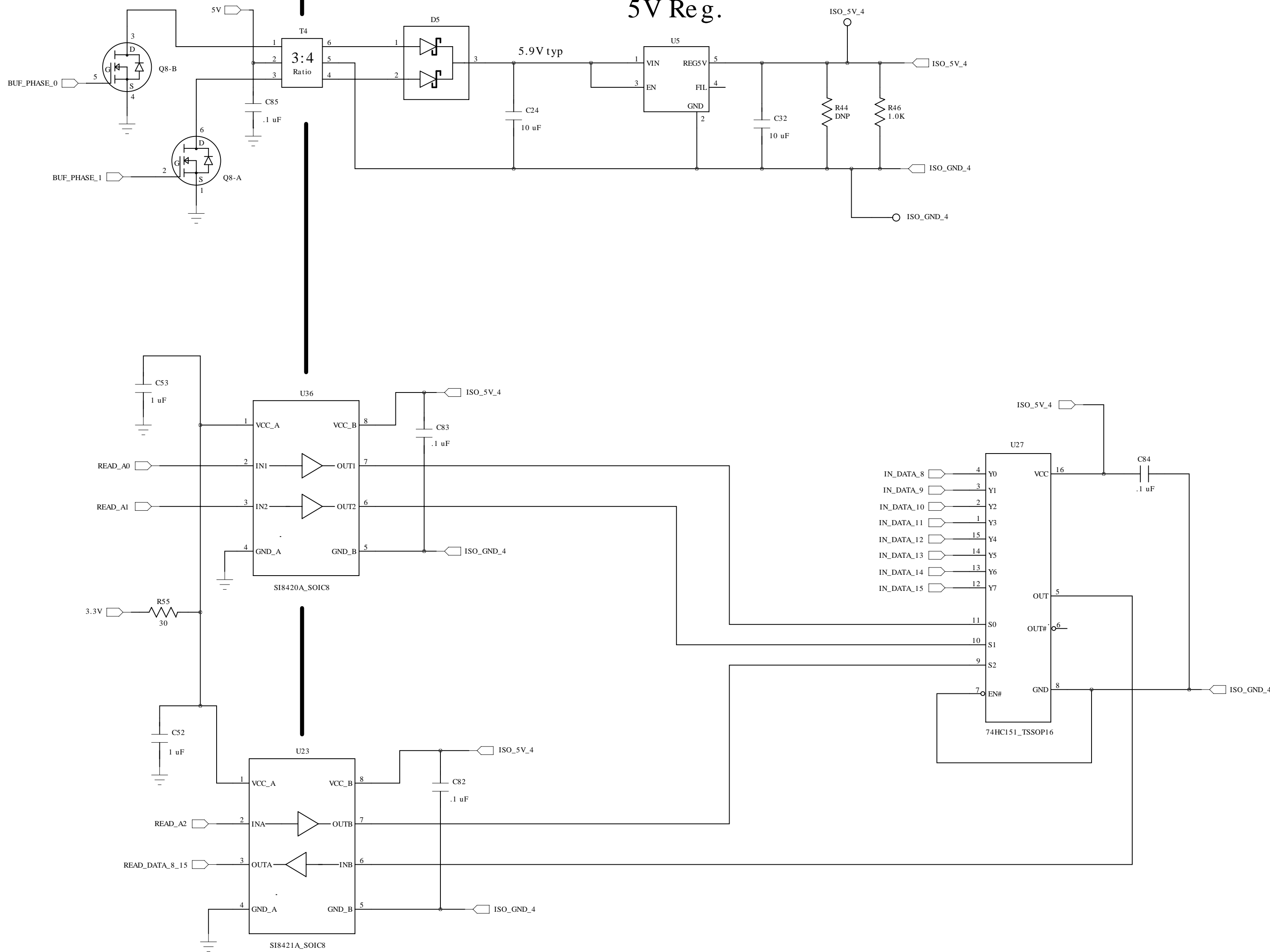


Phase_0# and Phase_1# must be non-overlapping active high 51% low; 49% high duty cycle and nominal 250 KHz 40 ns both off (low) at edges

Isolated Power

Read MUX

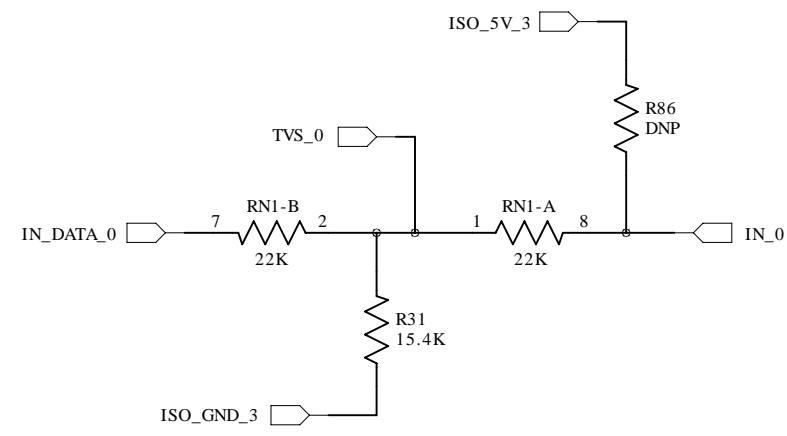
Read Data 8-15



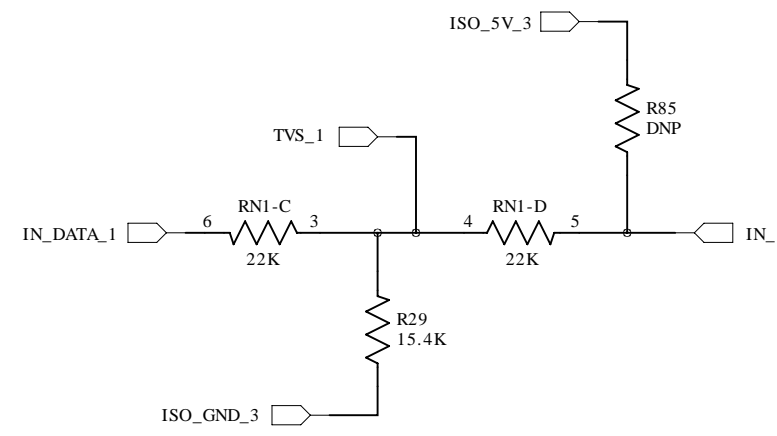
Dig. Inputs

0-30V range, 6V typ Threshold

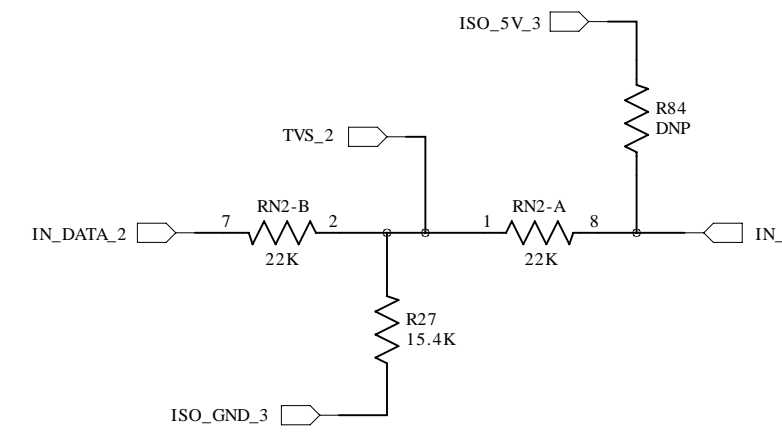
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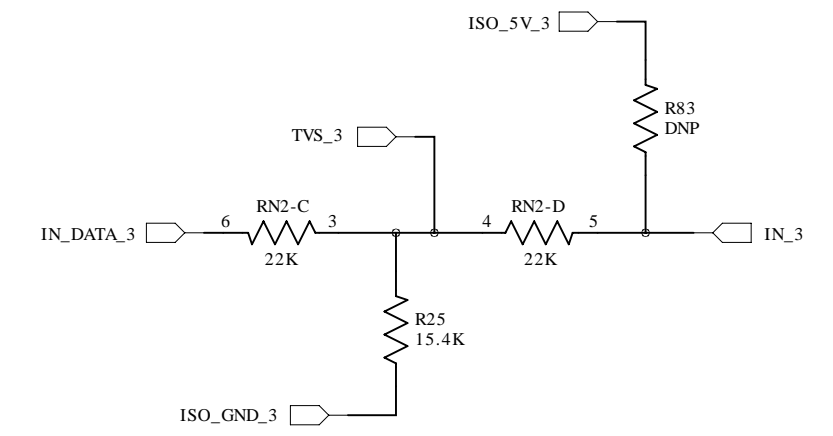
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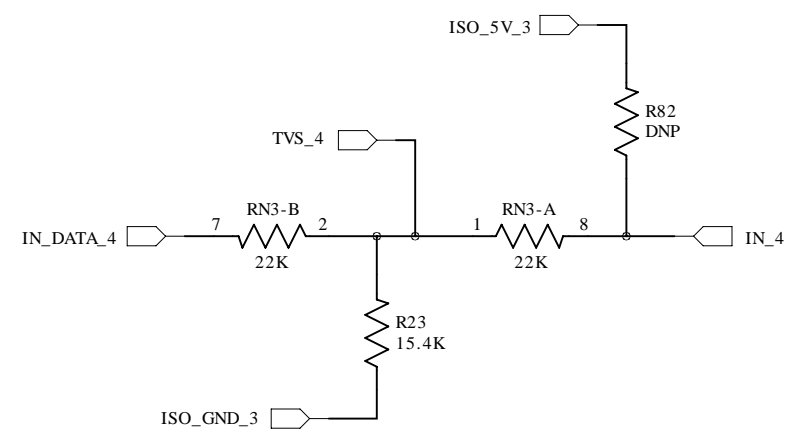
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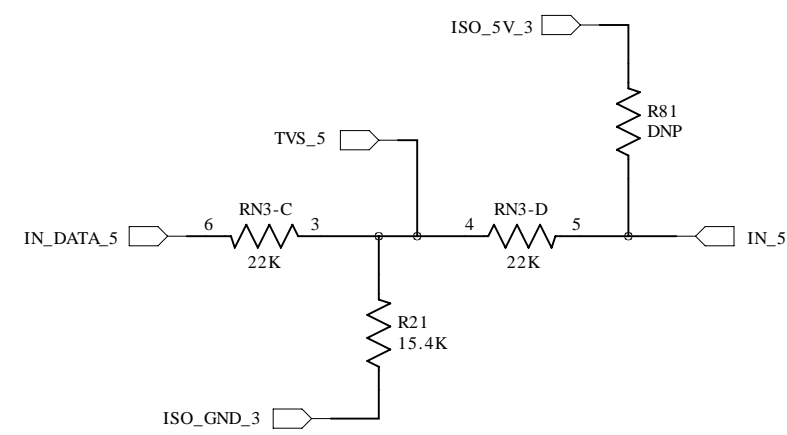
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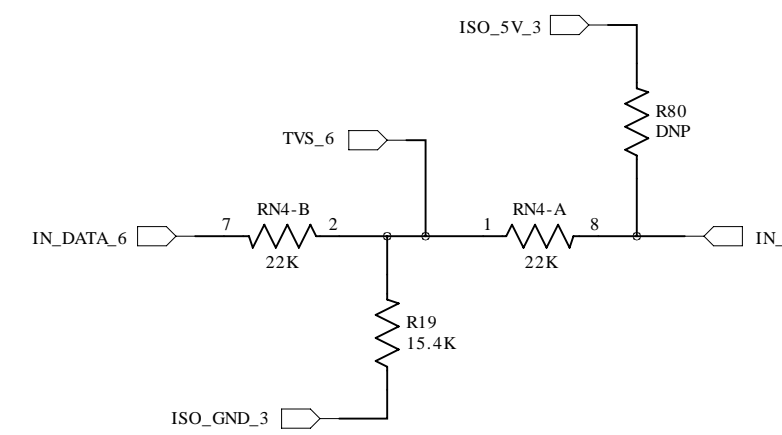
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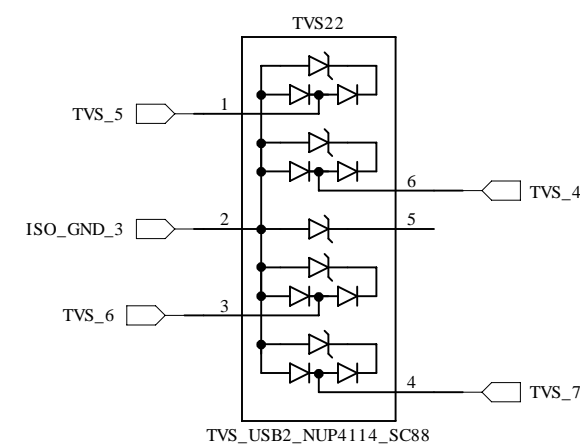
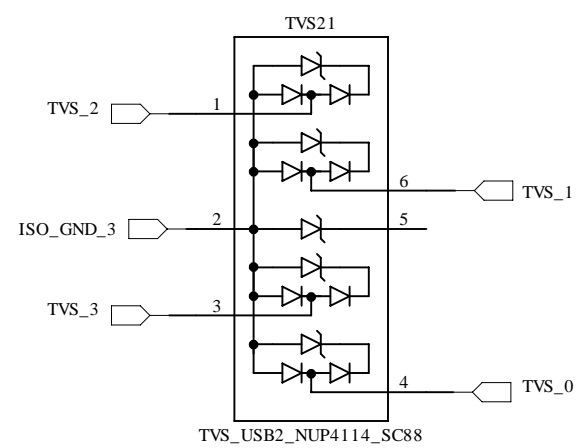
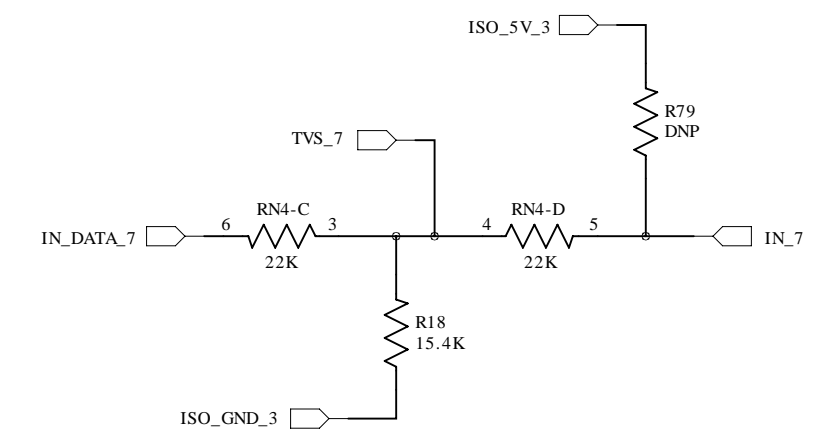
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6



7

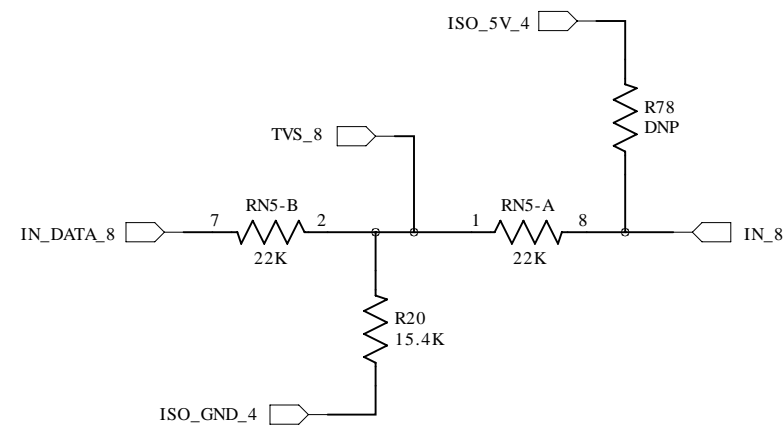


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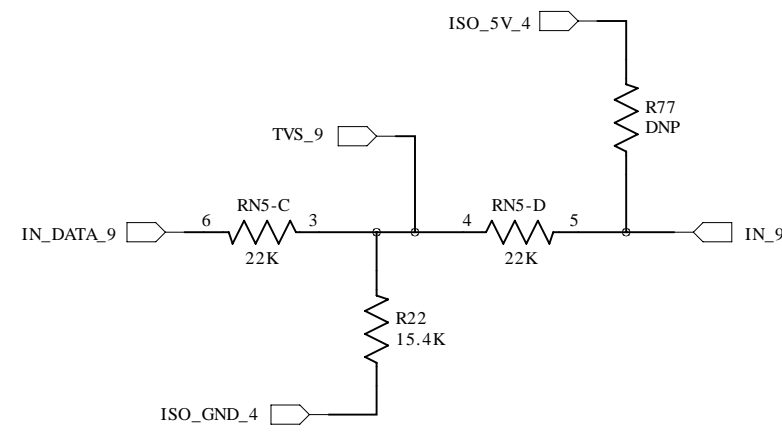
Dig. Inputs

0-30V range, 6V typ Threshold

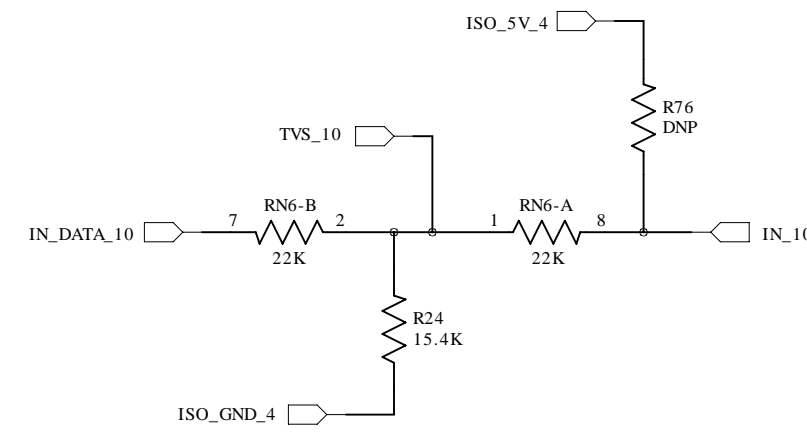
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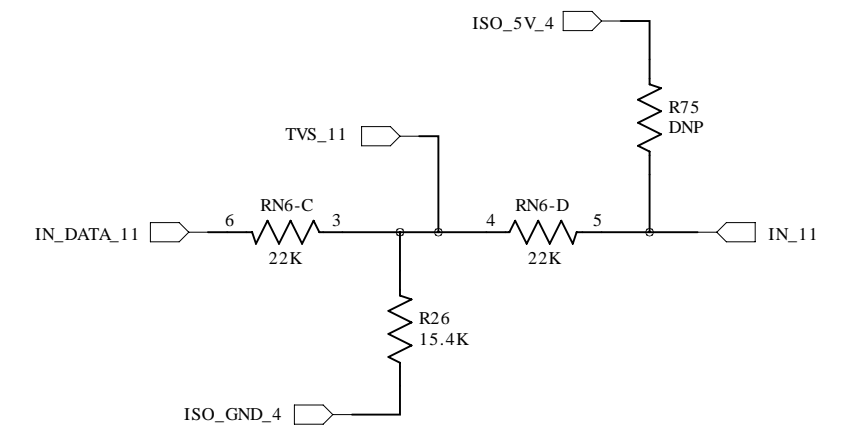
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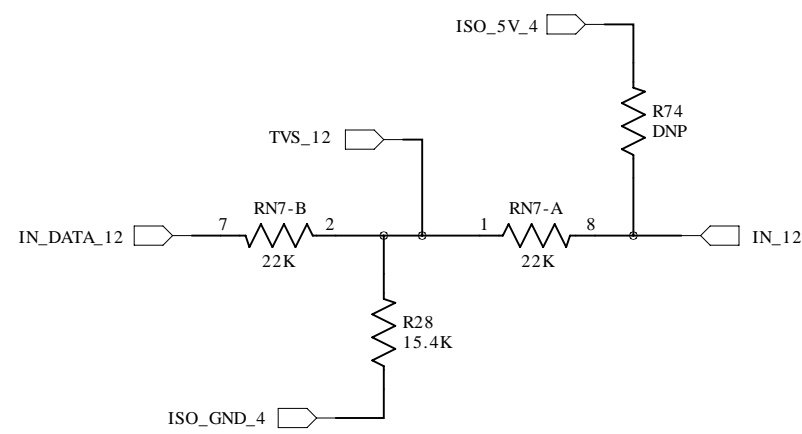
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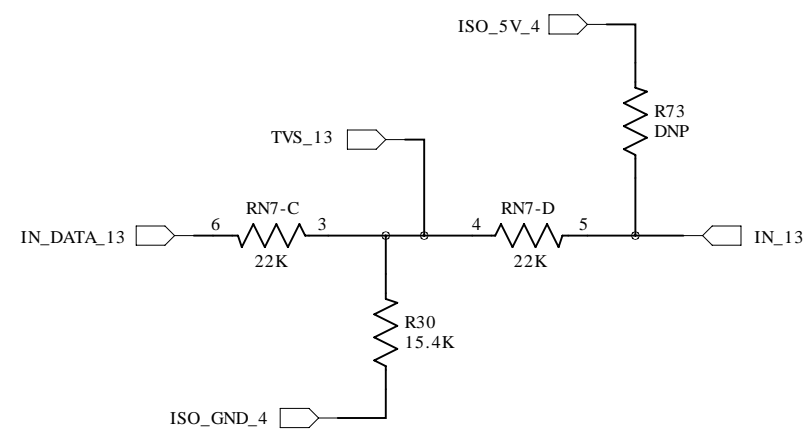
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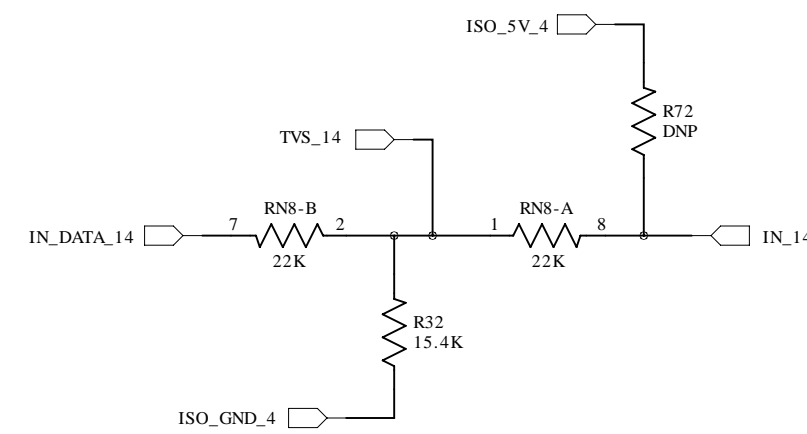
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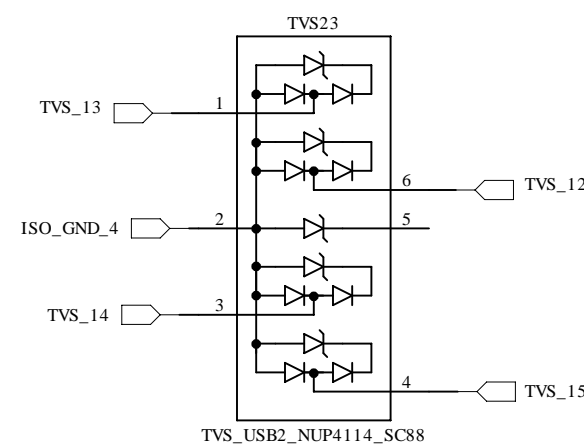
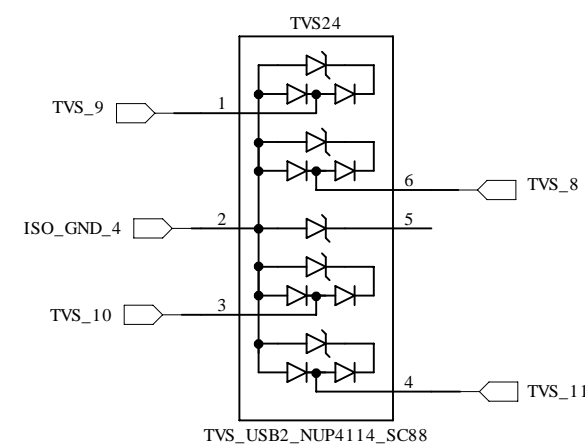
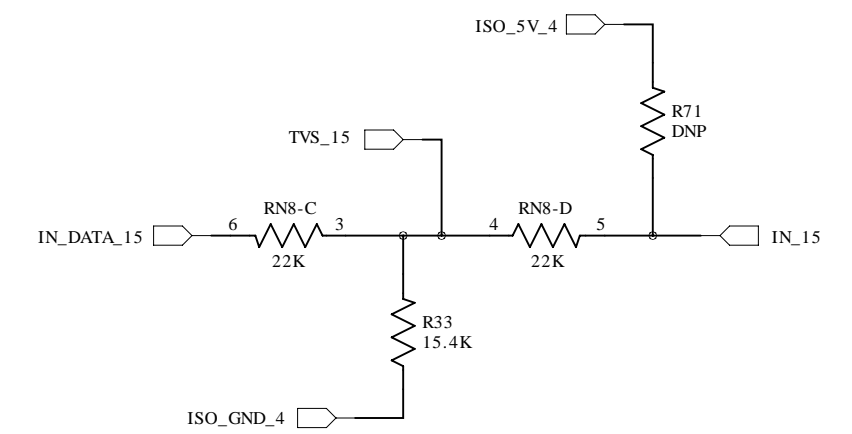
13



14



15



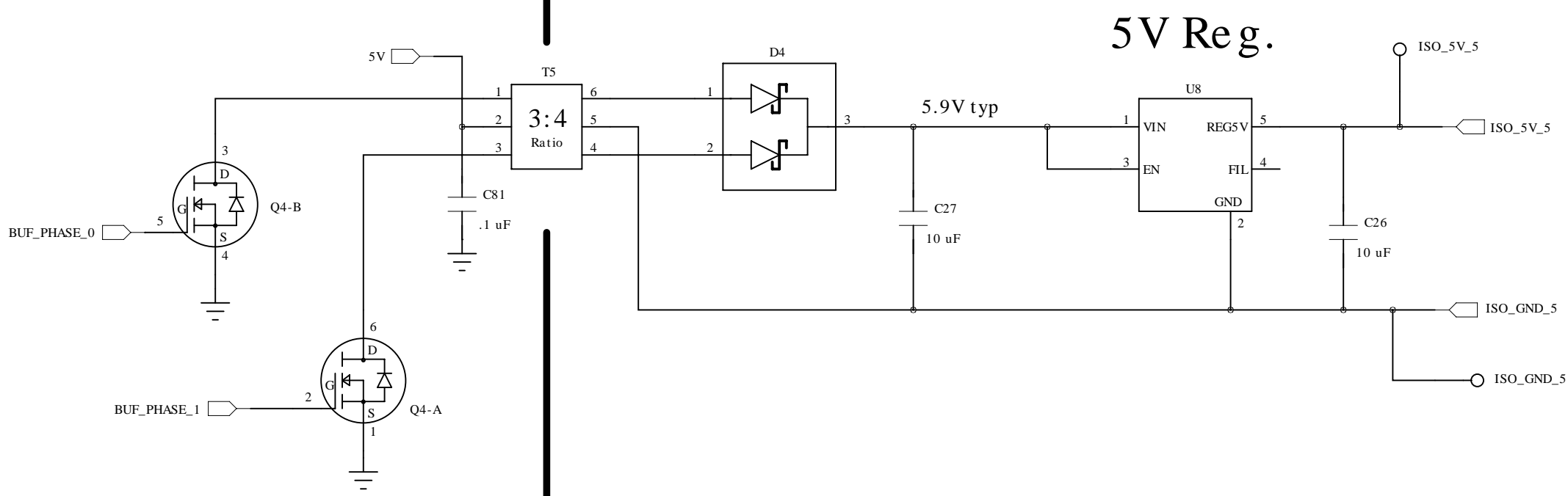
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Phase_0# and Phase_1# must be non-overlapping active high 51% low; 49% high duty cycle and nominal 250 KHz 40 ns both off (low) at edges

Isolated Power

Analog Channels 0-3

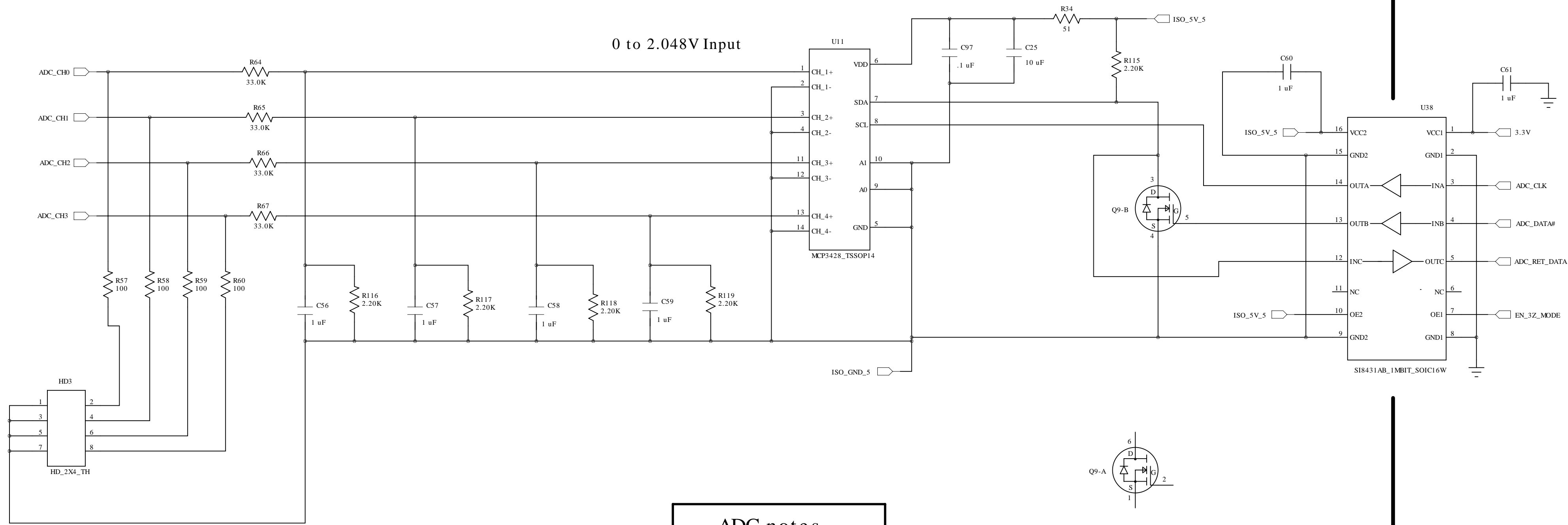
0-30V range or 4-20 mA



TS-8100 uses this ADC chip

16-bit A/D

0 to 2.048V Input



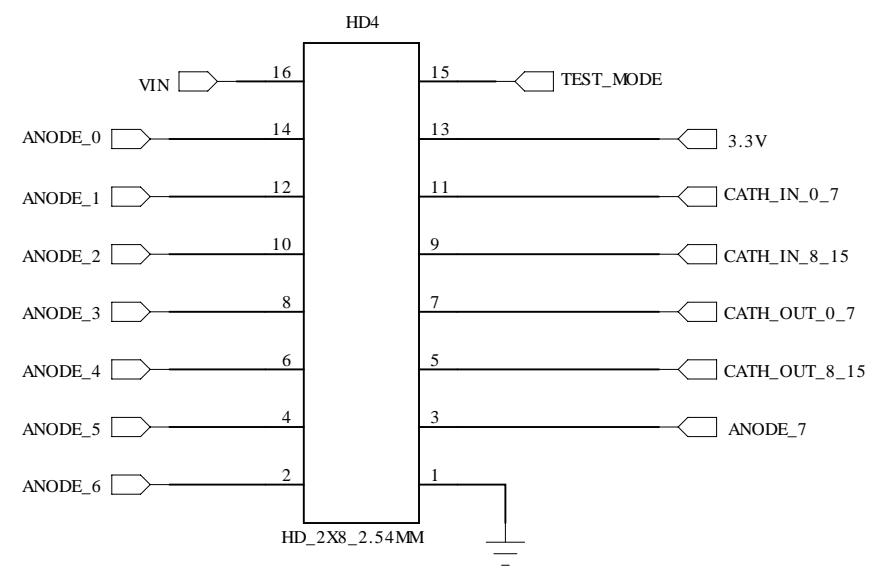
ADC notes

Input Impedance = 28 Kohm

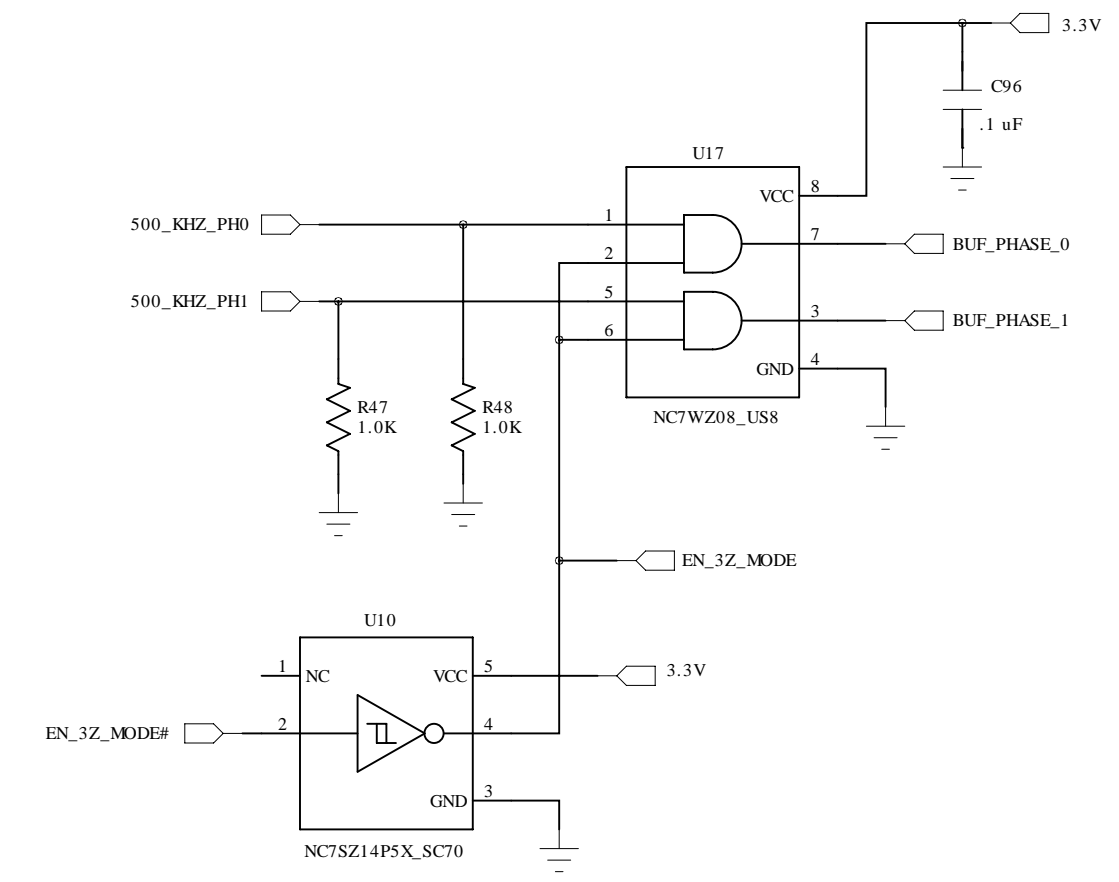
45 Hz bandwidth
4 ms Time Con.

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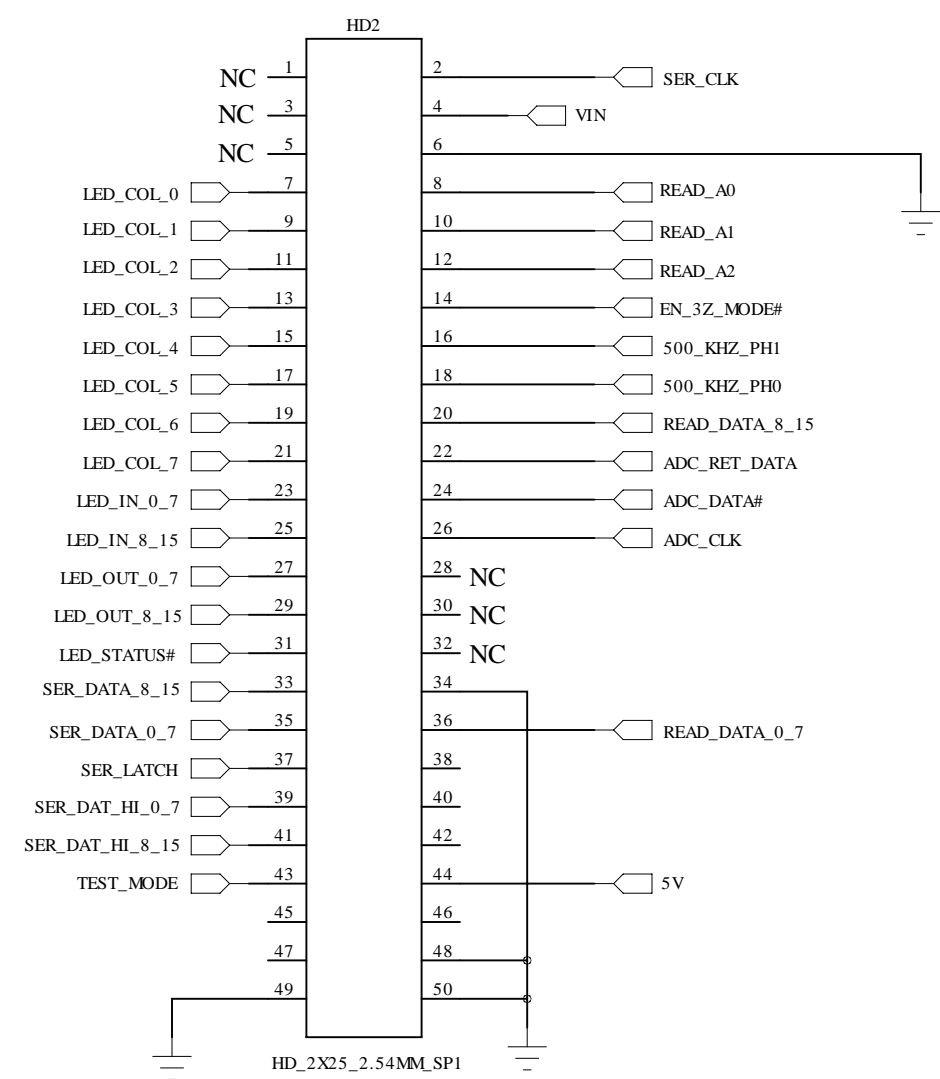
LED Header



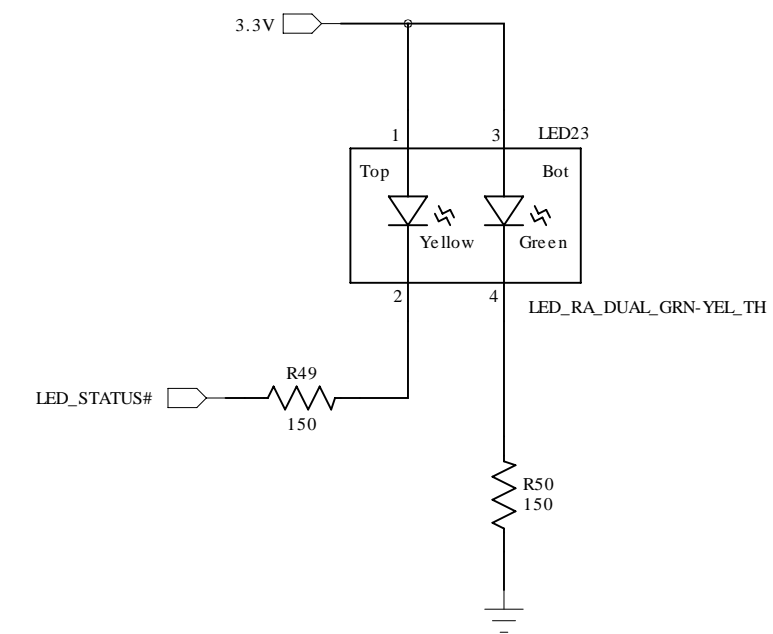
500 KHz Buffer



PC/104 Bus Connector

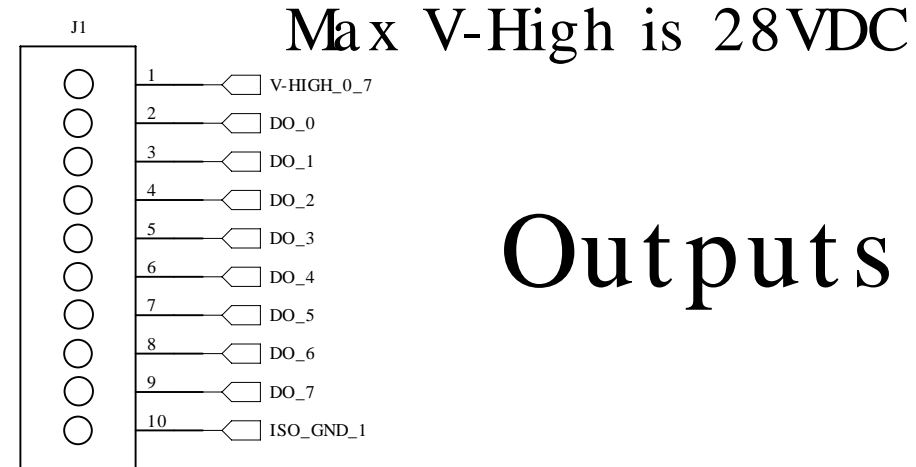


Status - Power



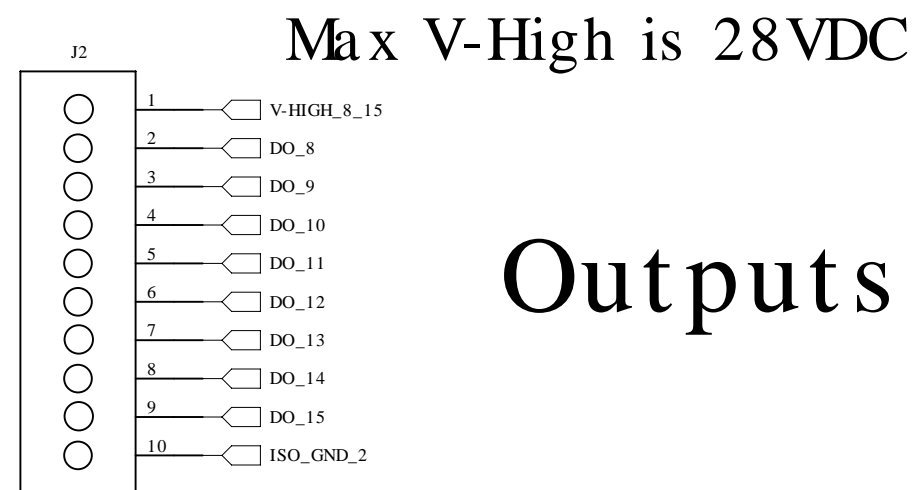
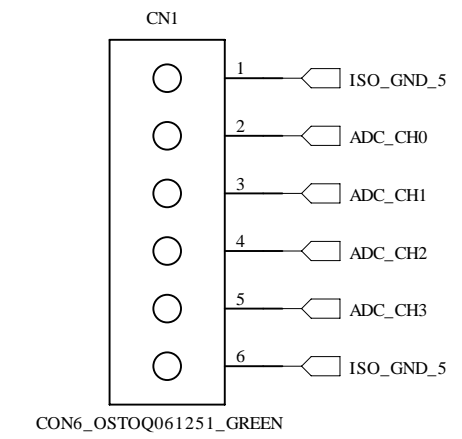
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4 x 10 and 1 x 6 Screw Term. Connectors

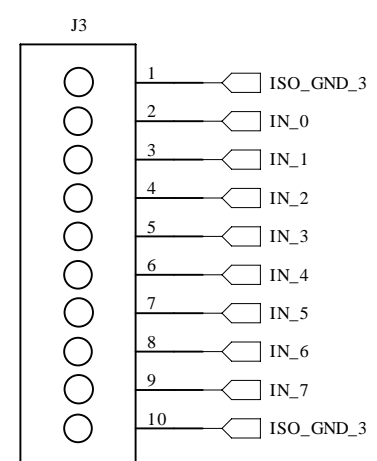


Outputs 0-7

Analog 0-3

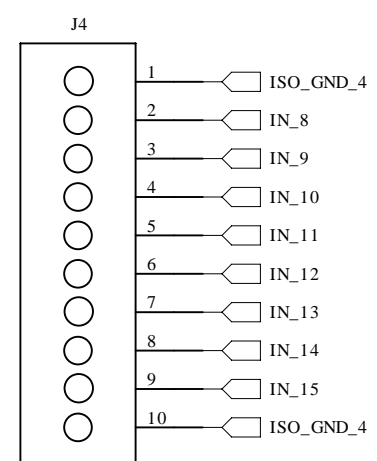
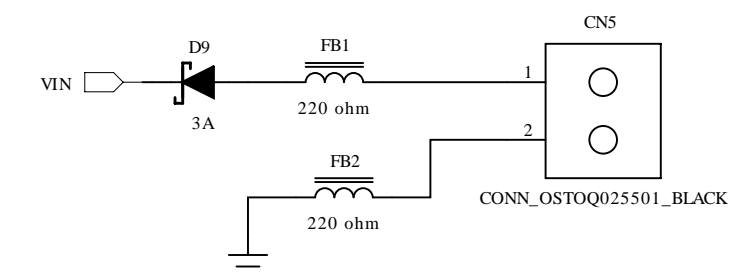


Outputs 8-15

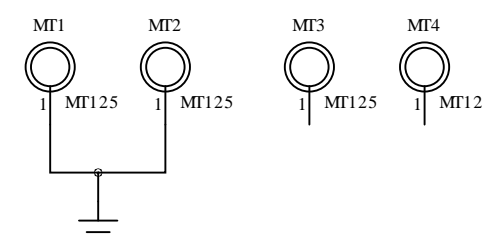


Inputs 0-7

8-28 VDC
Power Input



Inputs 8-15



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