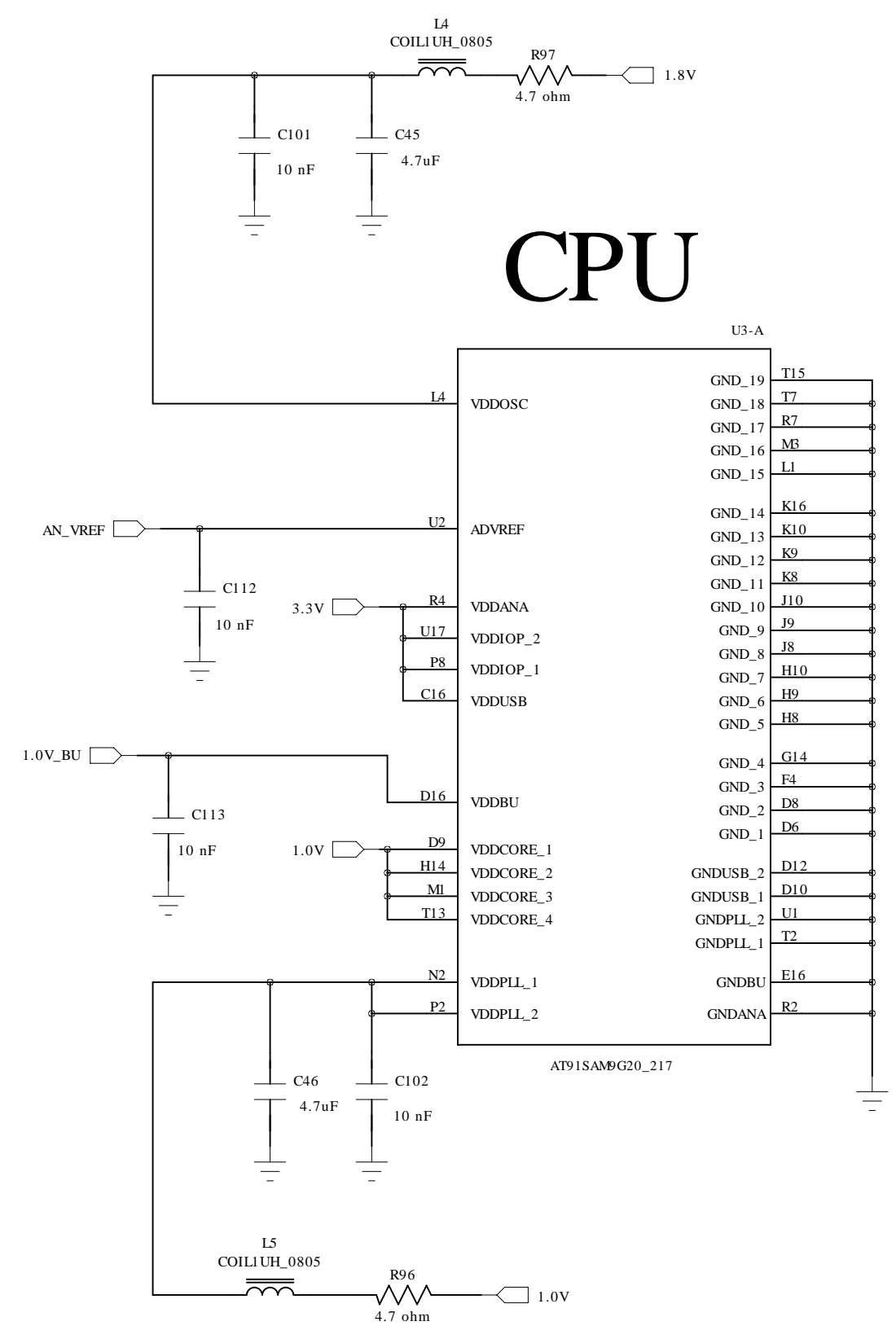
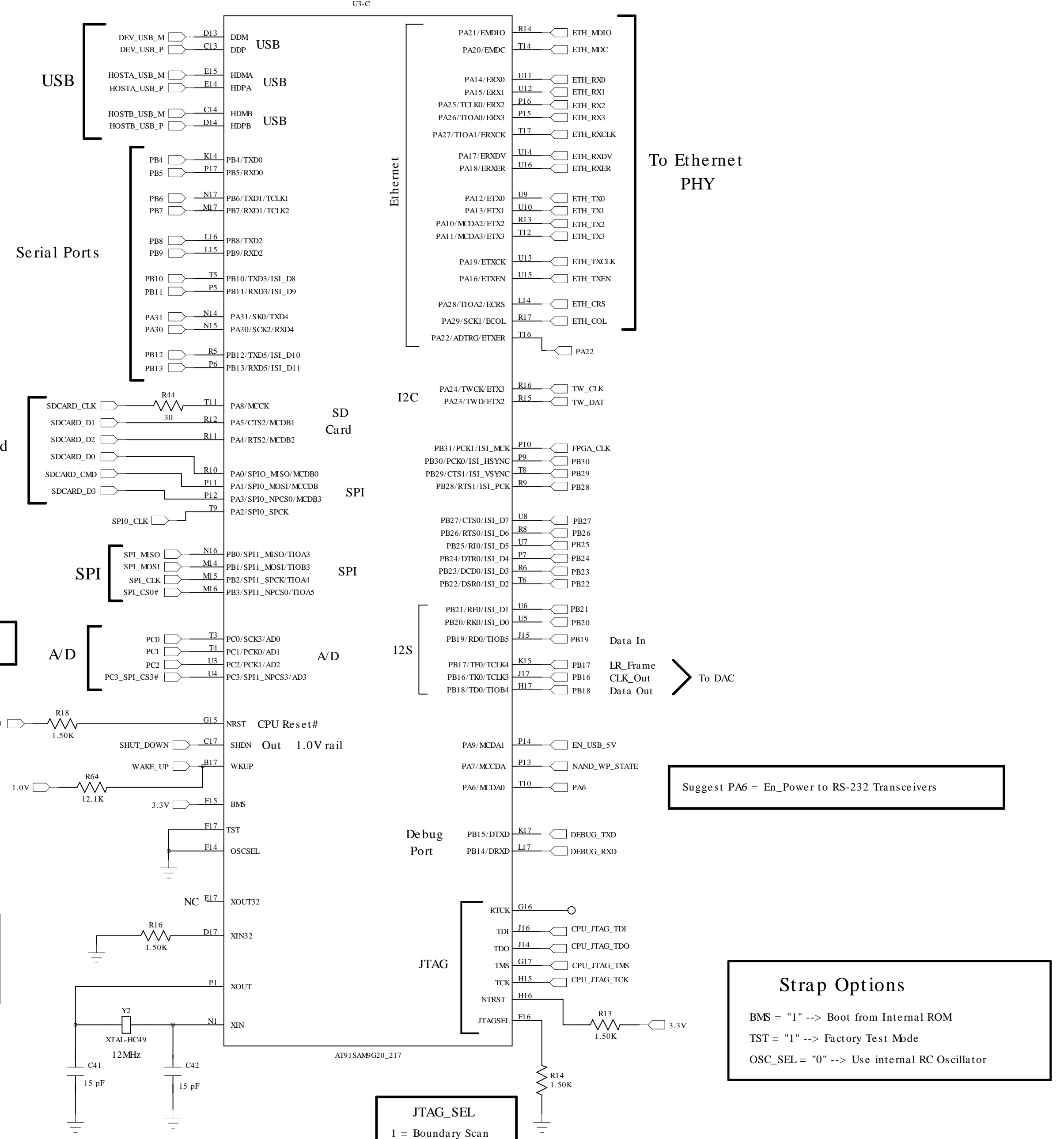


CPU



CPU



Ref. Design uses PC1 as clock to DAC

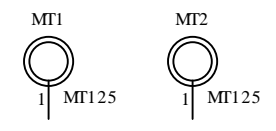
CPU_RESET# is bi-directional and can be programmed to cause interrupt instead of reset

WAKE_UP Ref. Design has 100K PU to 1.0V and sw. to GND

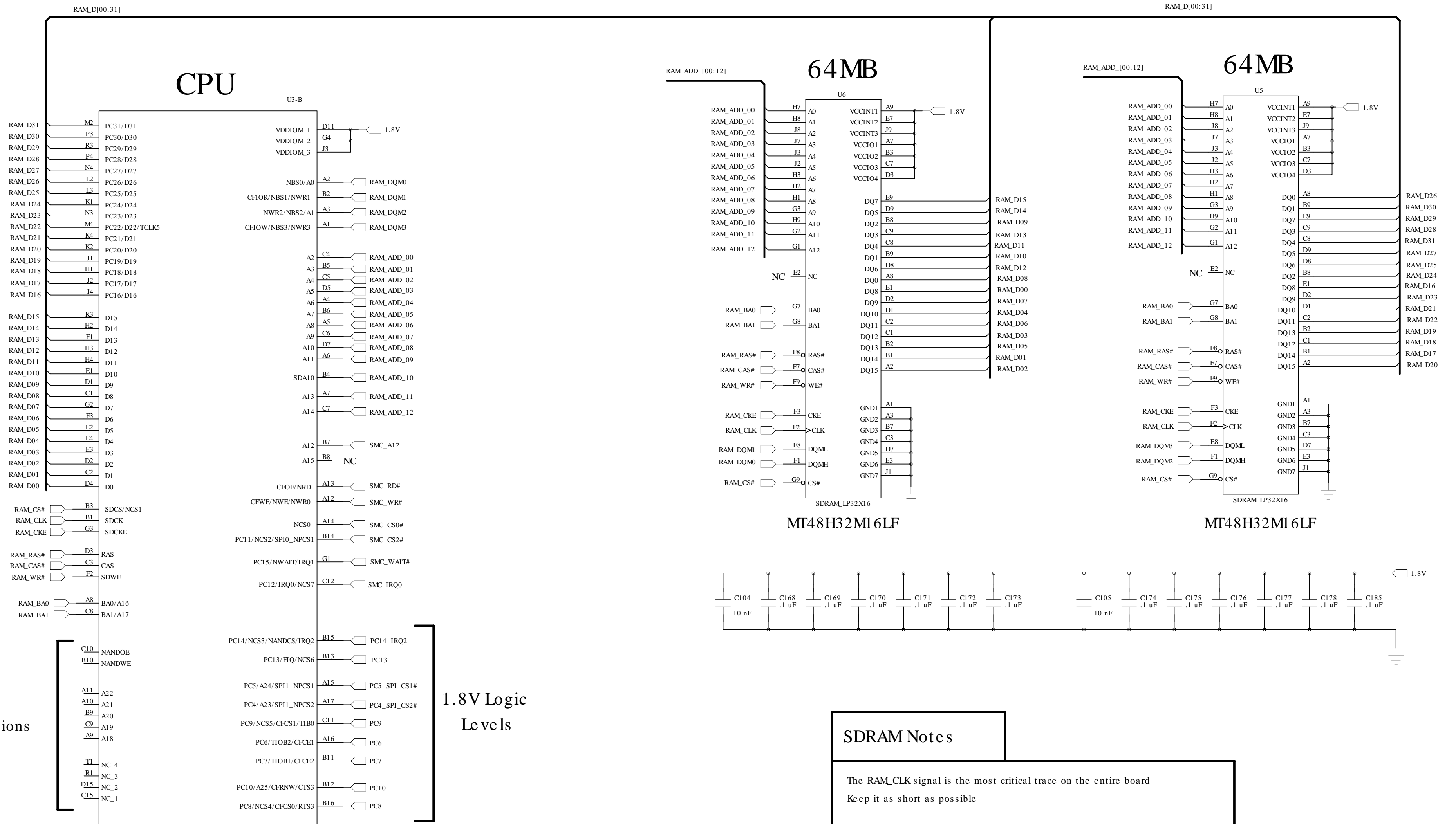
JTAG_SEL
1 = Boundary Scan
0 = CPU ICE mode

Suggest PA6 = En_Power to RS-232 Transceivers

Strap Options
BMS = "1" --> Boot from Internal ROM
TST = "1" --> Factory Test Mode
OSC_SEL = "0" --> Use internal RC Oscillator



128 MB RAM



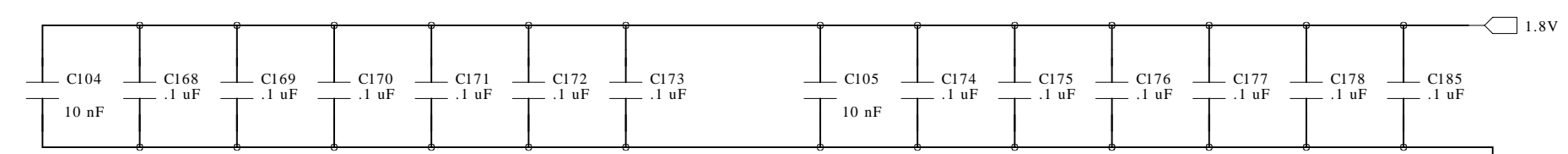
No Connections

Logic Levels in this "Gate" are all 0 to 1.8V

1.8V Logic Levels

SDRAM Notes

- The RAM_CLK signal is the most critical trace on the entire board. Keep it as short as possible.
- All other RAM signals, should be kept as short as feasible. Some RAM signals go to the FPGA also - this is a complication.
- RAM data signals can be swapped bit-wise or byte-wise. For example, D16-D23 can be swapped with D24-D31. This would require the respective DQMx lines to be swapped as well.
- Bit-wise swaps are allowed within a byte. For example, D2 and D5 can be swapped.



FPGA

A3P125 has:
 3000 Tiles (about 1200 LUTs)
 4 Kbytes total of Block RAM
 97 I/O with 144 pin package
 "true instant ON"
 Input PLL clock = 1.5 MHz min

Warning: MUX_AD00 thru AD07 is used by NAND Flash

Devices connected to this bus must never drive it when BUS_RD# is deasserted (must be off within 30 nS of deassertion)

Devices must pull the BUS_WAIT# line low if they need more than 150 nS strobe

FPGA_CLK = CPU Timer Out

DIO_09 = Push_switch

All NVRAM interface signals must be kept in low state when not accessing NVRAM

RED_LED# and GREEN_LED# must be Open Drain

When SYSTEM_RESET# asserted, then set these as follows:

Asserted:
 OFF_BD_RST#
 EN_SDCARD_PWR#
 RED_LED#
 GREEN_LED#

Deasserted:
 EN_ETH_PWR#
 REBOOT
 NVRAM_CS
 NAND_CS#

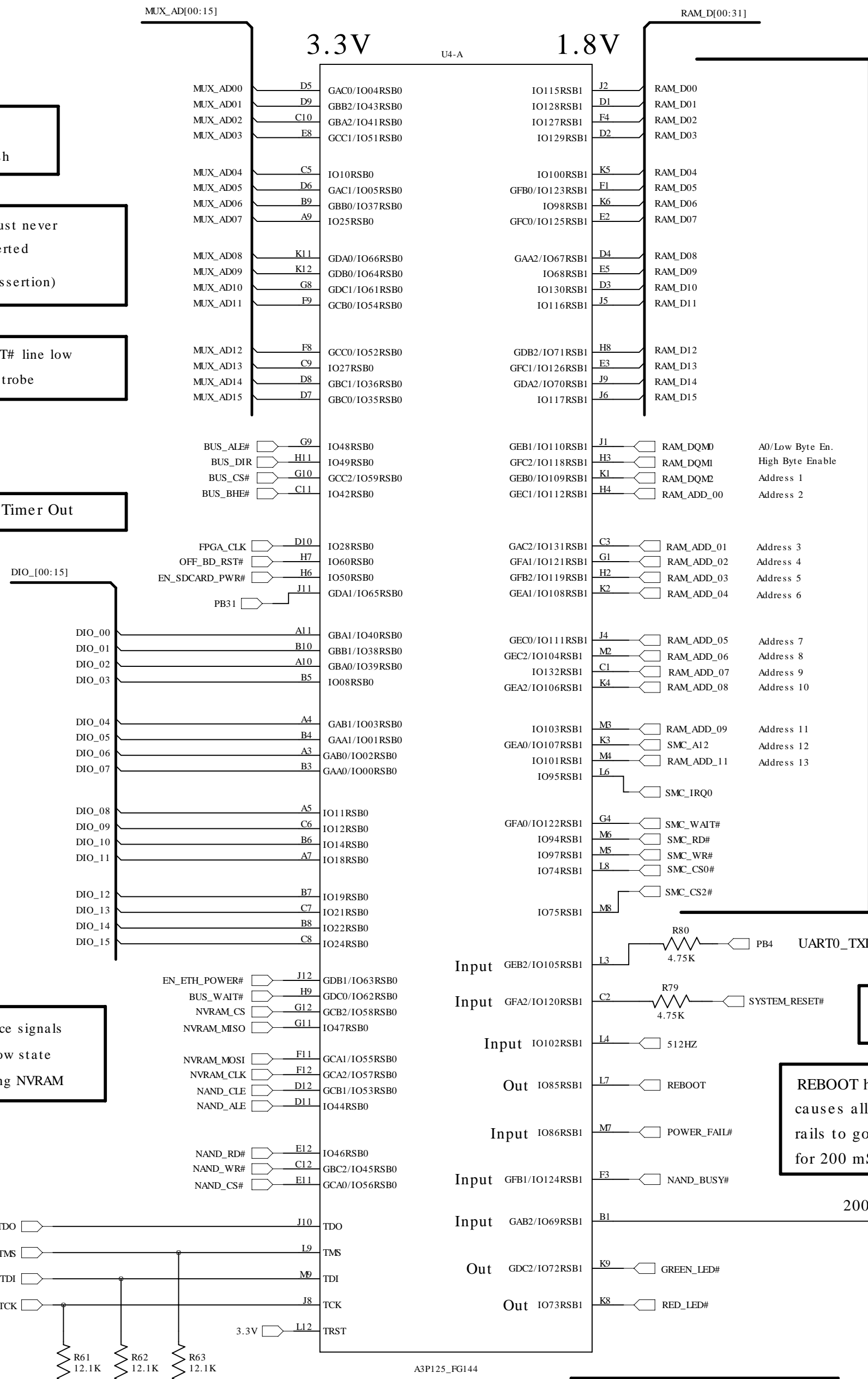
When SYSTEM_RESET# deasserted, Latch BUS_ALE# and BUS_RD# into a register

Early Boot code should deassert OFF_BD_RST# signal. (after SPI Flash loaded into RAM)

Boot Straps

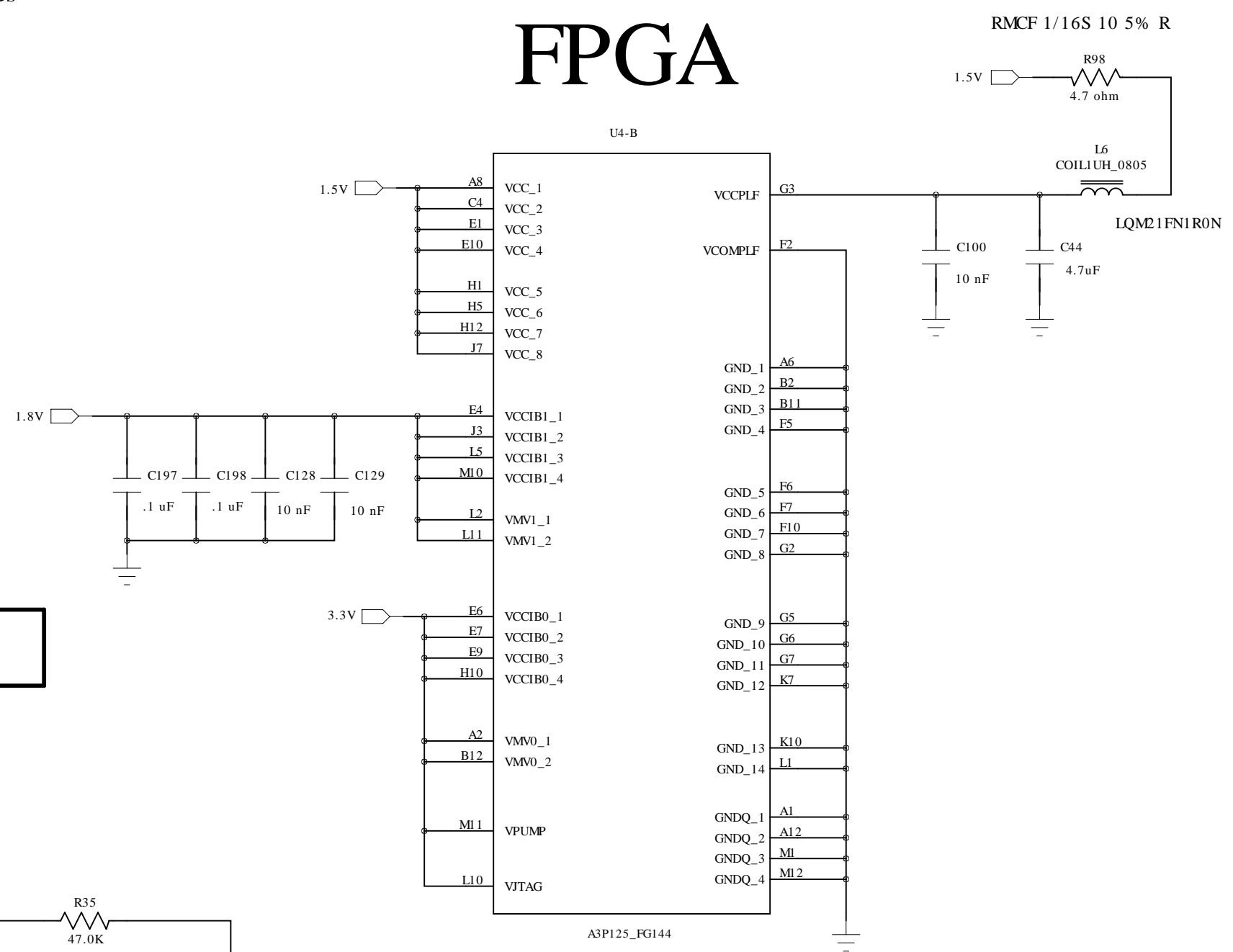
Mode 2	Boots from
1	NAND Flash
0	SD Card

BUS_ALE# = MODE1
 BUS_RD# = MODE2



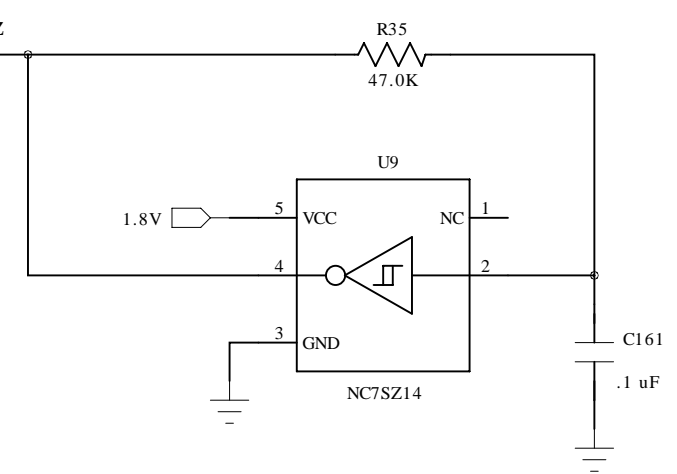
To CPU
 Address/Data Bus

FPGA

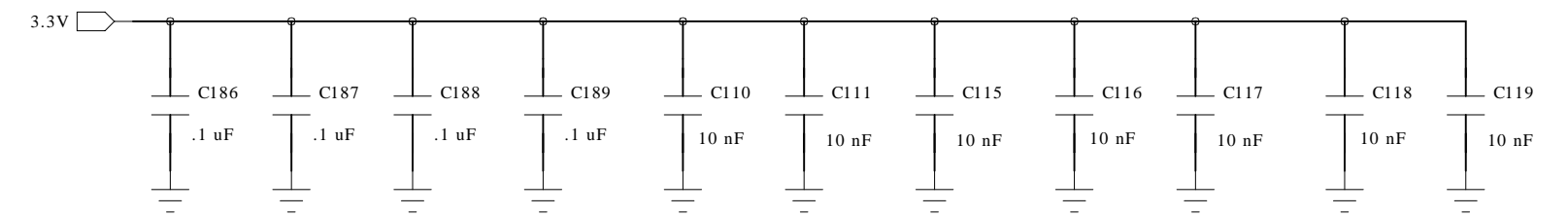
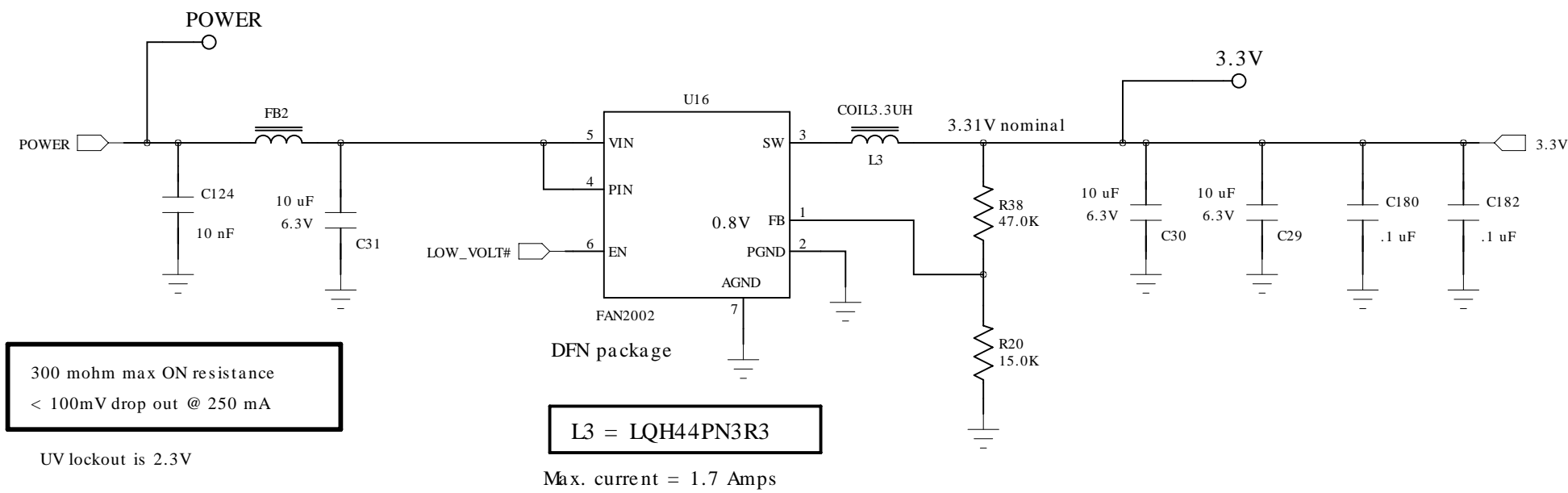


Inputs with 1.8V rail have diode clamp to 1.8V

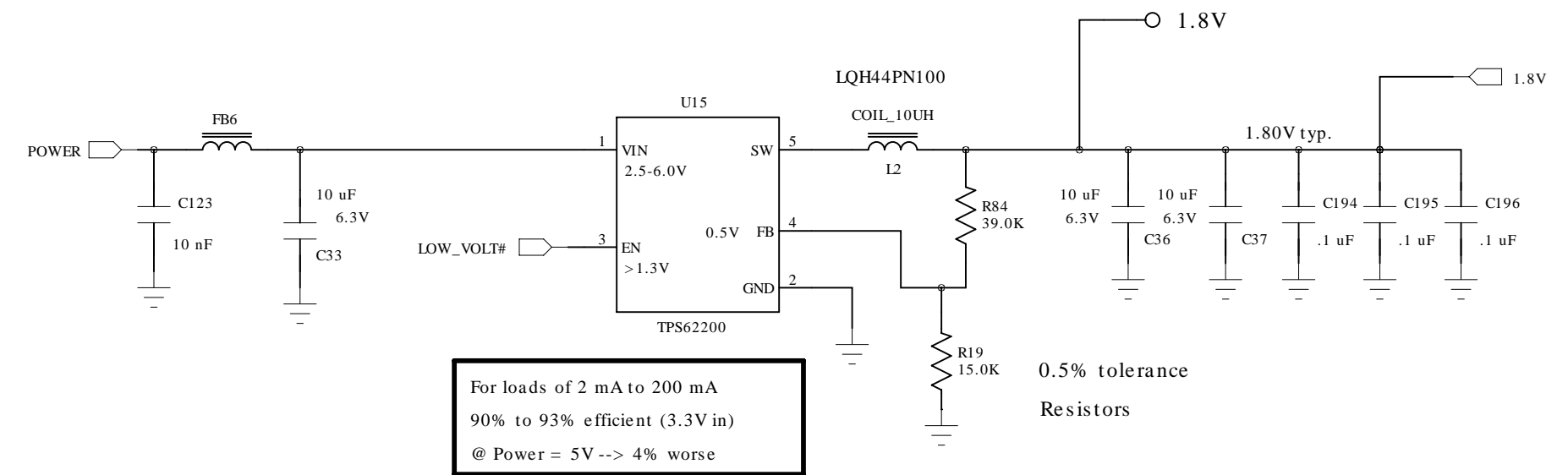
REBOOT high causes all power rails to go low for 200 mS



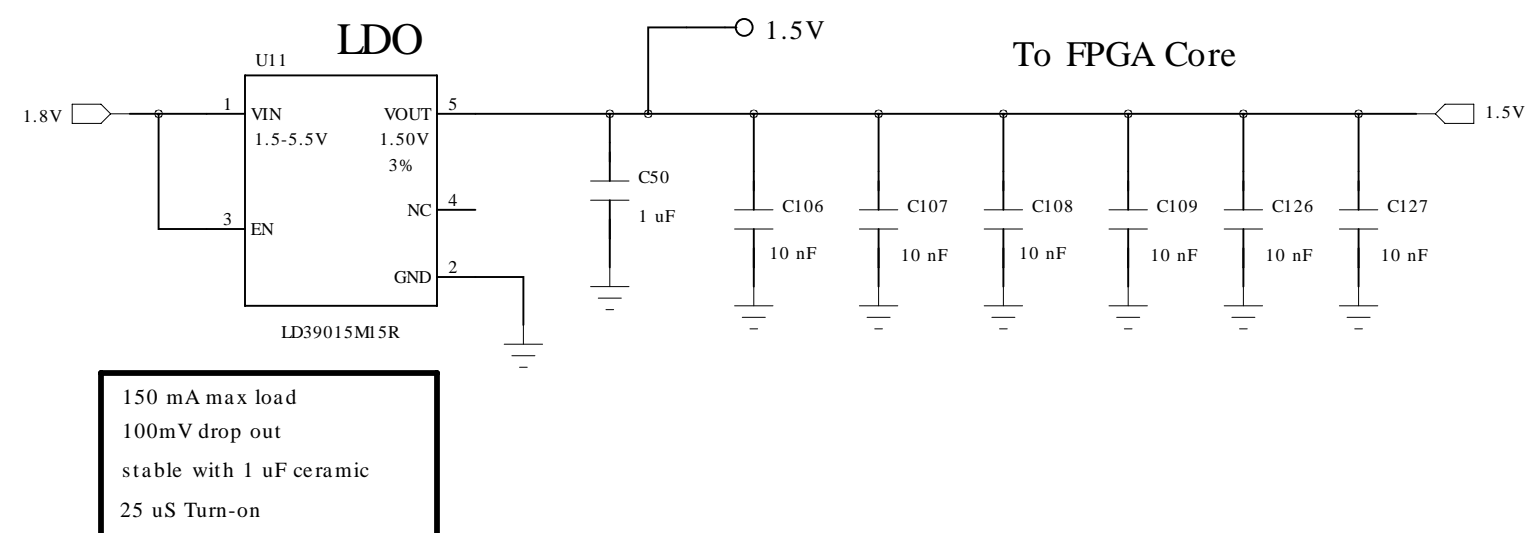
3.3V Supply



1.8V Supply



1.5V Supply



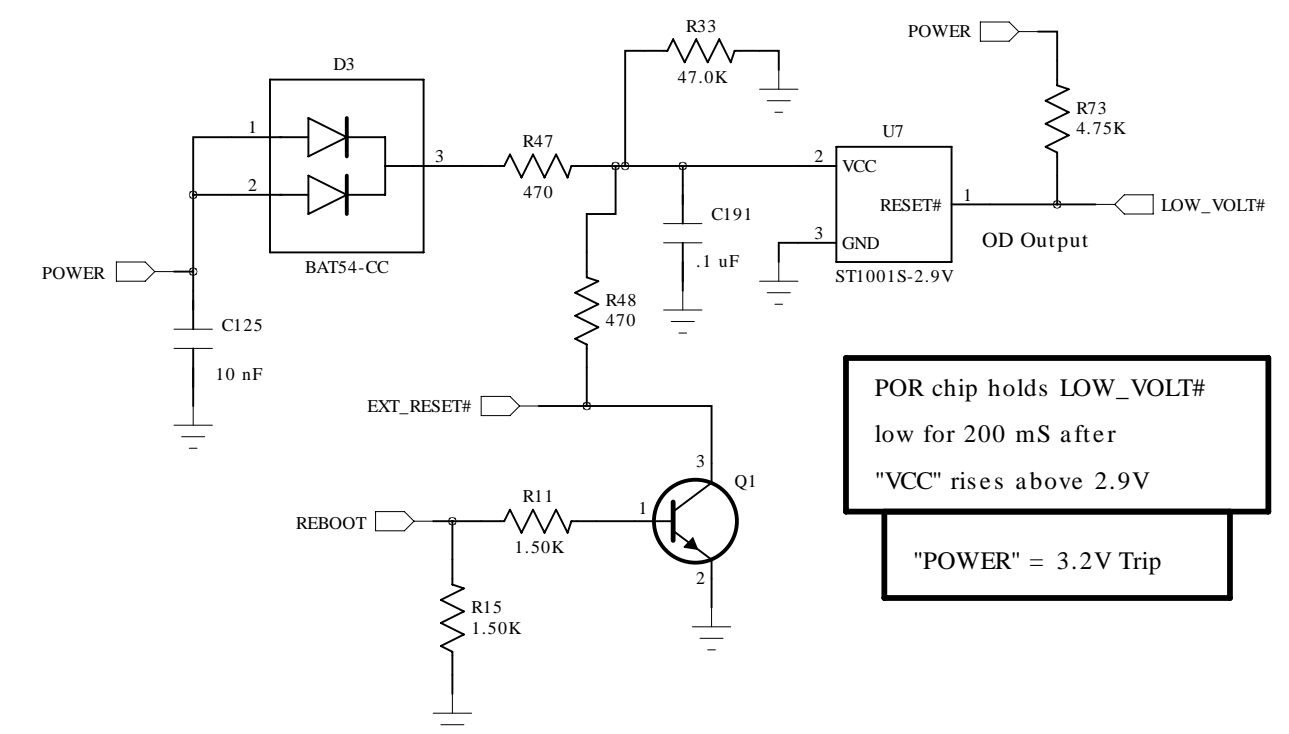
Power Sequence

After power is first applied, or after a "Reboot"
All power rails are off for 200 mS then:

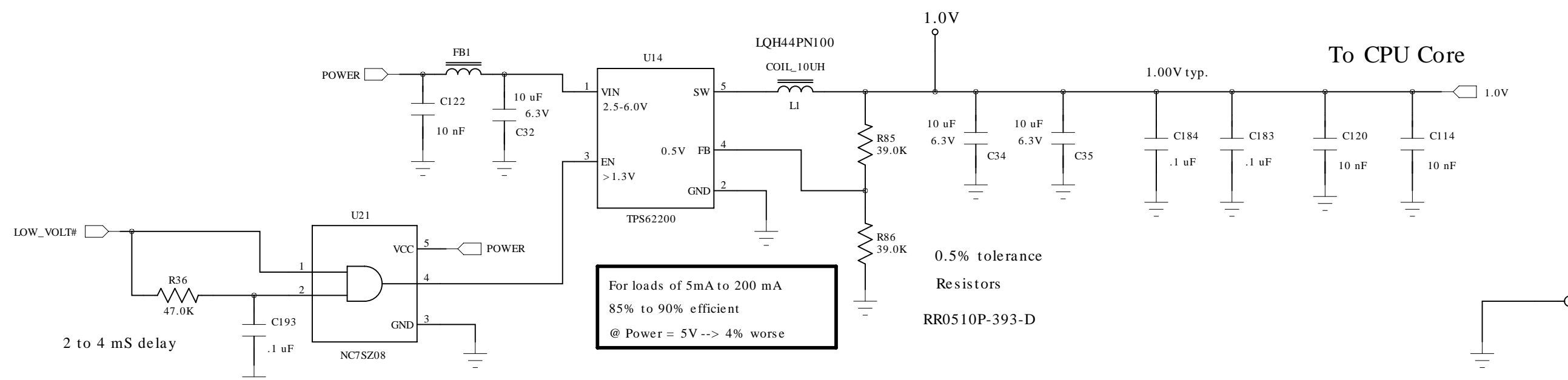
- the 3.3V and 1.8V are enabled
these will reach 95% in about 800 uS
(the 1.5V rail will ramp 25 uS delayed)
- Then 2-4 mS later, the 1.0V rail is enabled
It also requires about 800 uS to ramp

CPU Reset# is asserted before 1.0V rail is enabled

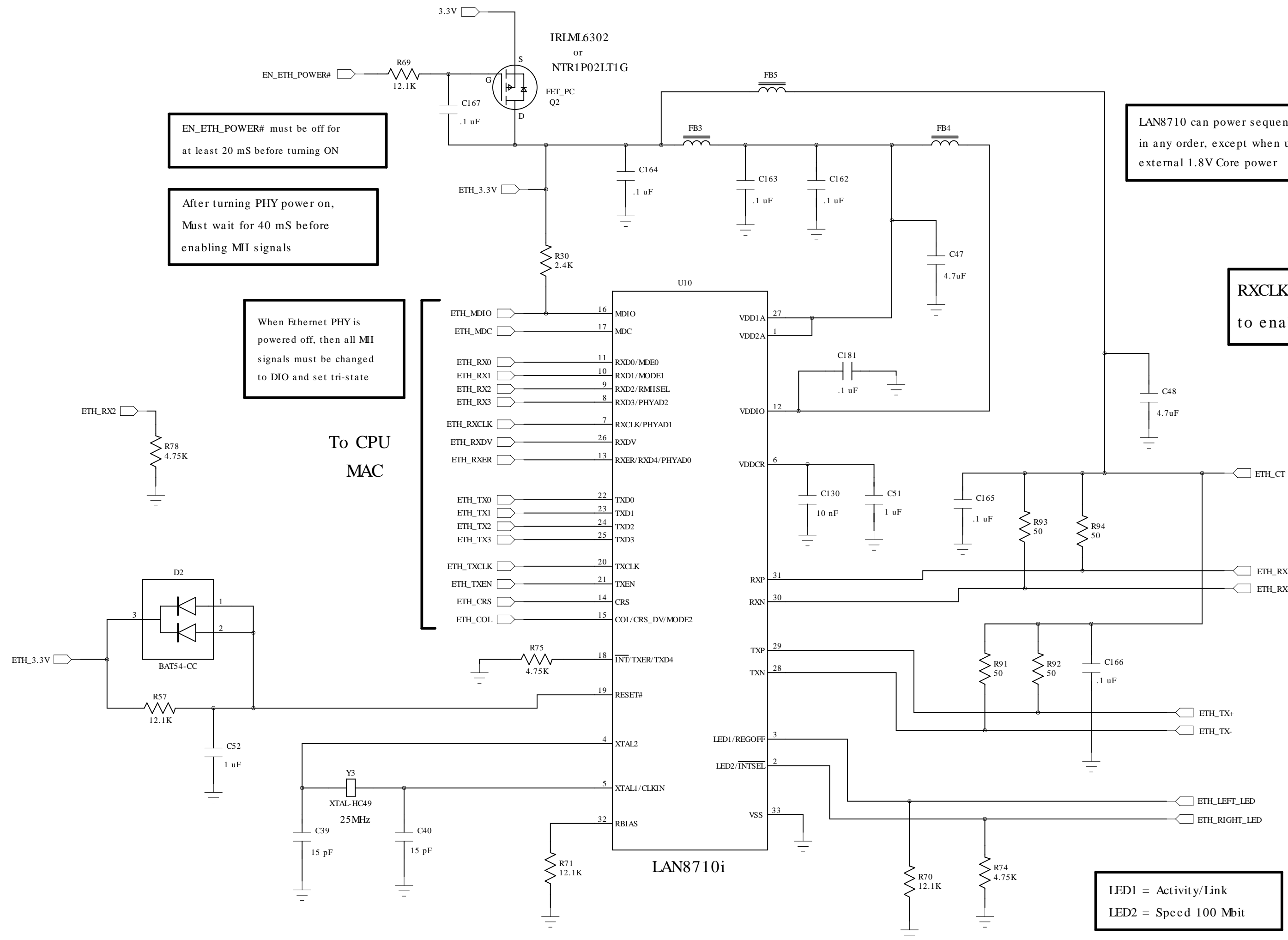
POR



1.0V Supply



10/100 Ethernet



EN_ETH_POWER# must be off for at least 20 mS before turning ON

After turning PHY power on, Must wait for 40 mS before enabling MII signals

When Ethernet PHY is powered off, then all MII signals must be changed to DIO and set tri-state

LAN8710 can power sequence in any order, except when using external 1.8V Core power

RXCLK must be biased low to enable internal 1.8V reg.

To CPU MAC

LED1 = Activity/Link
LED2 = Speed 100 Mbit

Resistor PD on pin 18 is not required per data sheet But Jesse could not get it to work until we added it

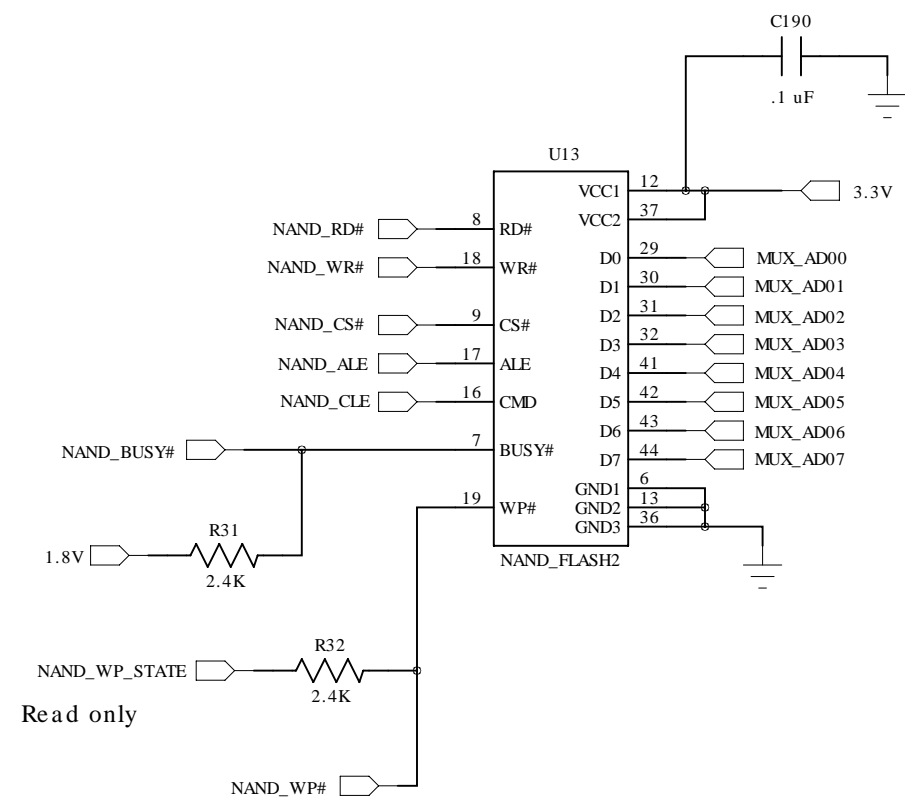
MDIO bus can not be used until 100 uS after Reset# is deasserted
MDCLK max is 2.5 MHz

PHY PU and PD resistors are 67K ohm typical

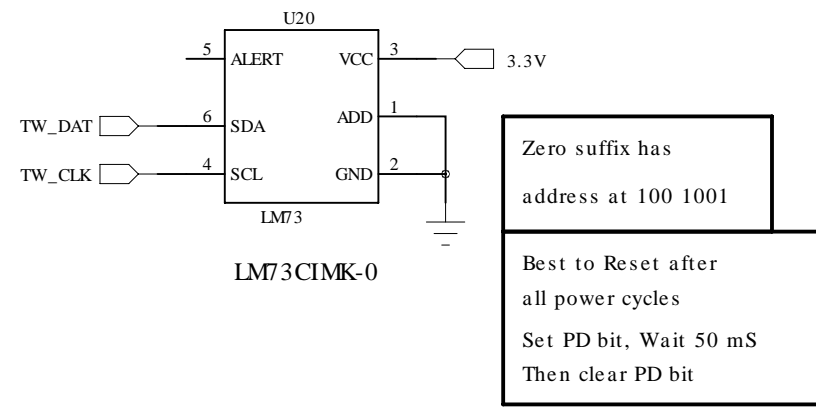
CPU PU resistors are 70K typ. and 40K min.

Beware
The PHY address is controlled by strapping pins. If CPU has PU; PHY has PD --> indeterminate

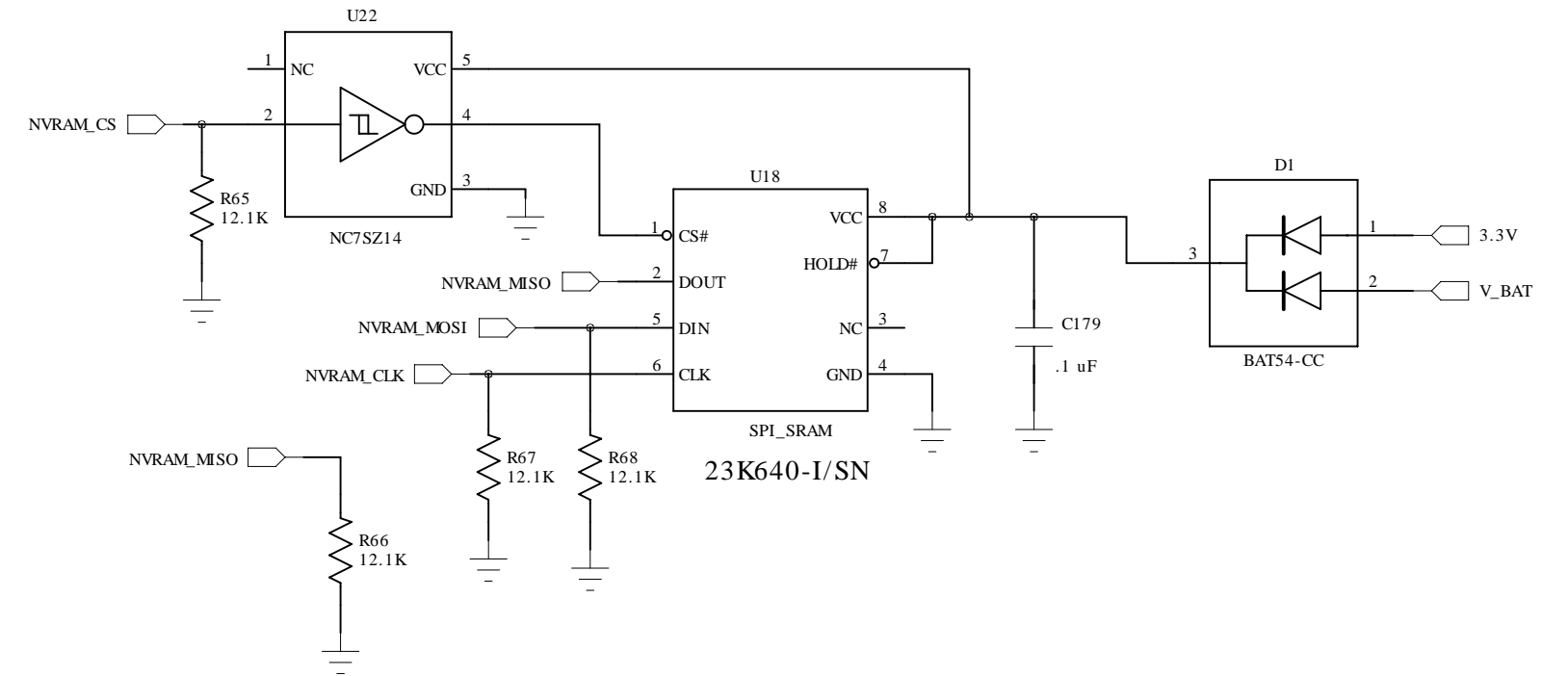
512 MB or 2 GB NAND Flash



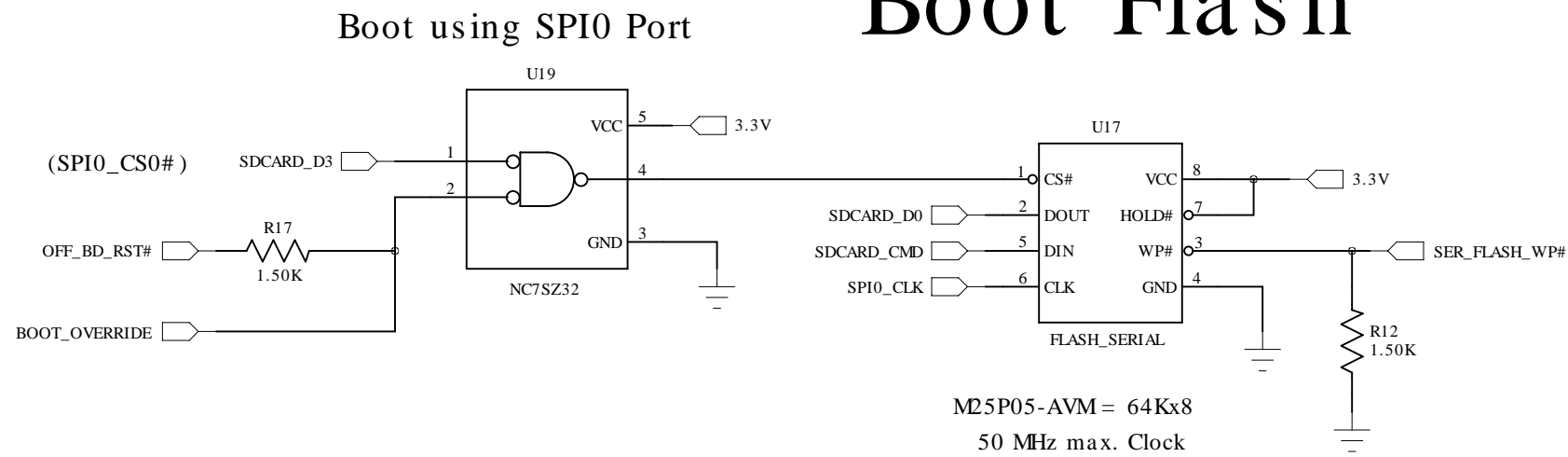
Temp Sensor



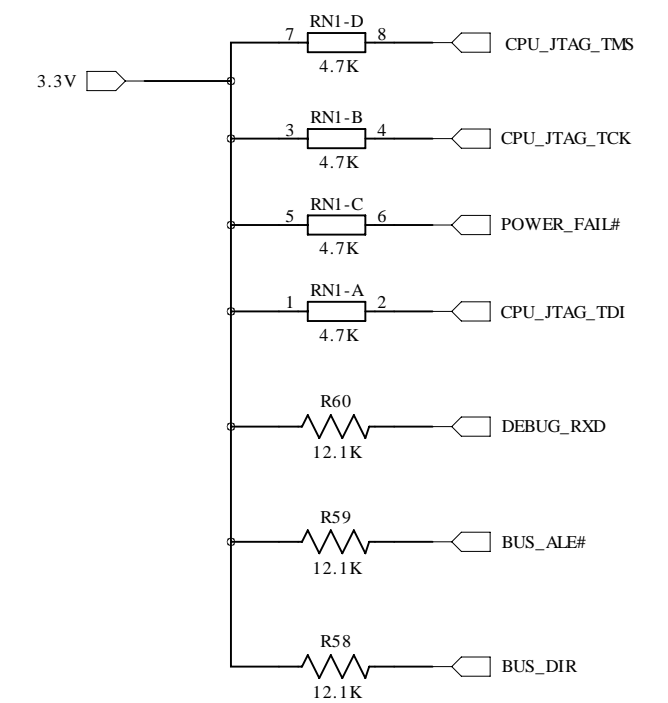
8K Byte NVRAM



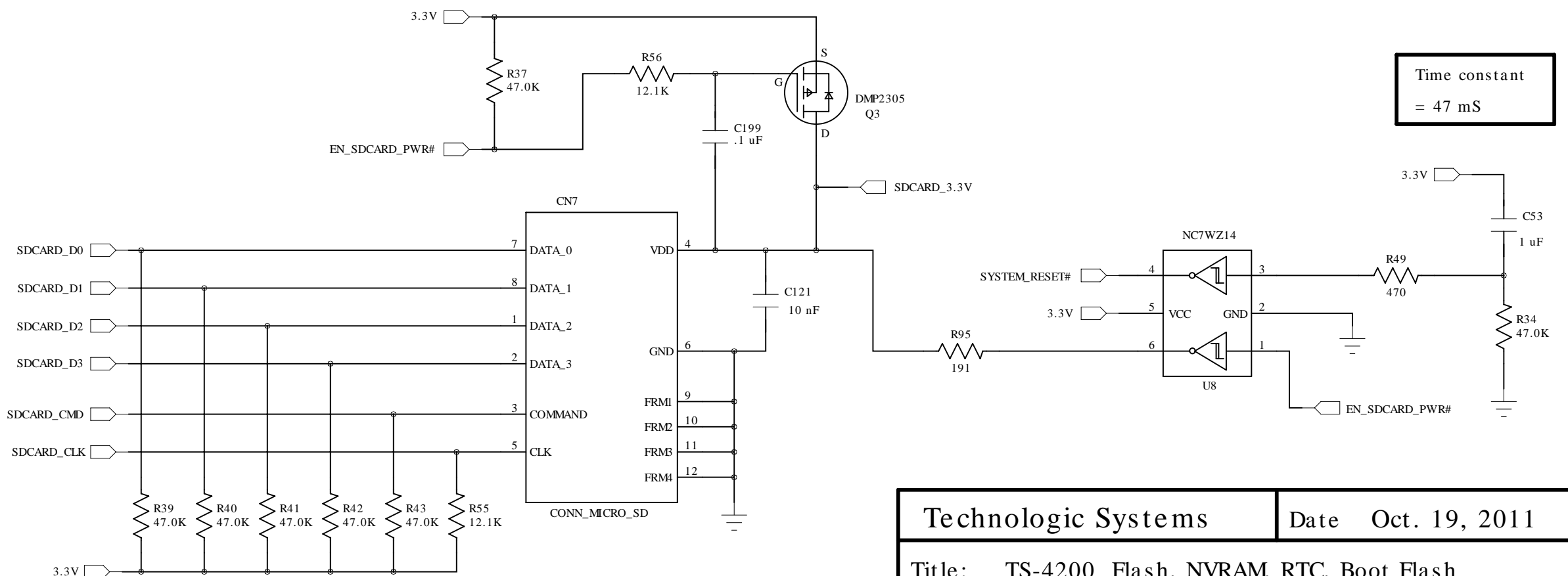
64KB Serial Boot Flash



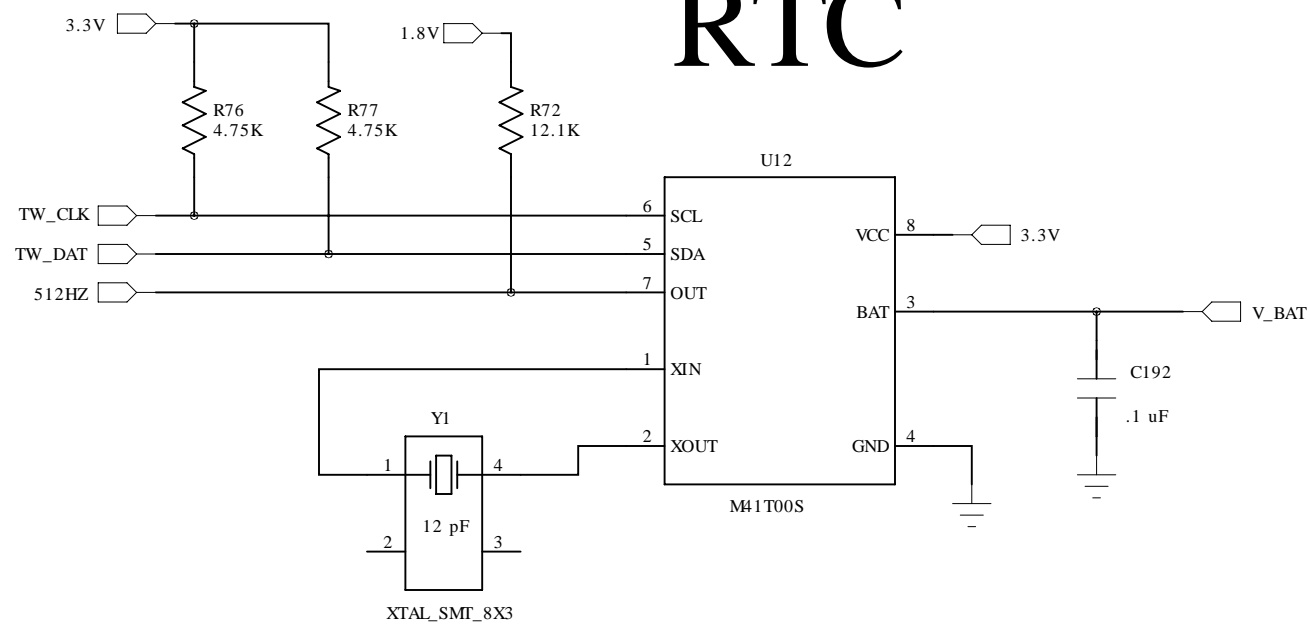
Boot using SPI0 Port



Micro SD Card Socket



RTC



Two 100-pin Off-board Connectors

⚠ All signals driving DIO on CN1 & CN2 must be powered by the 3.3V on CN2, or remain at 0V until the CN2 3.3V rail is > 3.0V

"POWER" pins supply all power to the module
Apply 3.6V to 5.5V to these pins

Current drain is 50mA to 400 mA

EXT_RESET# is an Input
used to reboot the CPU

CN2 pin 27 should be connected
to CN2 pin 33 on the base board

OFF_BD_RESET# is an Output
used to reset all peripherals

POWER_FAIL# must
not be driven high

SD Card
SD card signals on connector
are wired in parallel with
SD card socket. Only one
can be populated with SD card

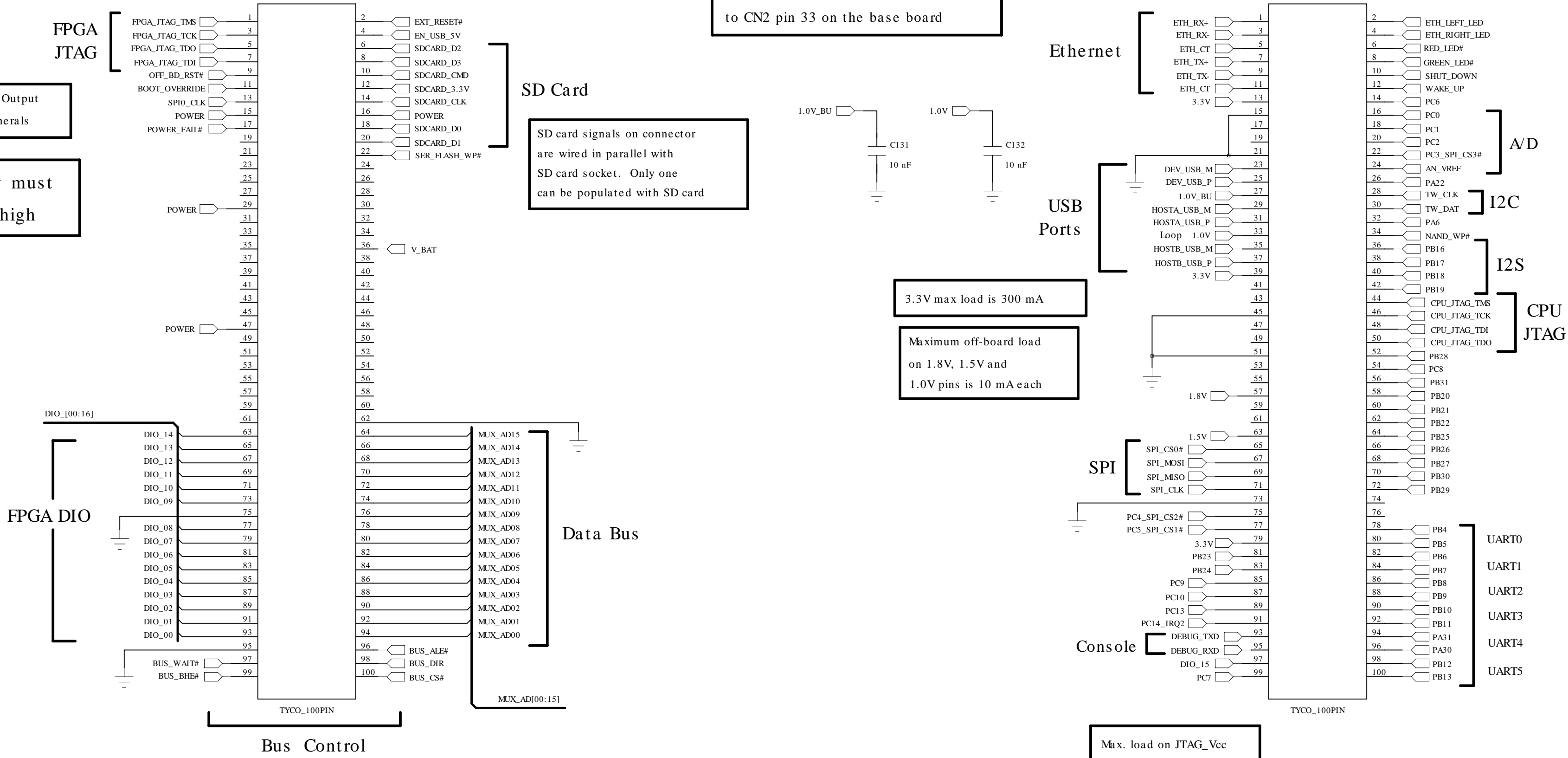
3.3V max load is 300 mA
Maximum off-board load
on 1.8V, 1.5V and
1.0V pins is 10 mA each

Max. load on JTAG_Vcc
(CN2-79) is 20 mA

These DIO have 1.8V levels
PC4, PC5, PC6
PC7, PC8, PC9
PC10, PC13, PC14
All other DIO uses 3.3V levels

Left

Right



Boot Strap

Mode 2	Boots from
1	NAND Flash
0	SD Card

BUS_DIR = MODE2

MODE1 and MODE2 states
are latched prior to
OFF_BD_RESET# deasserted

MODE1 and MODE2
have PU resistors

Use 1.5K ohm resistor
to "OFF_BD_RESET#"
to set Mode pins "low"

Devices connected to this bus must never
drive it when BUS_CS# is deasserted
(must be off within 30 nS of deassertion)

Devices must pull the BUS_WAIT# line low
if they need more than 150 nS strobe

The data bus can not have more than
30 pF of off-board capacitive loading
May need data buffer chip for heavy loads

If Bus is not needed, the following
can be changed to DIO:
- Bus Control signals
- MUX_AD08 thru 15

Bus cycles use 11 address lines
AD0 thru AD10
This provides 1K address space
for 8-bit bus cycles (000-3FF)
and 1K for 16-bit cycles (400-7FF)

BUS_ALE# = Address Latch Enable
BUS_BHE# = Byte High Enable (for 16-bit cycles)