3.3V Supply

1.8V Supply

1.5V Supply

1.0V Supply

Power Sequence
After power is first applied, or after a "Reboot"
All power rails are off for 200 ms then:
- the 3.3V and 1.8V are enabled
delayed with 1uF ceramic
20uS delay
- Then 2-4 mS later, the 1.0V rail is enabled
it also requires about 800 uS to ramp
cPU Reset is asserted before 1.0V rail is enabled

POR
POR chip holds LOW_VOL for 200 mS after
"VCC" rises above 2.9V
"POWER" = 3.2V Trip

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EN_ETH POWER must be off for at least 20 ms before turning on.

After turning PHY power on, must wait for 40 ms before enabling PHY signals.

When Ethernet PHY is powered off, then all PHY signals must be changed to 0V and set tri-state.

To CPU MAC

WDO can not be used until 100 us after Reset is deselected.

MDCLK max is 2.5 MHz.

Beware

PHY PU and PD resistors are 67k ohm typical.

CPU PU resistors are 70k typ. and 40k min.

The PHY address is controlled by strapping pin. If CPU has PU, PHY has PD --> indeterminant.
Two 100-pin Off-board Connectors

"POWER" pin supplies all power to the module. Apply 3.6V to 5.5V to these pins.

Current drain is 50mA to 400mA

OFF_BO_RESET# is an Output used to reset all peripherals.

EXT_RESET# is an Input used to reset all the CPU.

SD Card:
SD card signals on connector are wired in parallel with SD card socket. Only one can be populated with SD card.

USB Ports:
3.3V max load is 300mA
Maximum off-board load on 1.8V, 15V and 1.65V pins is 10mA each.

Ethernet:
Max load on JTAG_VCC (CN2-79) is 20mA

These DIO have 1.8V levels:
- PC4, PC5, PC6
- PC7, PC8, PC9
- PC10, PC13, PC14

Boot Strap:

<table>
<thead>
<tr>
<th>Mode 2</th>
<th>Boots from</th>
<th>Mode1 and Mode2 states are isolated prior to OFF_BO_RESET# deasserted</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>NAND Flash</td>
<td>MODE1 = MODE2</td>
</tr>
<tr>
<td>0</td>
<td>SD Card</td>
<td>MODE1 = MODE2, have PULL resistors</td>
</tr>
</tbody>
</table>

Bus Control:

Devices connected to this bus must never drive it when BUSIRQ# is deasserted (must be off within 30 ns of deassertion).

Devices must pull the BUS_WAIT# line low if they need more than 150 ns strobe.

The data bus can only have more than 30 pF of off-board capacitive loading. May need data buffer chip for heavy loads.

If Bus is not needed, the following can be changed to DIO:
- Bus Control signals
  - MAX_A008 thru 15

DIO_00 can be BUS_IRQ
DIO_01 can be BUS_DIR
DIO_02 can be BUS_CS#1
DIO_03 can be BUS_CS#2
DIO_04 can be BUS_CS#3
DIO_05 can be BUS_CS#4

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[Diagram showing connections and pinouts for FPGA, JTAG, SD Card, Ethernet, USB Ports, SPI, Console, and Data Bus connections]