CPU_RESET# is bi-directional and can be programmed to cause interrupt instead of reset.
### 3.3V Supply

- **1.5V Supply**
  - LDO to FPGA Core
  - 1.5V Supply

- **1.0V Supply**
  - To CPU Core

- **1.8V Supply**
  - 1.8V Supply

- **POR**
  - POR chip holds LOW_VOLT#
  - Low for 200 ms after "VCC" Max above 2.5V
  - "POWER" ≤ 5.2V Typ
10/100 Ethernet

To CPU
MAC

LED1 = Activity/Link
LED2 = Speed 100 Mbit
512 MB or 2 GB NAND Flash

64KB Serial Boot Flash

RTC

Temp Sensor

Micro SD Card Socket

8K Byte NVRAM

Time constant = 47 nS

NAND_WPSTATE

NAND ALE

NAND CLE

NAND CS#

NAND RD#

NAND WR# MUX AD00

NAND_BUSY#

1.8V

3.3V

1.8V

3.3V
Two 100-pin Off-board Connectors

*POWER* pins supply all power to the module
Apply 3.3V to 5.5V to these pins

Current drain is 50mA to 400 mA

**POWER FAIL#** must not be driven high

*OFF,BD_RESET#* is an Output
used to reset all peripherals

**OFF,BD_RESET#** is a Output
designed to assert prior to
**M ODE1** and **M ODE2** states

Apply 3.6V to 5.5V to these pins

**M ODE2** and **M ODE3** states
are locked prior to
**OFF,BD_RESET#** assertion

MODE1 and MODE3 have DC/AC mixers

**MODE0** and MODE2 have DC/AC mixers

**MODE0** and MODE2 states
are locked prior to
**OFF,BD_RESET#** assertion

These DIO have 1.8V levels
PC4, PC5, PC6
PC7, PC8, PC9
PC10, PC13, PC14

All other DIO uses 3.3V levels

**BUS_DIR = MODE2**

Devices connected to this bus must never
drive it when BUS_CS# is deasserted
(must be off within 50 ns of deassert)

Device must pull the BUS_WAIT# line low
if they need more than 150 ns strobe

**BUS_ALE# = Address Latch Enable**
**BUS_BHE# = Byte High Enable** (for 16-bit cycles)

**BUS_ALE#** and **BUS_BHE#** states
are locked prior to
**OFF,BD_RESET#** assertion

**EXT_RESET#** is an Input
used to reset the CPU

CN2 pin 27 should be connected
to CN2 pin 33 on the base board

**CN2 pin 27 should be connected**
to CN2 pin 33 on the base board

**CN2 pin 27 should be connected**
to CN2 pin 33 on the base board

3.3V max load is 500 mA

Minimum off-board load
on 3.3V, 1.5V and
1.8V pins is 10 mA each

- Bus Control signals
- MUX_AD08 through 15
- MUX_AD14 through 15
- MUX_AD[00:15]

- SPI0_CLK
- SPI0_CSN
- SPI0_SCK
- SPI0_MOSI

- UART0
- UART1
- UART2
- UART3
- UART4
- UART5

USB Ports

- USB0
- USB1
- USB2
- USB3
- USB4
- USB5

Ethernet

- A/D
- I2C
- I2S
- CPU
- JTAG

SD Card

- SD Card signals on connector
- are wired in parallel with
- SD card socket. Only one
- can be populated with SD card

Data Bus

- BUS_WAIT#
- SPI0_CLK
- SPI0_CSN
- SPI0_SCK
- SPI0_MOSI

These 1.8K ohm resistors
on "OFF_BD_RESET#" turn Mode pins "low"

The data bus can not have more than
50 pF of off-board capacitive loading
May need data buffer chip for heavy loads

Bus Control

Console

SPI

- RED LED#
- GREEN LED

- TX-
- 1.0V_BU
- RX+
- 1.5V
- 1.8V

- PA22
- PA31
- PB11
- PB9
- PB8
- PB5

- UART1
- UART2
- UART3
- UART4
- UART5

- 10 nF C131
- 10 nF

- PB24
- PB23
- PB22
- PB21
- PB20
- PB19

- 1.0V
- 1.5V
- 1.8V

- PC7
- PC8
- PC9
- PC10
- PC11
- PC12

- UART0
- UART1
- UART2
- UART3
- UART4
- UART5

- I2C
- SPI
- USB
- Ethernet

- PC13
- PC14
- PC15
- PC16
- PC17
- PC18

- 1000 SPI
- 100 UART
- 100 USB
- 100 Ethernet

- 100 Power
- 100 Clock
- 100 reset
- 100 Clear

- 100 FPGA
- 100 JTAG
- 100 Ethernet
- 100 SPI
- 100 USB
- 100 UART

- 100 SPI
- 100 USB
- 100 UART

- 100 SPI
- 100 USB
- 100 UART

- 100 SPI
- 100 USB
- 100 UART