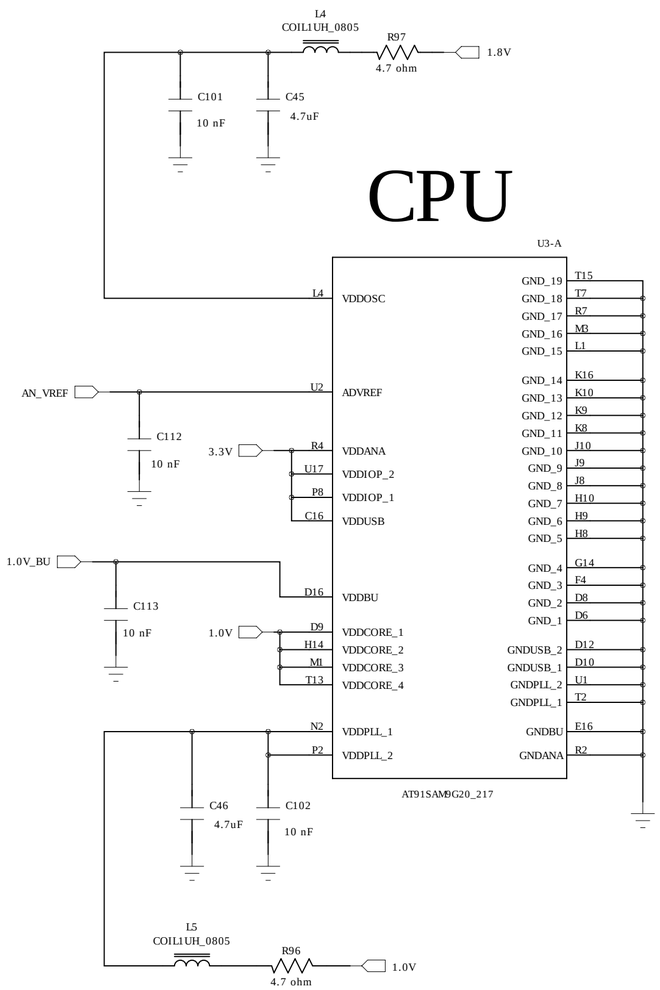
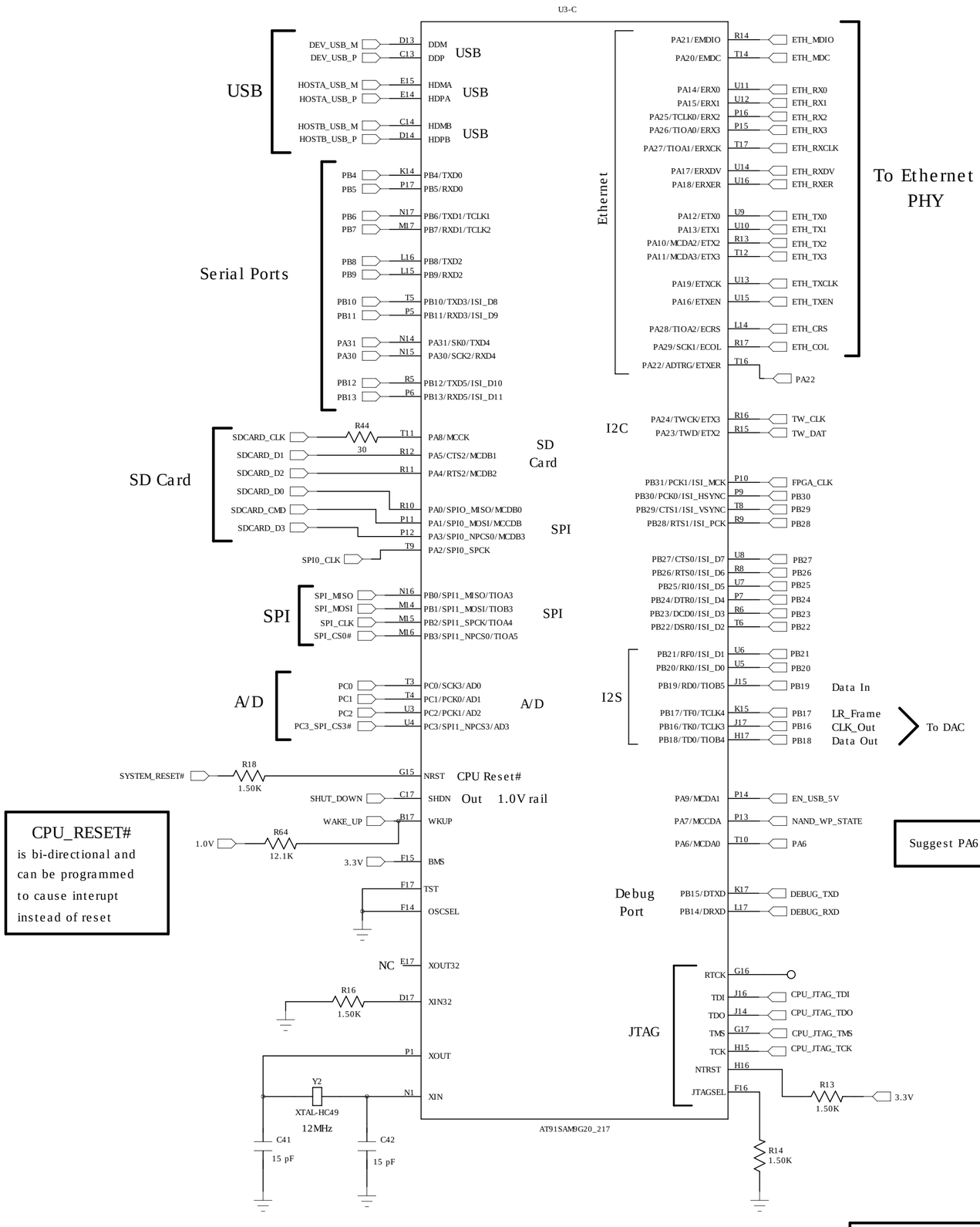
CPU



CPU



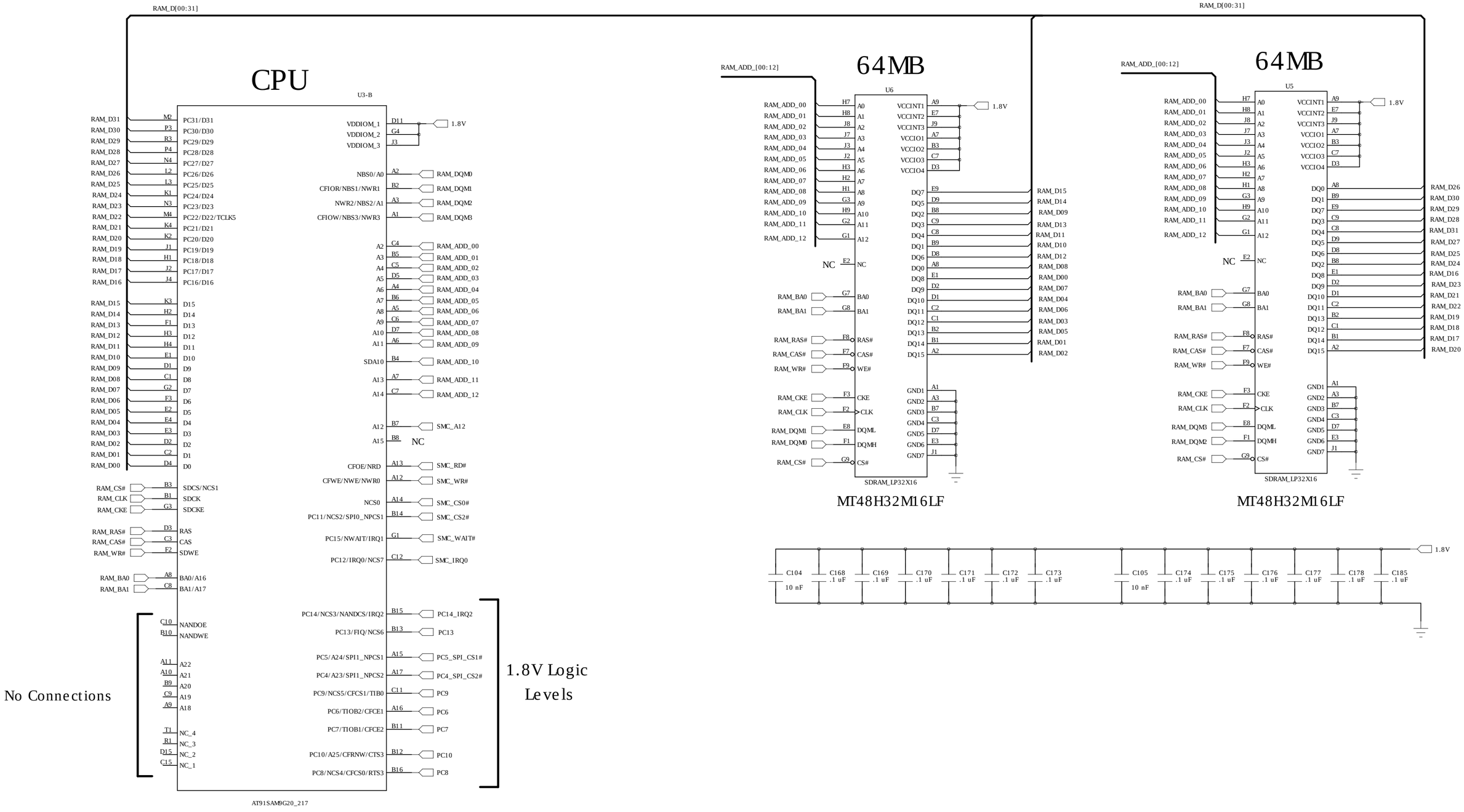
CPU_RESET#
is bi-directional and
can be programmed
to cause interupt
instead of reset

Suggest PA6 = En_Power to RS-232 Transceivers

MT1 1 MT125
MT2 1 MT125

Technologic Systems	Date Nov. 1, 2010	
Title: TS-4200 CPU		
Rev: C	Designer	Sheet 1 of 7

128 MB RAM



Technologic Systems		Date Nov. 1, 2010
Title: TS-4200 RAM		
Rev: C	Designer RLM	Sheet 2 of 7

A3P125 has:

3000 Tiles (about 1200 LUTs)

4 Kbytes total of Block RAM

97 I/O with 144 pin package

"true instant ON"

Input PLL clock = 1.5 MHz min

FPGA

Warning: MUX_AD00 thru AD07 is used by NAND Flash

Devices connected to this bus must never drive it when BUS_RD# is deasserted

(must be off within 30 nS of deassertion)

Devices must pull the BUS_WAIT# line low if they need more than 150 nS strobe

FPGA_CLK = CPU Timer Out

All NVRAM interface signals must be kept in low state when not accessing NVRAM

When SYSTEM_RESET# asserted, then set these as follows:

Asserted:

- OFF_BD_RST#
- EN_SDCARD_PWR#
- RED_LED#
- GREEN_LED#

Deasserted:

- EN_ETH_PWR#
- REBOOT
- NVRAM_CS
- NAND_CS#

When SYSTEM_RESET# deasserted, Latch BUS_ALE# and BUS_RD# into a register

Early Boot code should deassert OFF_BD_RST# signal. (after SPI Flash loaded into RAM)

Boot Straps

Mode 2	Boots from
1	NAND Flash
0	SD Card

BUS_ALE# = MODE1

BUS_RD# = MODE2

3.3V

1.8V

U4-A

MUX_AD[00:15]

RAM_D[00:31]

MUX_AD00	D5	GAC0/IO04RSB0	IO115RSB1	J2	RAM_D00
MUX_AD01	D9	GBB2/IO43RSB0	IO128RSB1	D1	RAM_D01
MUX_AD02	C10	GBA2/IO41RSB0	IO127RSB1	F4	RAM_D02
MUX_AD03	E8	GCC1/IO51RSB0	IO129RSB1	D2	RAM_D03
MUX_AD04	C5	IO10RSB0	IO100RSB1	K5	RAM_D04
MUX_AD05	D6	GAC1/IO05RSB0	GFB0/IO123RSB1	F1	RAM_D05
MUX_AD06	B9	GBB0/IO37RSB0	IO98RSB1	K6	RAM_D06
MUX_AD07	A9	IO25RSB0	GFC0/IO125RSB1	E2	RAM_D07
MUX_AD08	K11	GDA0/IO66RSB0	GAA2/IO67RSB1	D4	RAM_D08
MUX_AD09	K12	GDB0/IO64RSB0	IO68RSB1	E5	RAM_D09
MUX_AD10	G8	GDC1/IO61RSB0	IO130RSB1	D3	RAM_D10
MUX_AD11	F9	GCB0/IO54RSB0	IO116RSB1	J5	RAM_D11
MUX_AD12	F8	GCC0/IO52RSB0	GDB2/IO71RSB1	H8	RAM_D12
MUX_AD13	C9	IO27RSB0	GFC1/IO126RSB1	E3	RAM_D13
MUX_AD14	D8	GBC1/IO36RSB0	GDA2/IO70RSB1	J9	RAM_D14
MUX_AD15	D7	GBC0/IO35RSB0	IO117RSB1	J6	RAM_D15
BUS_ALE#	G9	IO48RSB0	GEB1/IO110RSB1	J1	RAM_DQM0 A0/Low Byte En.
BUS_DIR	H11	IO49RSB0	GFC2/IO118RSB1	H3	RAM_DQM1 High Byte Enable
BUS_CS#	G10	GCC2/IO59RSB0	GEB0/IO109RSB1	K1	RAM_DQM2 Address 1
BUS_BHE#	C11	IO42RSB0	GEC1/IO112RSB1	H4	RAM_ADD_00 Address 2
FPGA_CLK	D10	IO28RSB0	GAC2/IO131RSB1	C3	RAM_ADD_01 Address 3
OFF_BD_RST#	H7	IO60RSB0	GFA1/IO121RSB1	G1	RAM_ADD_02 Address 4
EN_SDCARD_PWR#	H6	IO50RSB0	GFB2/IO119RSB1	H2	RAM_ADD_03 Address 5
PB31	J11	GDA1/IO65RSB0	GEA1/IO108RSB1	K2	RAM_ADD_04 Address 6
DIO_00	A11	GBA1/IO40RSB0	GEC0/IO111RSB1	J4	RAM_ADD_05 Address 7
DIO_01	B10	GBB1/IO38RSB0	GEC2/IO104RSB1	M2	RAM_ADD_06 Address 8
DIO_02	A10	GBA0/IO39RSB0	IO132RSB1	C1	RAM_ADD_07 Address 9
DIO_03	B5	IO08RSB0	GEA2/IO106RSB1	K4	RAM_ADD_08 Address 10
DIO_04	A4	GAB1/IO03RSB0	IO103RSB1	M3	RAM_ADD_09 Address 11
DIO_05	B4	GAA1/IO01RSB0	GEA0/IO107RSB1	K3	SMC_A12 Address 12
DIO_06	A3	GAB0/IO02RSB0	IO101RSB1	M4	RAM_ADD_11 Address 13
DIO_07	B3	GAA0/IO00RSB0	IO95RSB1	L6	SMC_IRQ0
DIO_08	A5	IO11RSB0	GFA0/IO122RSB1	G4	SMC_WAIT#
DIO_09	C6	IO12RSB0	IO94RSB1	M6	SMC_RD#
DIO_10	B6	IO14RSB0	IO97RSB1	M5	SMC_WR#
DIO_11	A7	IO18RSB0	IO74RSB1	L8	SMC_CS0#
DIO_12	B7	IO19RSB0	IO75RSB1	M8	SMC_CS2#
DIO_13	C7	IO21RSB0			
DIO_14	B8	IO22RSB0			
DIO_15	C8	IO24RSB0			
EN_ETH_POWER#	J12	GDB1/IO63RSB0			
BUS_WAIT#	H9	GDC0/IO62RSB0			
NVRAM_CS	G12	GCB2/IO58RSB0			
NVRAM_MISO	G11	IO47RSB0			
NVRAM_MOSI	F11	GCA1/IO55RSB0			
NVRAM_CLK	F12	GCA2/IO57RSB0			
NAND_CLE	D12	GCB1/IO53RSB0			
NAND_ALE	D11	IO44RSB0			
NAND_RD#	E12	IO46RSB0			
NAND_WR#	C12	GBC2/IO45RSB0			
NAND_CS#	E11	GCA0/IO56RSB0			
FPGA_JTAG_TDO	J10	TDO			
FPGA_JTAG_TMS	L9	TMS			
FPGA_JTAG_TDI	M9	TDI			
FPGA_JTAG_TCK	J8	TCK			
3.3V	L12	TRST			
Input	GEB2/IO105RSB1	L3	R80 4.75K	PB4	UART0_TXD
Input	GFA2/IO120RSB1	C2	R79 4.75K	SYSTEM_RESET#	
Input	IO102RSB1	L4	512HZ		
Out	IO85RSB1	L7	REBOOT		
Input	IO86RSB1	M7	POWER_FAIL#		
Input	GFB1/IO124RSB1	F3	NAND_BUSY#		
Input	GAB2/IO69RSB1	B1	200 Hz R35 47.0K		
Out	GDC2/IO72RSB1	K9	GREEN_LED#		
Out	IO73RSB1	K8	RED_LED#		

A3P125_FG144

DIO_[00:15]

R61 12.1K, R62 12.1K, R63 12.1K to 3.3V

To CPU Address/Data Bus

Inputs with 1.8V rail have diode clamp to 1.8V

REBOOT high causes all power rails to go low for 200 mS

RED_LED# and GREEN_LED# must be Open Drain

U9 NC7SZ14: 1.8V, VCC, NC, GND, C161 .1 uF

FPGA

U4-B

1.5V	A8	VCC_1	
	C4	VCC_2	
	E1	VCC_3	
	E10	VCC_4	
	H1	VCC_5	
	H5	VCC_6	
	H12	VCC_7	
	J7	VCC_8	
1.8V	E4	VCCIB1_1	
	J3	VCCIB1_2	
	L5	VCCIB1_3	
	M10	VCCIB1_4	
	L2	VMV1_1	
	L11	VMV1_2	
3.3V	E6	VCCIB0_1	
	E7	VCCIB0_2	
	E9	VCCIB0_3	
	H10	VCCIB0_4	
	A2	VMV0_1	
	B12	VMV0_2	
	M11	VPUMP	
	L10	VJTAG	
	G3	VCCPLF	
	F2	VCOMPLF	
	A6	GND_1	
	B2	GND_2	
	B11	GND_3	
	F5	GND_4	
	F6	GND_5	
	F7	GND_6	
	F10	GND_7	
	G2	GND_8	
	G5	GND_9	
	G6	GND_10	
	G7	GND_11	
	K7	GND_12	
	K10	GND_13	
	L1	GND_14	
	A1	GNDQ_1	
	A12	GNDQ_2	
	M1	GNDQ_3	
	M12	GNDQ_4	

A3P125_FG144

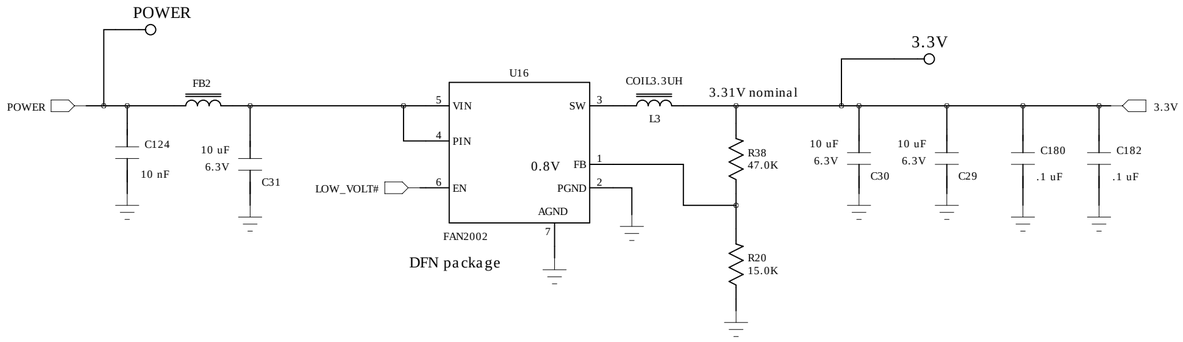
1.8V: C197 .1 uF, C198 .1 uF, C128 10 nF, C129 10 nF

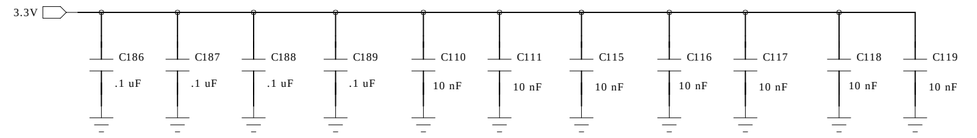
RMCF 1/16S 10 5% R

1.5V: R98 4.7 ohm, L6 COIL1UH_0805 LQM21FN1R0N, C100 10 nF, C44 4.7uF

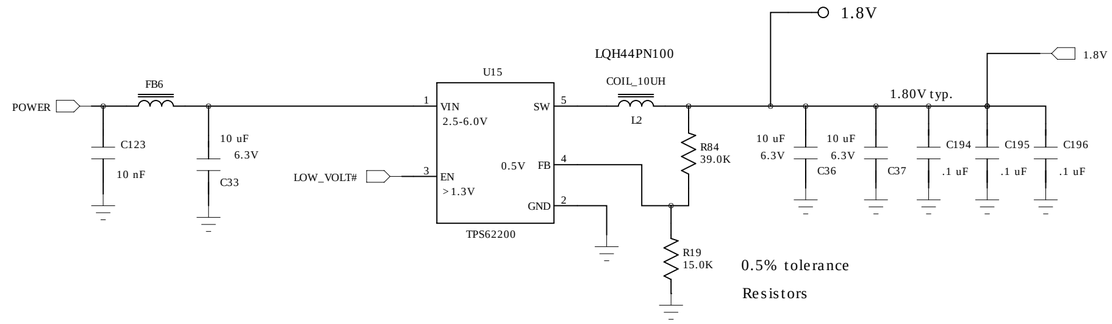
Technologic Systems	Date Nov. 1, 2010	
Title: TS-4200 FPGA		
Rev: C	Designer	Sheet 3 of 7

3.3V Supply

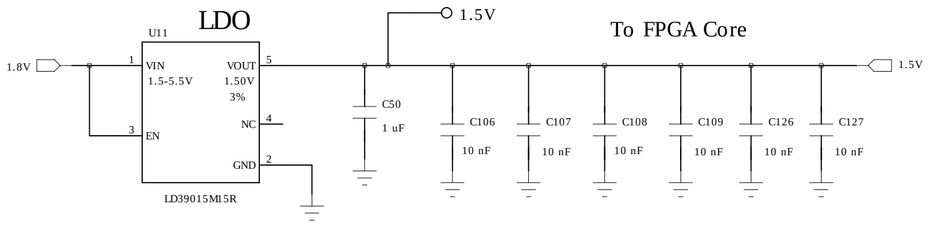




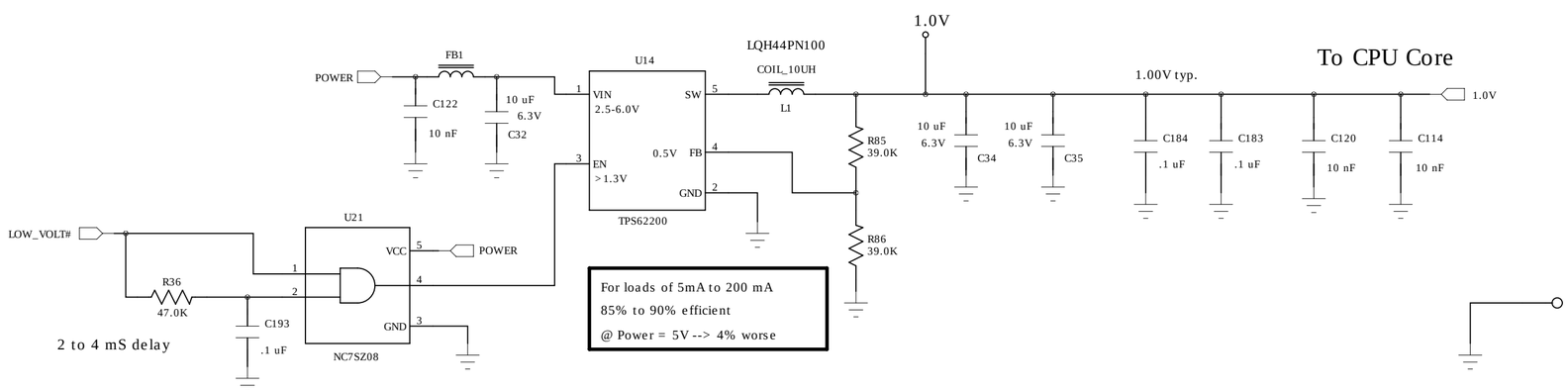
1.8V Supply



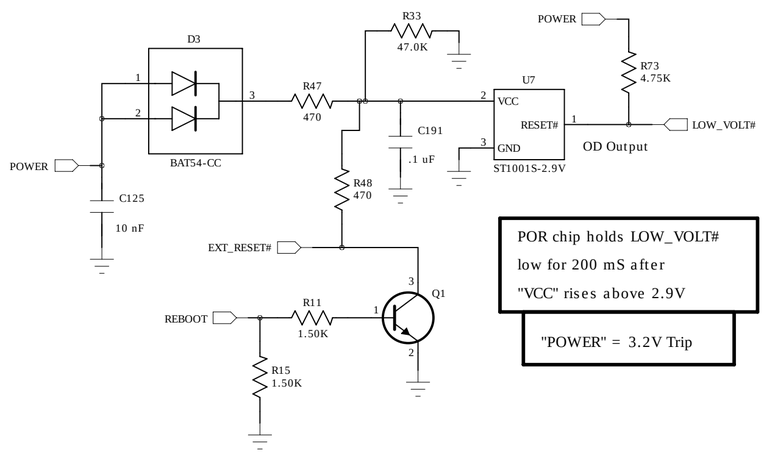
1.5V Supply



1.0V Supply

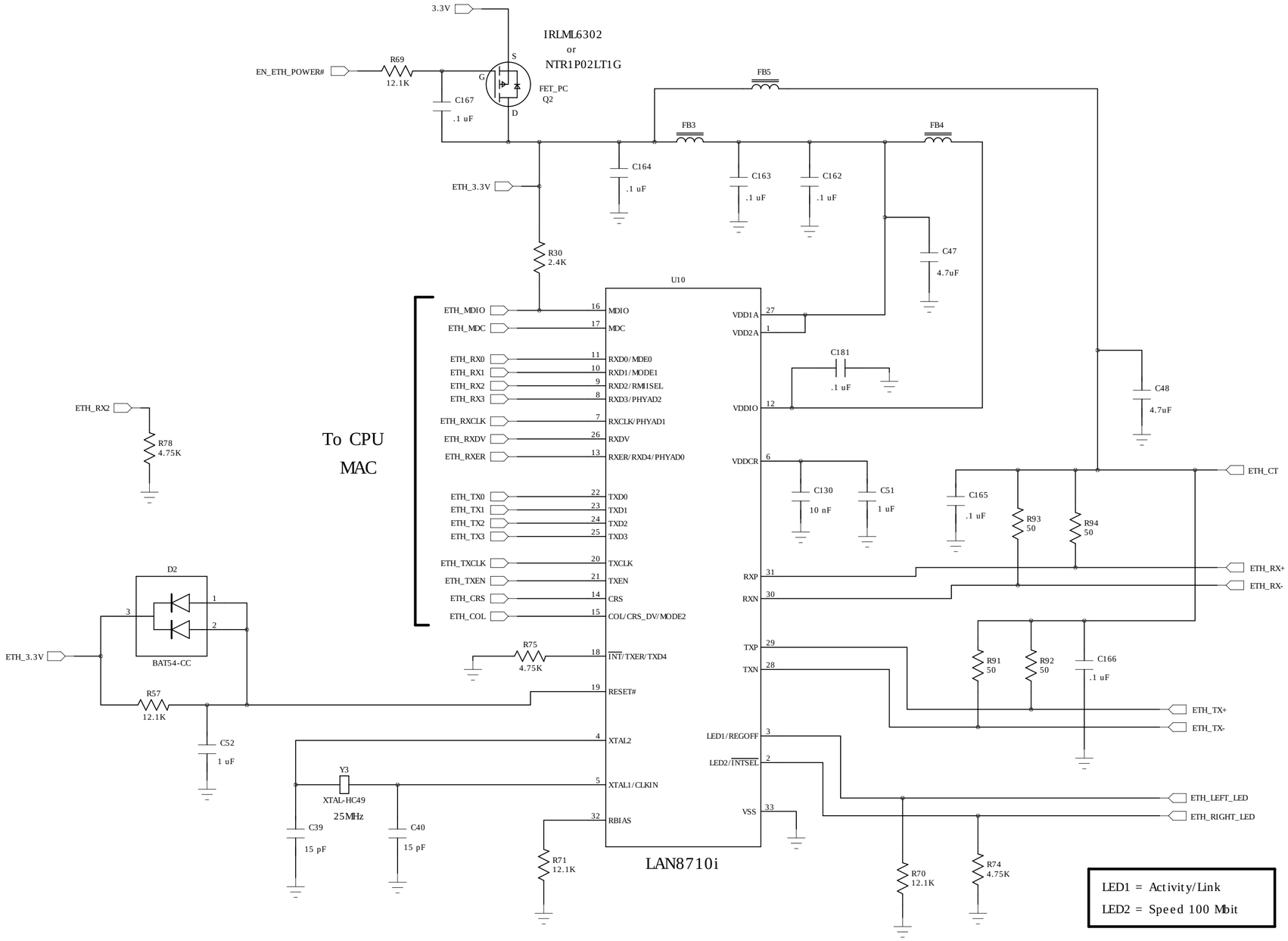


POR



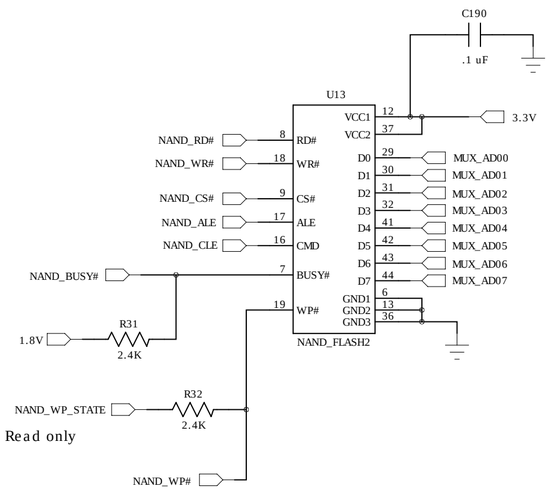
Technologic Systems	Date Nov. 1, 2010	
Title: TS-4200 Power Supplies and POR		
Rev: C	Designer RLM	Sheet 4 of 7

10/100 Ethernet

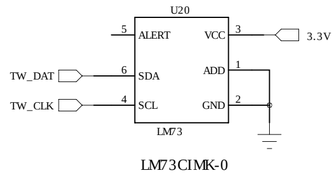


Technologic Systems		Date Nov. 1, 2010
Title: TS-4200 Ethernet PHY		
Rev: C	Designer	Sheet 5 of 7

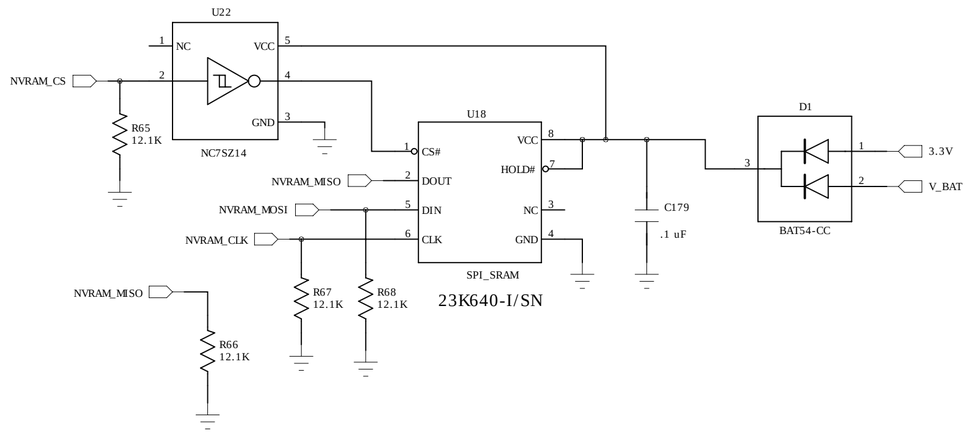
512 MB or 2 GB NAND Flash



Temp Sensor

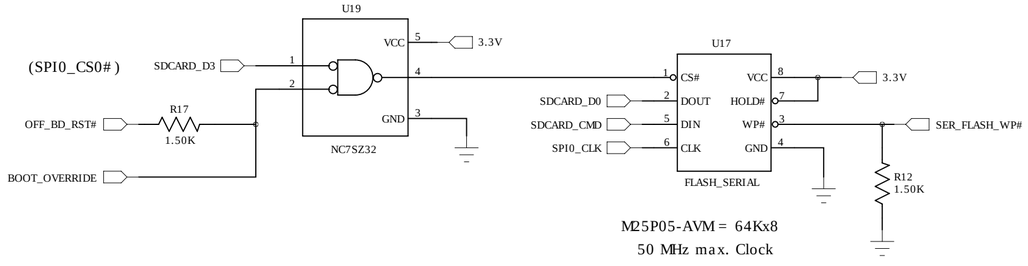


8K Byte NVRAM

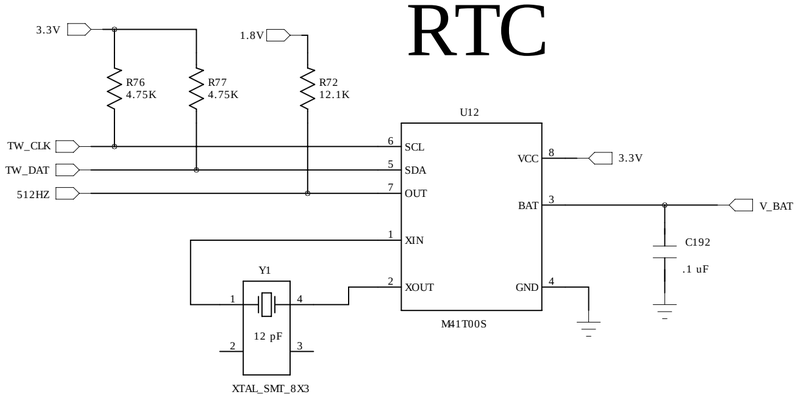


64KB Serial Boot Flash

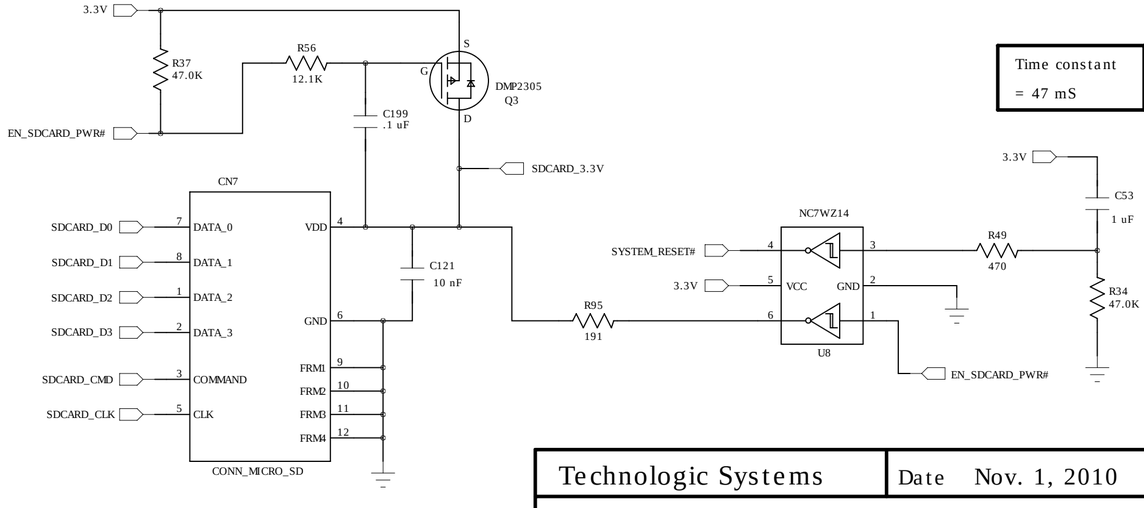
Boot using SPI0 Port

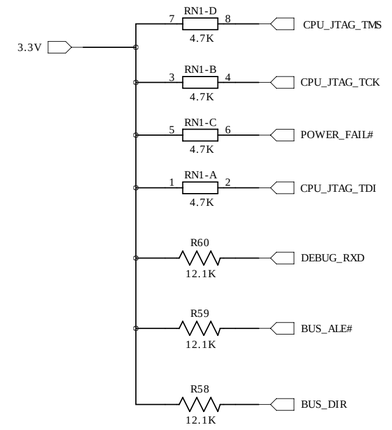


RTC



Micro SD Card Socket





Technologic Systems	Date Nov. 1, 2010	
Title: TS-4200 Flash, NVRAM, RTC, Boot Flash		
Rev: C	Designer	Sheet 6 of 7

Two 100-pin Off-board Connectors

"POWER" pins supply all power to the module
Apply 3.6V to 5.5V to these pins

Current drain is 50mA to 400 mA

All signals driving DIO on CN1 & CN2 must be powered by the 3.3V on CN2, or remain at 0V until the CN2 3.3V rail is > 3.0V

EXT_RESET# is an Input
used to reboot the CPU

CN2 pin 27 should be connected
to CN2 pin 33 on the base board

Left

CN1

FPGA JTAG: FPGA_JTAG_TMS 1, FPGA_JTAG_TCK 3, FPGA_JTAG_TDO 5, FPGA_JTAG_TDI 7

OFF_BD_RST# 9

BOOT_OVERRIDE 11

SPI0_CLK 13

POWER 15

POWER_FAIL# 17

POWER 29

POWER 47

2 EXT_RESET#
4 EN_USB_5V
6 SDCARD_D2
8 SDCARD_D3
10 SDCARD_CMD
12 SDCARD_3.3V
14 SDCARD_CLK
16 POWER
18 SDCARD_D0
20 SDCARD_D1
22 SER_FLASH_WP#

SD Card

SD card signals on connector
are wired in parallel with
SD card socket. Only one
can be populated with SD card

36 V_BAT

OFF_BD_RESET# is an Output
used to reset all peripherals

POWER_FAIL# must
not be driven high

DIO_[00:16]

FPGA DIO: DIO_14 63, DIO_13 65, DIO_12 67, DIO_11 69, DIO_10 71, DIO_09 73, DIO_08 75, DIO_07 77, DIO_06 79, DIO_05 81, DIO_04 83, DIO_03 85, DIO_02 87, DIO_01 89, DIO_00 91

BUS_WAIT# 97
BUS_BHE# 99

64 MUX_AD15
66 MUX_AD14
68 MUX_AD13
70 MUX_AD12
72 MUX_AD11
74 MUX_AD10
76 MUX_AD09
78 MUX_AD08
80 MUX_AD07
82 MUX_AD06
84 MUX_AD05
86 MUX_AD04
88 MUX_AD03
90 MUX_AD02
92 MUX_AD01
94 MUX_AD00

Data Bus

96 BUS_ALE#
98 BUS_DIR
100 BUS_CS#

TYCO_100PIN

MUX_AD[00:15]

Bus Control

1.0V_BU — C131 10 nF
1.0V — C132 10 nF

Right

CN2

Ethernet: ETH_RX+ 1, ETH_RX- 3, ETH_CT 5, ETH_TX+ 7, ETH_TX- 9, ETH_CT 11, 3.3V 13

USB Ports: DEV_USB_M 23, DEV_USB_P 25, 1.0V_BU 27, HOSTA_USB_M 29, HOSTA_USB_P 31, Loop 1.0V 33, HOSTB_USB_M 35, HOSTB_USB_P 37, 3.3V 39

3.3V max load is 300 mA

Maximum off-board load
on 1.8V, 1.5V and
1.0V pins is 10 mA each

1.8V 57

SPI: 1.5V 63, SPI_CS0# 65, SPI_MOSI 67, SPI_MISO 69, SPI_CLK 71

PC4_SPI_CS2# 75
PC5_SPI_CS1# 77
3.3V 79
PB23 81
PB24 83
PC9 85
PC10 87
PC13 89
PC14_IRQ2 91

Console: DEBUG_TXD 93, DEBUG_RXD 95

DIO_15 97
PC7 99

2 ETH_LEFT_LED
4 ETH_RIGHT_LED
6 RED_LED#
8 GREEN_LED#
10 SHUT_DOWN
12 WAKE_UP
14 PC6
16 PC0
18 PC1
20 PC2
22 PC3_SPI_CS3#
24 AN_VREF

A/D

26 PA22
28 TW_CLK
30 TW_DAT

I2C

32 PA6
34 NAND_WP#
36 PB16
38 PB17
40 PB18
42 PB19

I2S

44 CPU_JTAG_TMS
46 CPU_JTAG_TCK
48 CPU_JTAG_TDI
50 CPU_JTAG_TDO

CPU JTAG

52 PB28
54 PC8
56 PB31
58 PB20
60 PB21
62 PB22
64 PB25
66 PB26
68 PB27
70 PB30
72 PB29
74
76
78 PB4
80 PB5
82 PB6
84 PB7
86 PB8
88 PB9
90 PB10
92 PB11
94 PA31
96 PA30
98 PB12
100 PB13

UART0
UART1
UART2
UART3
UART4
UART5

TYCO_100PIN

Boot Strap

Mode 2	Boots from
1	NAND Flash
0	SD Card

BUS_DIR = MODE2

MODE1 and MODE2 states
are latched prior to
OFF_BD_RESET# deasserted

MODE1 and MODE2
have PU resistors

Use 1.5K ohm resistor
to "OFF_BD_RESET#"
to set Mode pins "low"

Devices connected to this bus must never
drive it when BUS_CS# is deasserted
(must be off within 30 nS of deassertion)

Devices must pull the BUS_WAIT# line low
if they need more than 150 nS strobe

The data bus can not have more than
30 pF of off-board capacitive loading
May need data buffer chip for heavy loads

BUS_ALE# = Address Latch Enable
BUS_BHE# = Byte High Enable (for 16-bit cycles)

If Bus is not needed, the following
can be changed to DIO:
- Bus Control signals
- MUX_AD08 thru 15

These DIO have 1.8V levels
PC4, PC5, PC6
PC7, PC8, PC9
PC10, PC13, PC14

All other DIO uses 3.3V levels

Technologic Systems	Date Nov. 1, 2010	
Title: TS-4200 Off-board Connectors		
Rev: C	Designer	Sheet 7 of 7