TECHNOLIGIC SYSTEMS

Title: TS-4200 Ethernet PHY
Rev: D
Sheet 5 of 7

10/100 Ethernet

EN_ETH_POWER# must be off for at least 20 ms before turning ON.

After turning PHY power on, Must wait for 40 ms before enabling MI signals.

When Ethernet PHY is powered off, then all MI signals must be changed to DIO and set tri-state.

To CPU

MAC

ETH_3.3V

ETH_LEFT_LED

ETH_RIGHT_LED

ETH_CT

ETH_RX+

ETH_TX+

ETH_RX-

ETH_TX-

ETH_RX0

ETH_TX0

ETH_RX1

ETH_TX1

ETH_RX2

ETH_TX2

ETH_RX3

ETH_TX3

ETH_RXCLK

ETH_TXCLK

ETH_RXER

ETH_TXER

ETH_COL

ETH_CRS

ETH_MDC

ETH_MDI

ETH_3.3V

ETH_MDI0

ETH_MDO

LED1 = Activity/Link
LED2 = Speed 100 Mbit
**Two 100-pin Off-board Connectors**

“POWER” pins supply all power to the module. Apply 3.6V to 5.5V to these pins.

Current drain is 50mA or 400 mA.

**POWER_FAIL#** must not be driven high.

**OFF_BD_RESET#** is an Input used to reset all peripherals.

**OFF_BD_RESET#** must be asserted before Mode1 and Mode2 states.

Apply 3.6V to 5.5V to these pins:
- **POWER** pins supply power to the module.

**Boot Strap**

- Mode 0 (left): NAND Flash
- Mode 1 (right): SD Card

**BUS_DIR = MODE2**

**ICE_BD_RESET#** is an Input used to reset the CPU.

**CN2 pin 27 should be connected to CN2 pin 33 on the base board.**

**CN2 pin should be connected to CN2 pin 33 on the base board.**

**SD Card**

SD card signals on connector are wired in parallel with SD card socket. Only one can be populated with SD card.

- **SPI**
- **USB Ports**
- **Ethernet**
- **CPU JTAG**
- **Console**

**These DIO have 1.8V levels**

- PC4, PC5, PC6
- PC7, PC8, PC9
- PC10, PC13, PC14

**All other DIO uses 3.3V levels**

- **Signal levels and currents**
- **Bus cycle 11 address lines**
  - AD0 to AD10
  - This provides 1K address space
  - 8-bit bus cycles (000–3FF)
  - 1K for 16-bit cycles (400–7FF)

**DIO settings**

- **DIO_00 to DIO_14**
- **DIO_07**
- **DIO_08 to DIO_10**
- **DIO_11 to DIO_13**
- **DIO_15**

**Bus Control**

- Devices connected to this bus must never drive it when BUS_CS# is deasserted (must be off within 50 nS of deassertion)
- Devices must pull the BUS_WAIT# line low if they need more than 150 nS strobe
- The data bus can not have more than 50 pF of off-board capacitive loading
- May need data buffer chip for heavy loads
- **BUS_AL# = Address Latch Enable**
- **BUS_BHE# = Byte High Enable (for 16-bit cycles)**

**Technologic Systems**

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