- OSC_SEL = "0" -> Use internal RC Oscillator
- TST = "0" -> Factory Test Mode
- OSC_SEL = "0" -> Use internal RC Oscillator

CPU_RESET# is bi-directional and can be programmed to cause interrupt instead of reset

WAKE_UP Ref. Design has 10KPU to 1.0V and sw. to GND

Strap Options

| BMS = "1" | Boot from Internal ROM |
| TST = "1" | Factory Test Mode |
| OSC_SEL = "0" | Use internal RC Oscillator |
Warning: MUX_4G00 thru ID007 is used by NAND Flash.

Devices connected to this bus must never drive it when BUS_RD is deasserted (must be off within 50 nS of deassertion).

Devices must pull the BUS_WAIT line low if they need more than 150 nS strobe.

Input PLL clock = 1.5 MHz min.

4 Kbytes total of Block RAM

3000 Tiles (about 1200 LUTs)

“true instant ON”

Drive it when BUS_RD# is deasserted

Device connected to this bus must never drive it when BUS_RD is deasserted

97 I/O with 144 pin package

(must be off within 30 nS of deassertion)

if they need more than 150 nS strobe

97 I/O with 144 pin package

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if they need more than 150 nS strobe

FPGA_CLK = CPU Time Out

FPGA_CLIK = CPU Time Out

To CPU

Address/Data Bus

When SYSTEM_RESET# asserted, then set these as follows:

Assisted:
OFF_BD_RST
EN_SD/SD1_PWR#
RED_LEDS
GREEN_LEDS

Deasserted:
EN_ETH_PWR#
REBOOT
NVRAM_CS
NAND_CS#

When SYSTEM_RESET# deasserted, each BUS_ALE# and BUS_RD# into a register

Early Boot code should deassert OFF_BD_RST# signal

(after SPI Flash loaded into RAM)

Boot Straps

Mode 2

Mode 1

0

NAND Flash

SD Card

BUS_ALE# = MODE1

BUS_RD# = MODE2

All NVRAM interface signals must be kept in low state when not accessing NVRAM

Inputs with 1.8V rail have deals clamp to 1.8V

REBOOT high causes all power rails to go low for 200 nS

RED_LEDS and GREEN_LEDS must be Open Drain

REBOOT high causes all power rails to go low for 200 nS

RED_LEDS and GREEN_LEDS must be Open Drain

NAND_CS#

NAND_RD#

NAND_CLE
3.3V Supply

1.8V Supply

1.5V Supply

1.0V Supply

Power Sequence

After power is first applied, or after a "Reset"
All power rails are off for 200 ms then:
- the 3.3V and 1.8V are enabled
delay with 1 uF ceramic
- Then 2-4 ms later, the 1.0V rail is enabled
It also requires about 800 uS to ramp

CPU Reset# is asserted before 1.0V rail is enabled

POR

POR chip holds LOW_VOLT
till 200 mS after
"CC" rises above 2.9V
"POWER" = 3.2V Top
10/100 Ethernet

Resistor PD on pin 18 is not required per data sheet. But Jesse could not get it to work until we added it.

Ethernet PHY has not been used until 100 MHz after Reset# is deasserted.

RXCLK must be biased low to enable internal 1.8V reg.

LED1 = Activity/Link
LED2 = Speed 100 Mbit

PHY PU and PD resistors are 67K ohm typical.

The PHY address is controlled by stripping pins. If CPU has PU, PHY has PD -> indeterminate

CPU PU resistors are 10K typ. and 40K min.

PHY PU resistor on pin 18 is not required per data sheet.
Two 100-pin Off-board Connectors

- "POWER" pins supply all power to the module
  - Apply 3.3V to 5V to these pins

- Current drain is 50mA to 400 mA

POWER_FAIL# must not be driven high

FPGA JTAG

OFF_RD_RESET# is an Output
  - used to reset all peripherals

MODE1 and MODE2

- SD Card
  - SD card signals on connector are wired in parallel with SD card socket: Only one can be populated with SD card

FPGA DIO

CN2 pin 27 should be connected to CN2 pin 33 on the base board

3.3V max load is 300 mA

SPI

Minimum off-board load on 3.3V, 1.5V and 1.0V pins is 16 mA each

Bus Control

- BUS_DIR = MODE2
- MODE1 and MODE2 states are latched via OFF_RD_RESET# deasserted

- MODE1 and MODE2 have 5V inputs

- BUS_AL = Address Latch Enable
  - BUS_AL# = Address Latch Enable (for 16-bit cycles)

- BUS_BHE = Byte High Enable

Slot 1 use 5k resistor on "OFF_RD_RESET#" to set Mode pins "low"

BOOT STRAP

- Mux. load on JTAG_Vcc
  - (CN2-79) is 20 mA

Data Bus

USB Ports

Ethernet

CPU JTAG

SPI

SD Card

Console

These DIO have 1.8V levels

- PC4, PC5, PC6
- PC7, PC8, PC9
- PC10, PC13, PC14

All other DIO uses 3.3V levels

Technologic Systems

Date: Oct. 19, 2011

Title: TS-4200 Off-board Connectors

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