March 2015

Changes from Rev.D to Rev.E

Added R28 = 45.3 ohm in series with RAM clock
This was required because 128 MB RAM version would fail at -20 to -40 degrees
This was seen in about 40% of all 128 MB boards
Problem was never reproduced in 64 MB versions

Rev.E BOM changes

Only change to BOM is adding
R28 = 60-4770-4
CPU

Serial Ports

SD Card

SPI

A/D

CPU_RESET# is bi-directional and can be programmed to cause interrupt instead of reset.
128 MB RAM

CPU

64MB

Logic Levels in this "Gate" are all 0 to 1.8V

1.8V Logic Levels
Warning: MXU_AD00 thru AD07 must be driven when BUS_RD# is deasserted (must be off within 30 nS of deassertion)

Device connected to this bus must never drive it when BUS_RD# is deasserted

Device must pull the BUS_W4TW bus low if they need more than 150 nS settle

A3P125 has:
- FPGA_JTAG_TDO
- FPGA_JTAG_TMS
- FPGA_JTAG_TCK
- FPGA_JTAG_TDI

DIO_09 = Push_switch

If they need more than 150 nS strobe

Boot Straps

Mode  | Boot's Item
-------|-------------
0     | NAND Flash
1     | SD Card

BUS_ALF = MODE1
BUS_RD# = MODE2

To CPU
Address/Data Bus

RED_LED and GREEN_LED must be Open Drain

Inputs with 1.8V rail have diodes clamp to 1.8V

REBOOT high causes all power rails to go low for 200 mS
3.3V Supply

1.8V Supply

1.5V Supply

1.0V Supply

Power Sequence

After power is first applied, or after a "Reboot"
All power rails are off for 200 ms then:
- the 3.3V and 1.8V are enabled
  these will reach 95% in about 800 µs
  (the 1.5V rail will ramp 25 µs delayed)
- Then 2–4 ms later, the 1.0V rail is enabled
  It also requires about 800 µs to ramp

CPU Reset# is asserted before 1.0V rail is enabled

POR

POR chip holds LOW_VOLT
low for 200 ms after
"MCC" rail above 2.9V

"POWER" ≥ 3.2V Typ

Technologic Systems

Date March 22, 2015

Title: TS-4200 Power Supplies and POR
Rev: E Designer RLM Sheet 5 of 8
**Title:** TS-4200 Ethernet PHY

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**10/100 Ethernet**

**EN_ETH_POWER** must be off for at least 20 ms before turning ON.

After turning PHY power on, must wait for 40 ms before enabling MI signals.

When Ethernet PHY is powered off, then all MI signals must be changed to DIO and set tri-state.

To CPU MAC

- **PHY PU and PD resistors** are 67K ohm typical.
- **CPU PU resistors** are 70K (up) and 40K ohm.
Two 100-pin Off-board Connectors

- **Off-BD_RESET#** is an Output
  - not be driven high
- **OFF_BD_RESET#** are latched prior to
  - CN2 pin 27 should be connected to
    - CN2 pin 33 on the base board
- **Power_FAIL#** must not be driven high

### Boot Strap

- **Mode 2**
  - BUS_DIR = MODE2
  - POWER must be supplied to the module
  - Apply 3.3V to 5.5V to these pins
  - Current draw is 50mA to 400 mA

### DIO Functionality

- **MODE0** and MODE2 states are latched pins on
  - OFF_BD_RESET# disasserted

- **MODE0** and MODE2 have PC2 locations
  - MODE0 and MODE2 states are latched pins on
  - OFF_BD_RESET# disasserted

- **DIO_00 to DIO_16**

#### Console

- **DIO_15 PB12**
  - **PB23**
  - **PB20**
  - **PB13**
  - **PB9**
  - **PB8**
  - **PB7**
  - **PB1**
  - **PB1**
  - **PB1**
  - **PB1**

#### CPU JTAG

- **CPU_JTAG_TDI**
  - **CPU_JTAG_TDO**
  - **CPU_JTAG_TCK**

#### SPI

- **SPI_MISO**
  - **SPI_MOSI**
  - **SP1_DAT**
  - **SP1_CLK**

#### USB Ports

- **EN_USB_5V**
  - **EXT_RESET#**

#### Ethernet

- **ETH_RX-**
  - **ETH_TX+**
  - **ETH_TX+**
  - **ETH_RX-**

### Power Supply

- **3.3V max load is 300 mA**
- **1.8V, 1.5V and 1.0V pins is 10 mA each**

### I/O Switching

- **10 nF C132**
- **- MUX_AD[00: 15]**
  - **MUX_AD08 thru 15**

### Device Information

- **PC4, PC5, PC6**
  - **PC7, PC8, PC9**
  - **PC10, PC13, PC14**

### ESD Protection

- **Any I/O routed to a user accessible connector should have additional ESD protection placed on the carrier board.**

### 8-bit Bus

- **Bus cycles use 11 address lines**
  - **AD9 thru AD0**
  - **This provides 1K-address space**
  - **for 8-bit bus cycles (000-3FF)**
  - **and 1K for 16-bit cycles (400-7FF)**

### Footnote

- **Pin 1 is the top left corner pin on the connector. All of the pins on the left are odd numbered. This may differ from the connector manufacturer’s datasheet.**

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**Title:** TS-4200 Off-board Connectors
**Date:** March 22, 2015
**Rev:** E **Designer:** Sheet 8 of 8