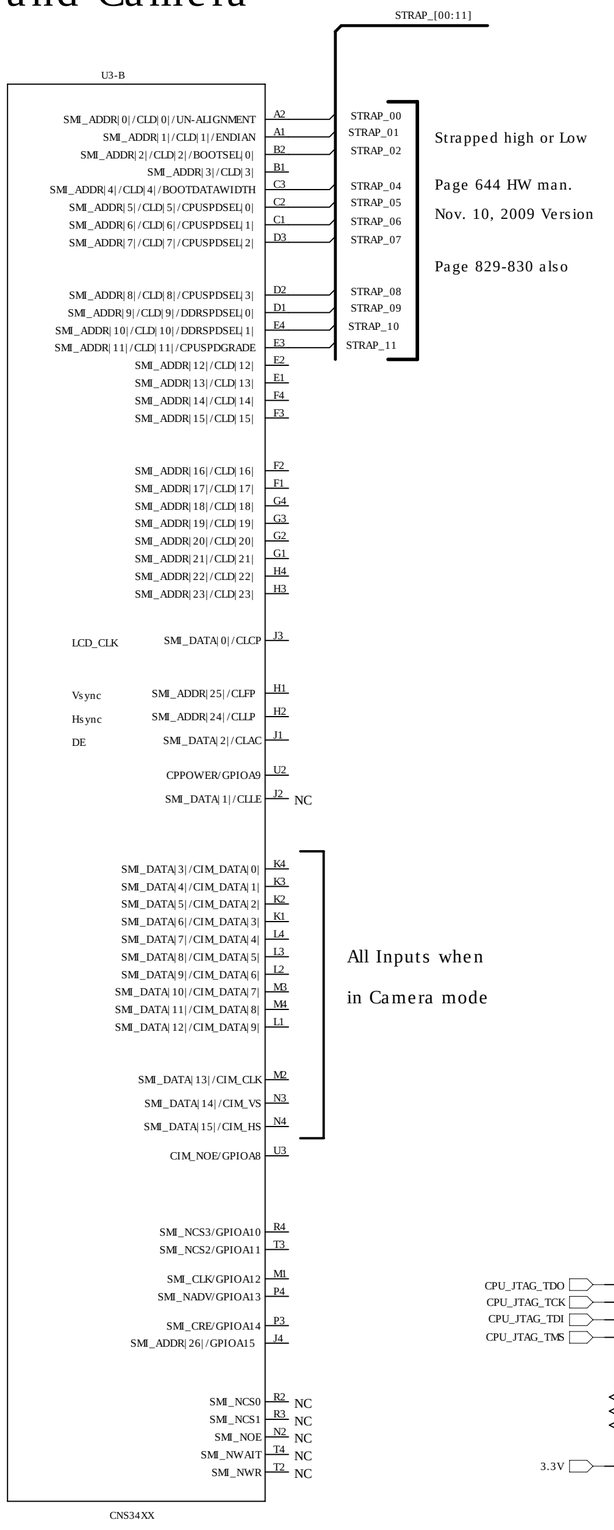
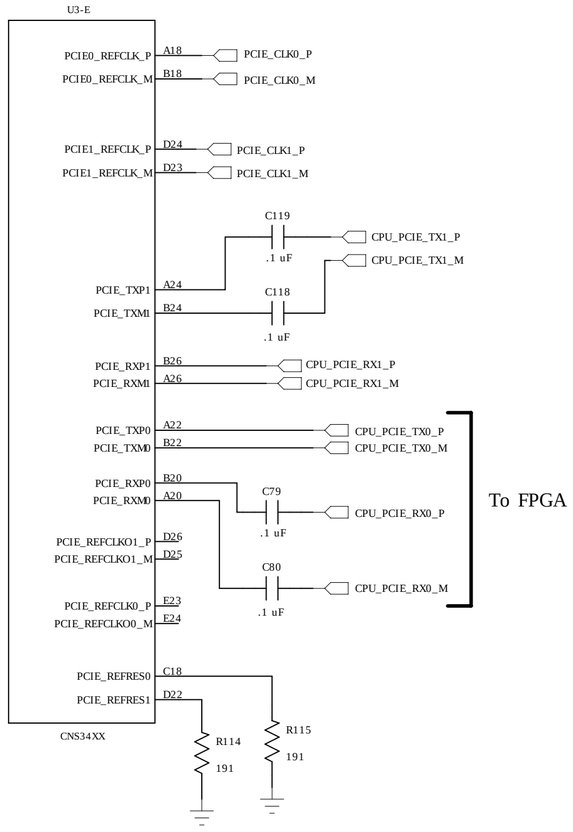
Cavium ARM11 CPU

LCD

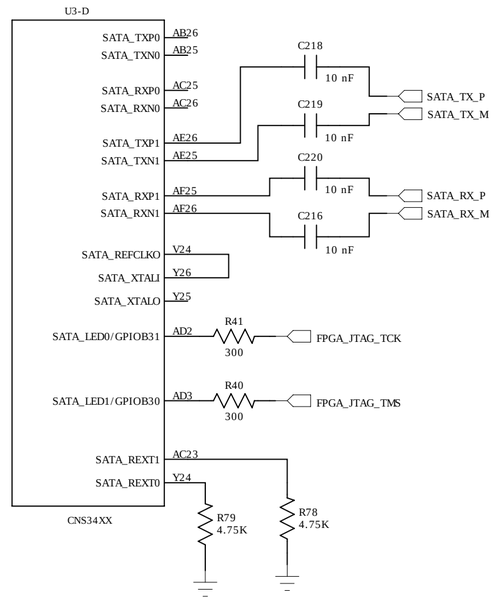
and Camera



PCI Ex.

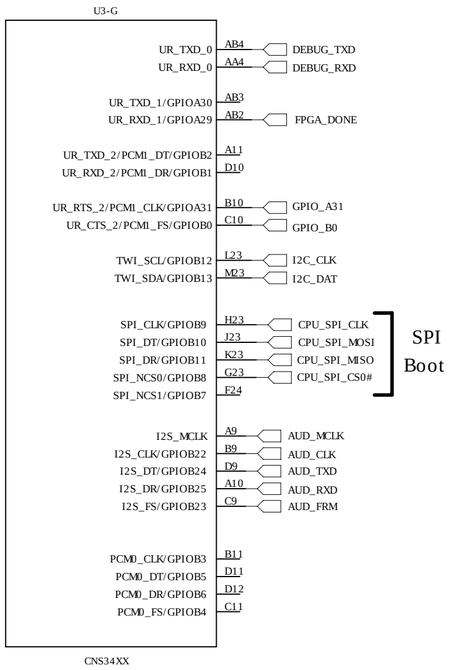


SATA

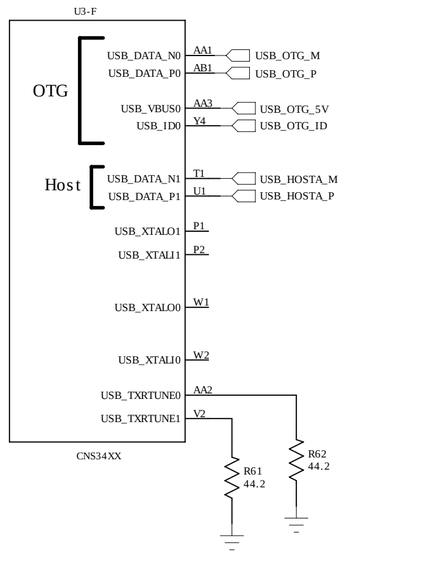


UARTs, SPI

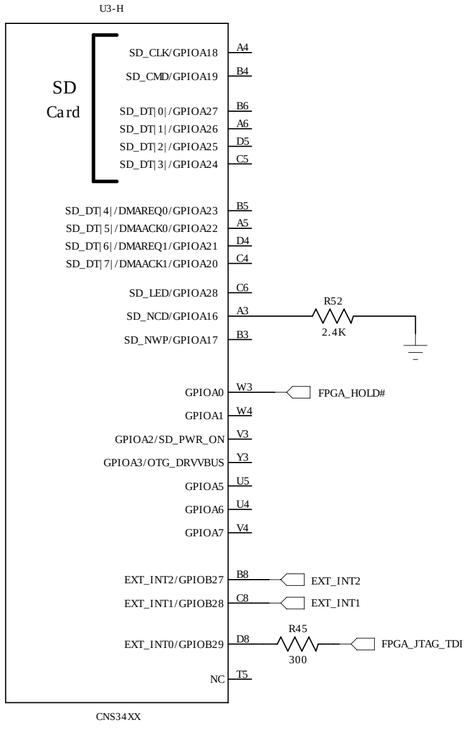
I2C, Audio



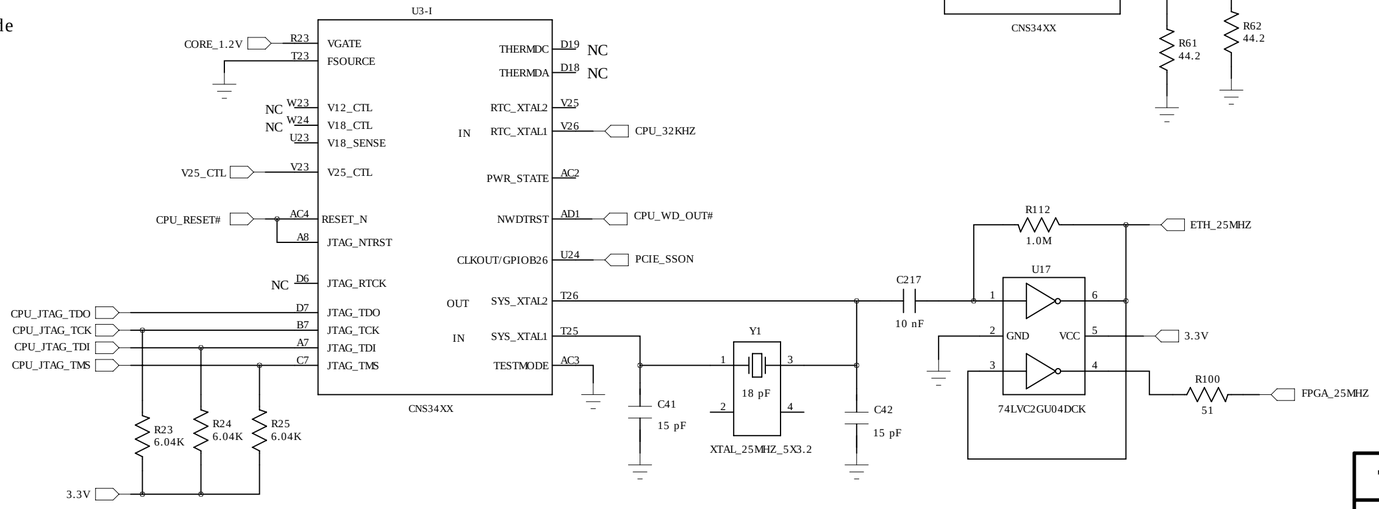
USB



SD Card

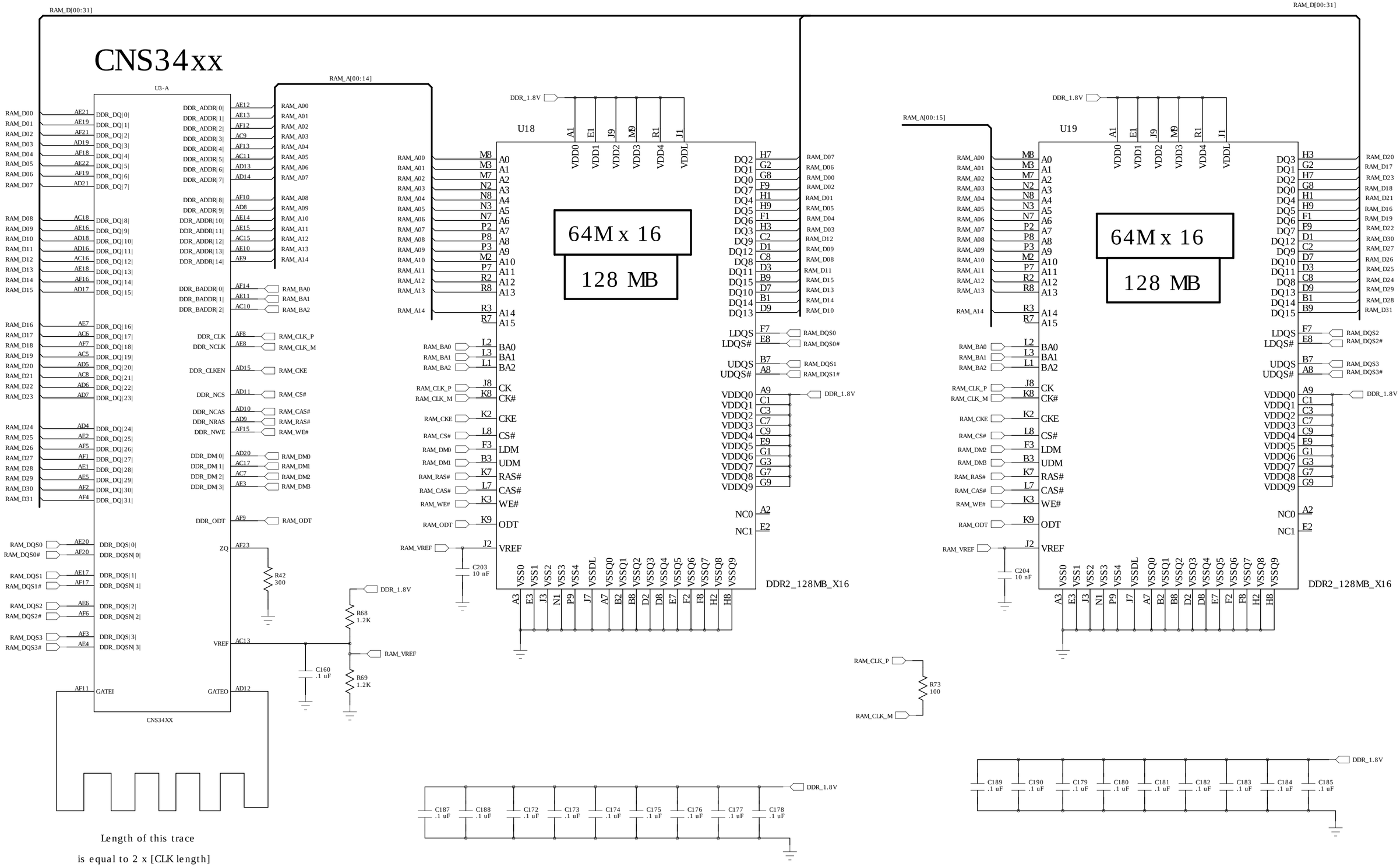


Control



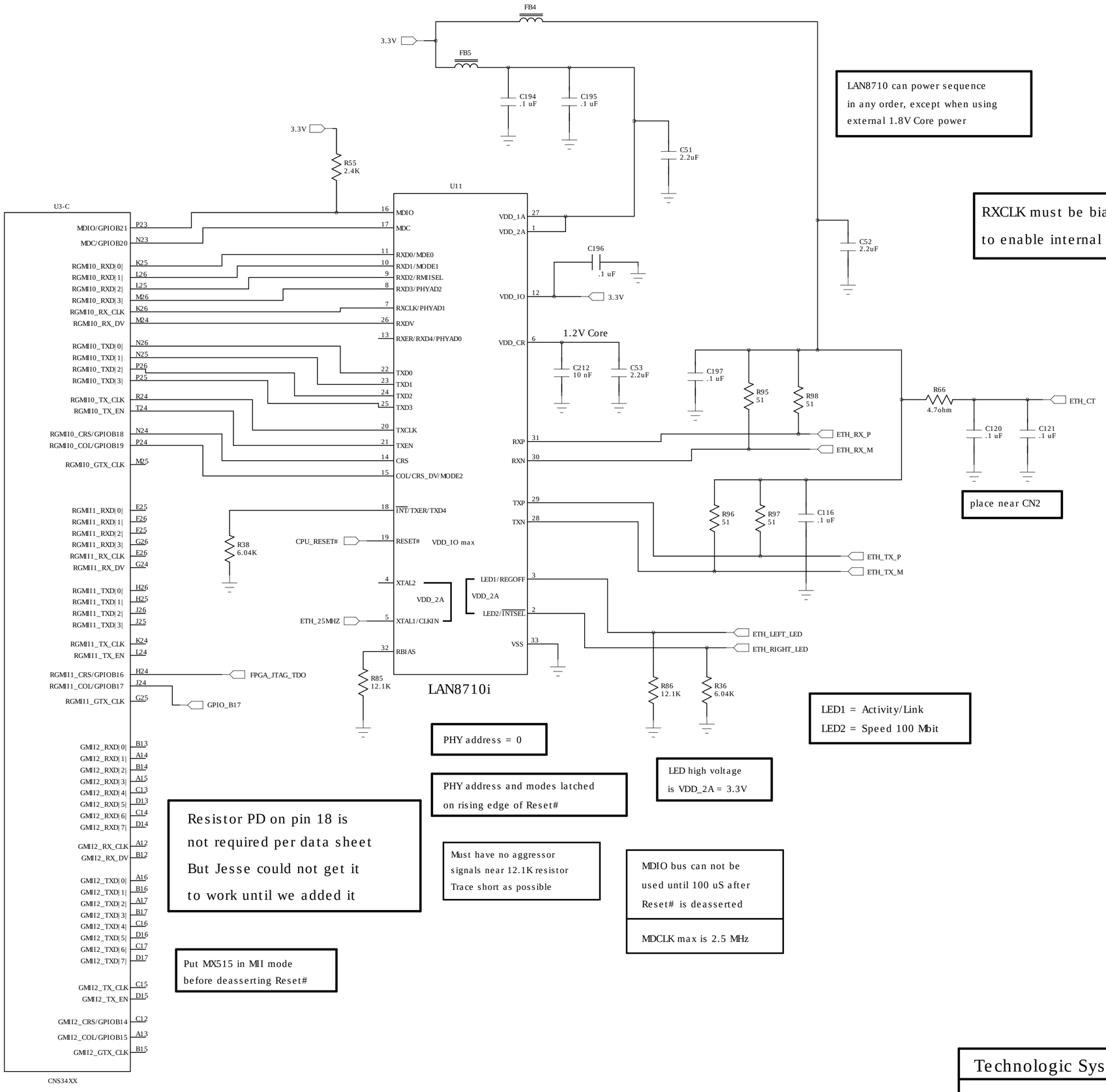
Technologic Systems	Date July 24, 2012	
Title: TS-4300 CPU		
Rev: B	Designer	Sheet 1 of 10

DDR2 SDRAM (256 MByte)



Technologic Systems	Date July 24, 2012	
Title: TS-4300 DDR2 RAM		
Rev: B	Designer	Sheet 2 of 10

10/100 Ethernet

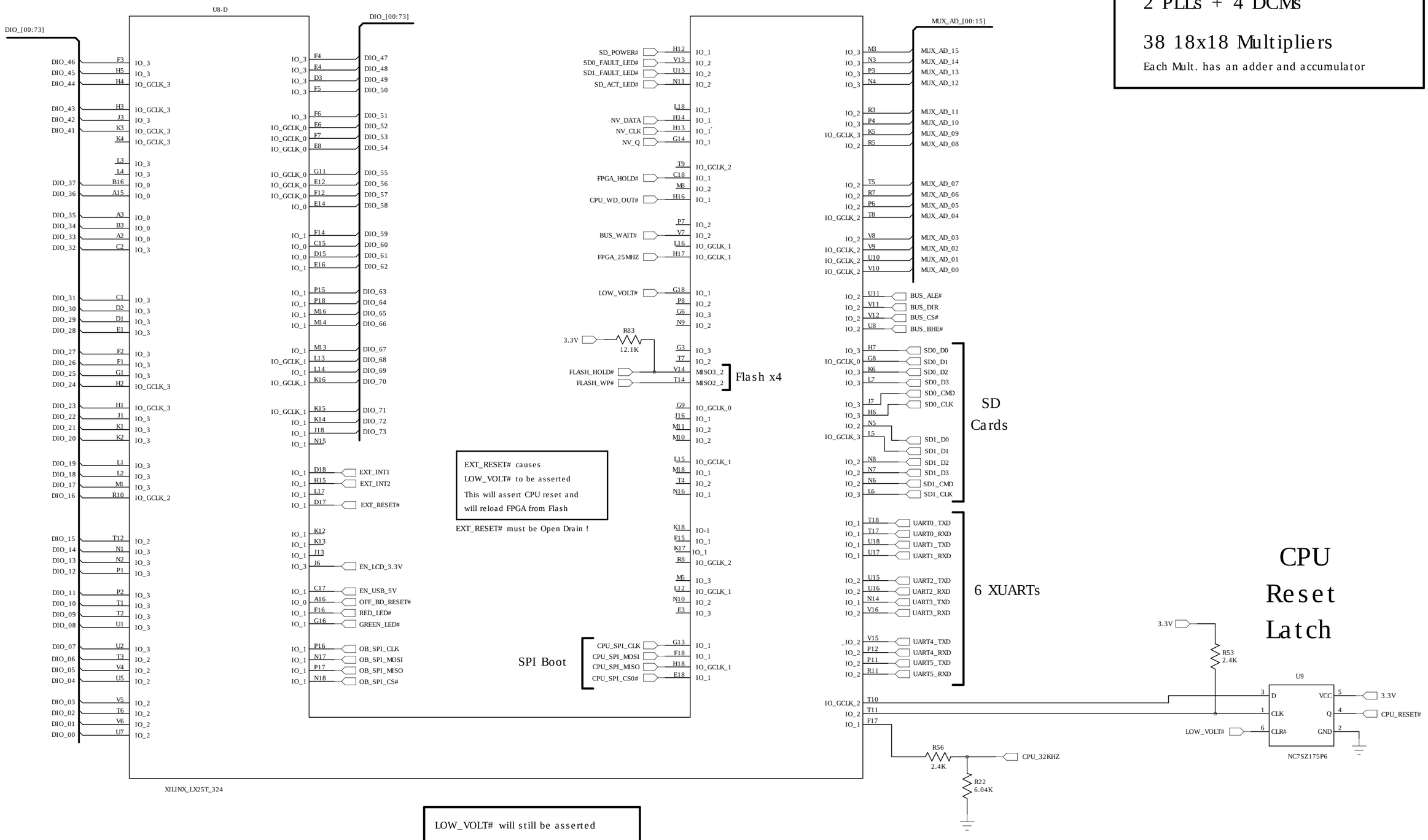


Technologic Systems	Date July 24, 2012	
Title: TS-4300 Ethernet		
Rev: B	Designer RLM	Sheet 3 of 10

Xilinx LX25T_324 FPGA

- 25K equivalent LUTs
- 15K 6-input LUTs
- 30K Flip-flops
- 52 [2K x 9] Block RAM
- 2 PLLs + 4 DCMs
- 38 18x18 Multipliers

Each Mult. has an adder and accumulator



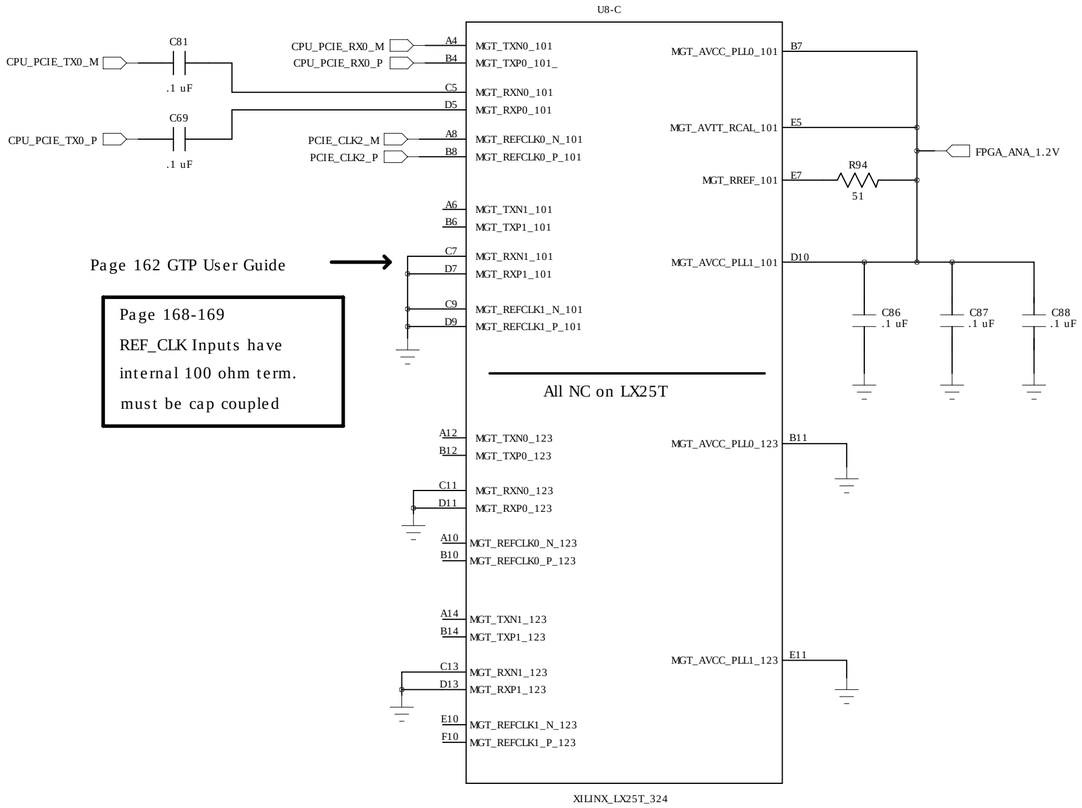
LOW_VOLT# will still be asserted
after FPGA is configured
and can be used as a FPGA reset

FPGA_HOLD# is driven by CPU and
can be used as a FPGA reset when
CPU is doing a soft FPGA reload

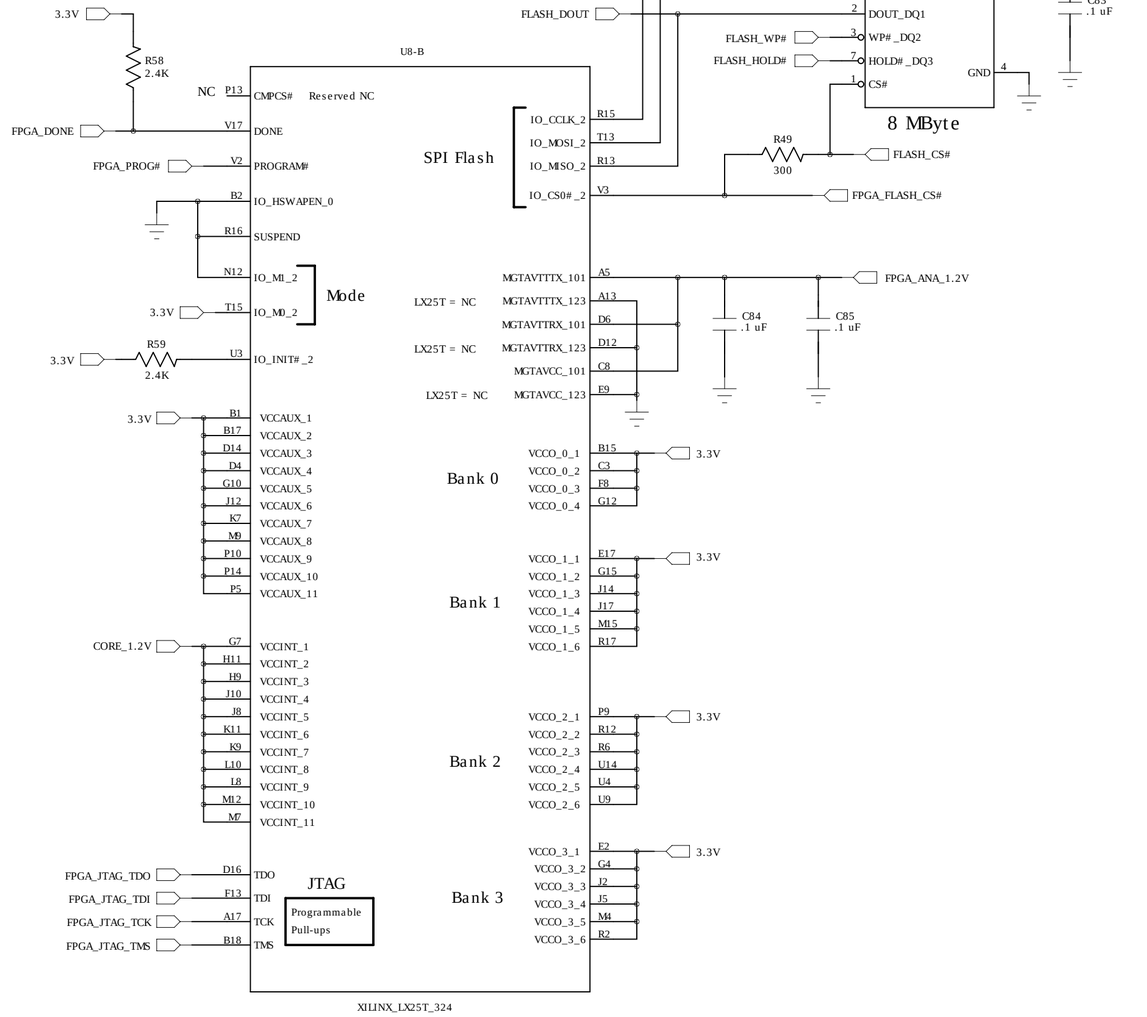
Technologic Systems	Date July 24, 2012	
Title: TS-4300 FPGA		
Rev: B	Designer	Sheet 4 of 10

Xilinx LX25T_324 FPGA

Gigabit Transceivers



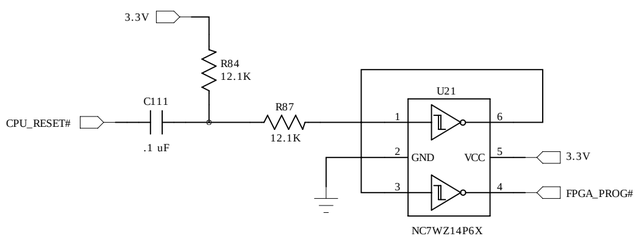
Power and Special Functions

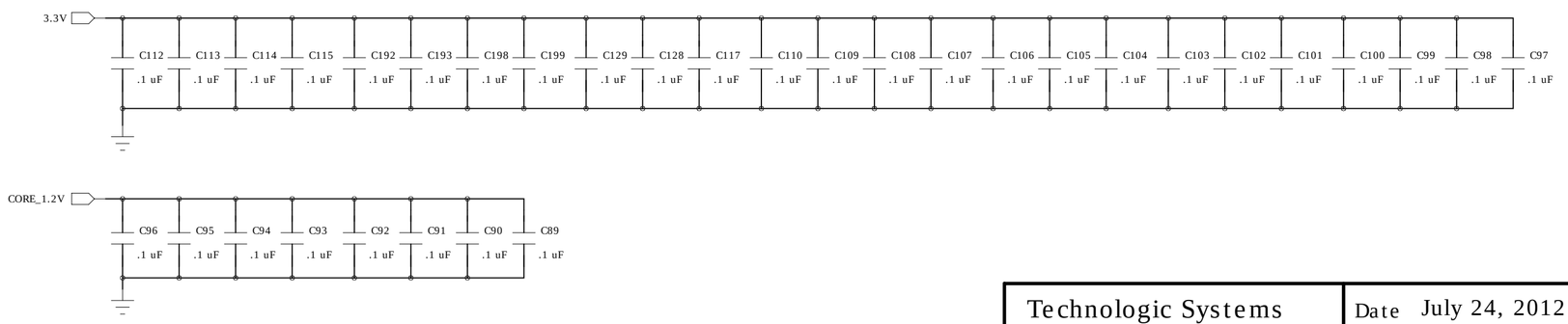


8MB SPI Flash

64 bytes of OTP

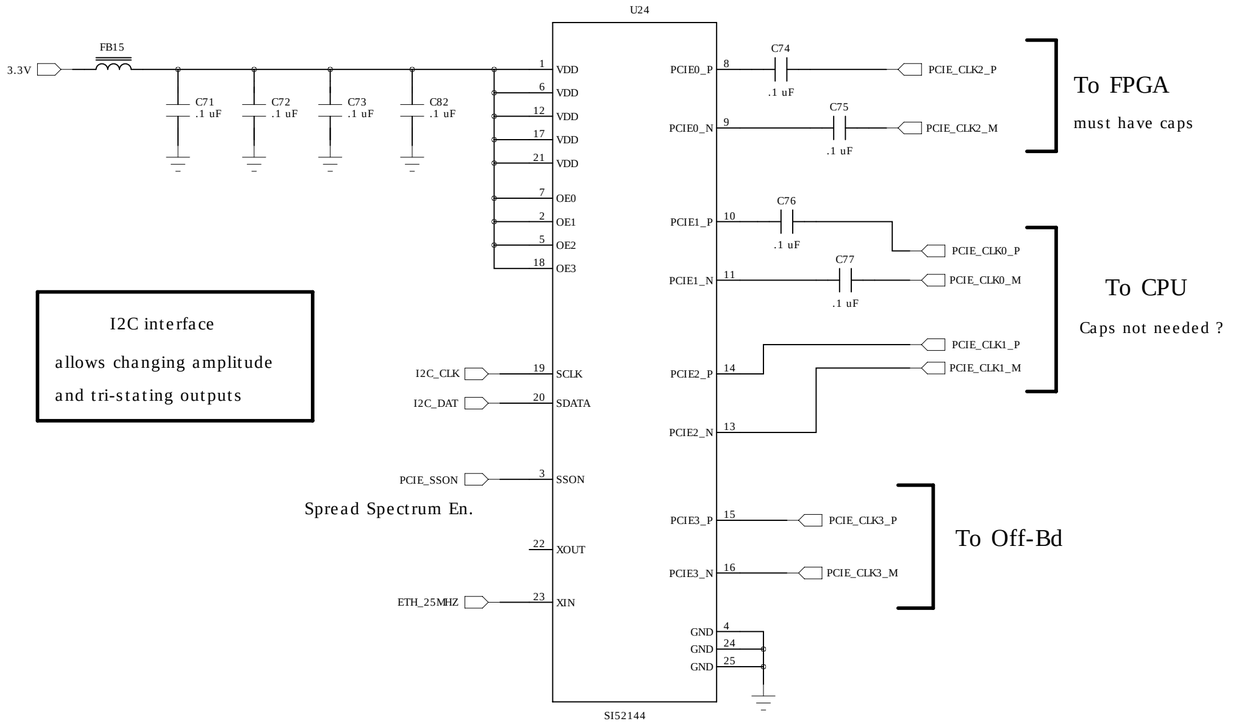
FPGA Reload





Technologic Systems	Date July 24, 2012	
Title: TS-4300 FPGA		
Rev: B	Designer	Sheet 5 of 10

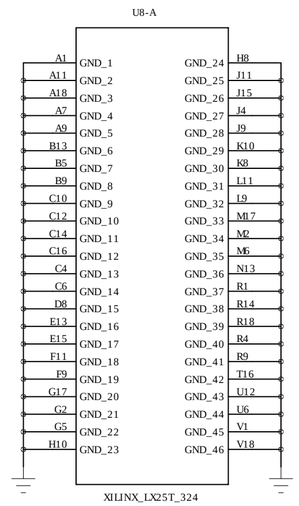
PCIe 100 MHz Clock Generator



I2C interface
allows changing amplitude
and tri-stating outputs

Spread Spectrum En.

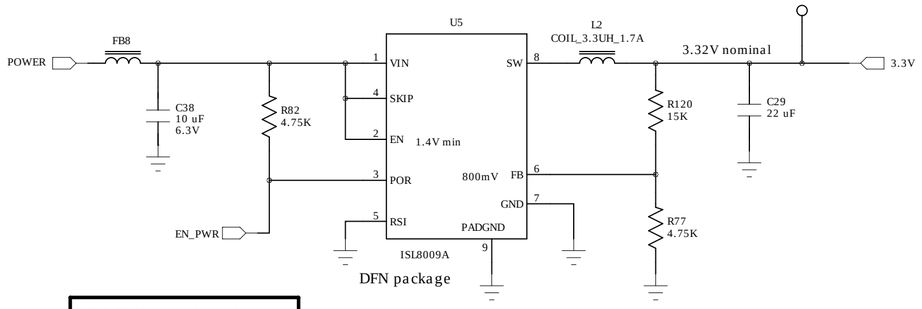
FPGA GND



Technologic Systems		Date July 24, 2012
Title: TS-4300 PCIe Clock generator		
Rev: B	Designer	Sheet 6 of 10

3.3V Power Supply

up to 1500 mA



EN_PWR goes low when
3.3V out of regulation

Coil = LQH44PN3R3

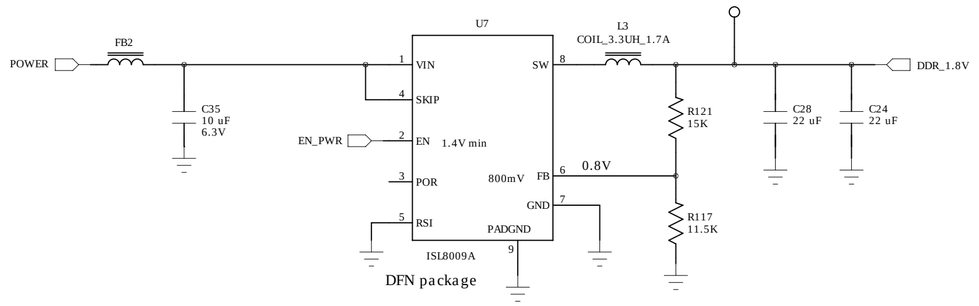
Max. current = 1.7 Amps

Power Sequence

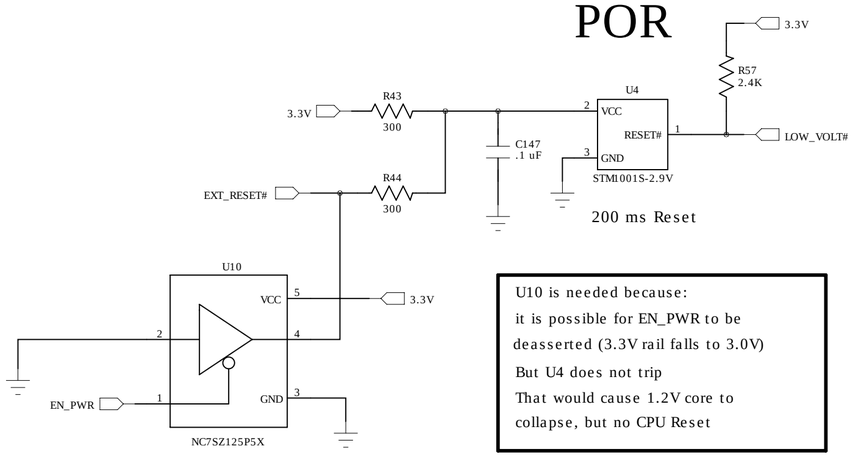
3.3V rail comes up first

Then about 1 mS later
The Core_1.2V and the
1.8V rail come up together

1.8V DDR2 Power Supply



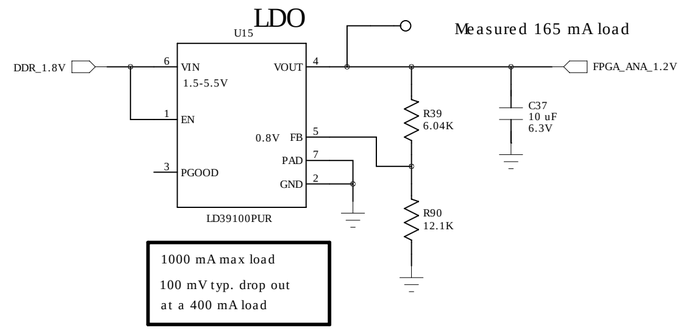
POR



U10 is needed because:
it is possible for EN_PWR to be deasserted (3.3V rail falls to 3.0V)
But U4 does not trip
That would cause 1.2V core to collapse, but no CPU Reset

FPGA Analog 1.2V Reg.

LDO

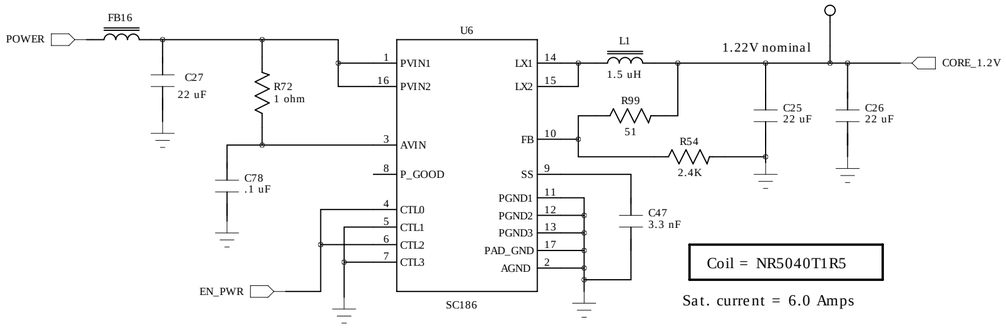


1000 mA max load
100 mV typ. drop out
at a 400 mA load

GND Test Point

1.2V Power Supply

up to 4000 mA

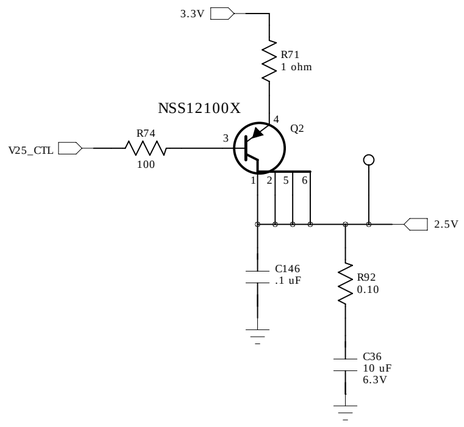


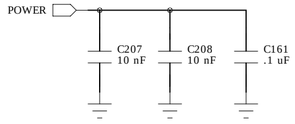
Coil = NR5040T1R5

Sat. current = 6.0 Amps

1.5 MHz sw. freq.

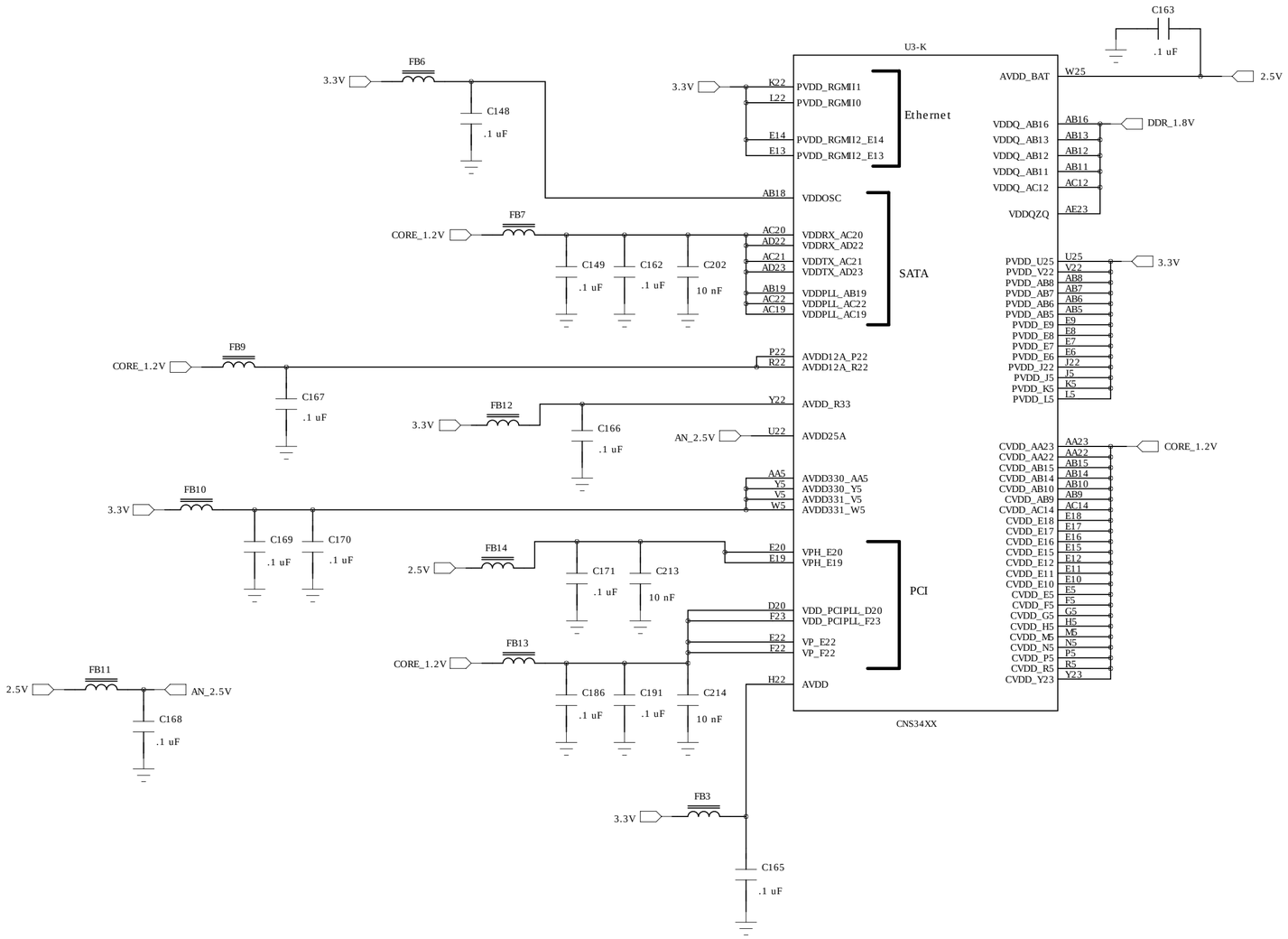
2.5V Power Supply

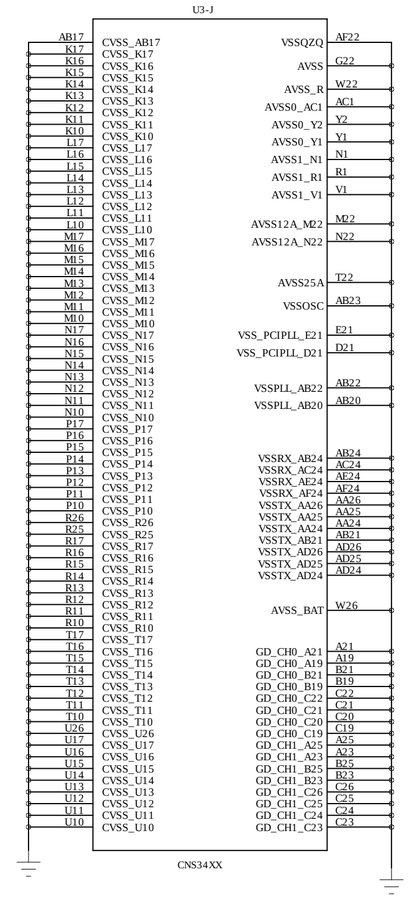


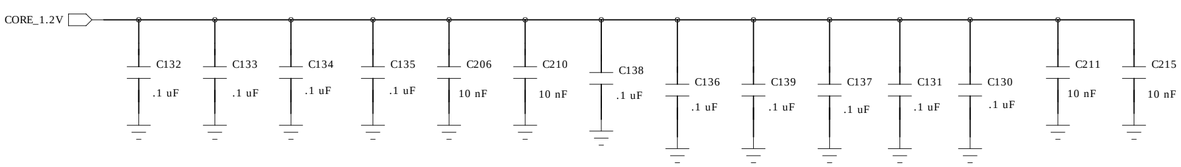


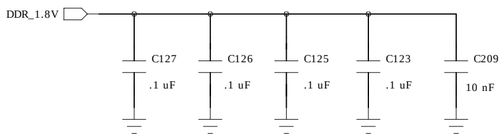
Technologic Systems		Date July 24, 2012
Title: TS-4300 Power Supply Rails		
Rev: B	Designer	Sheet 7 of 10

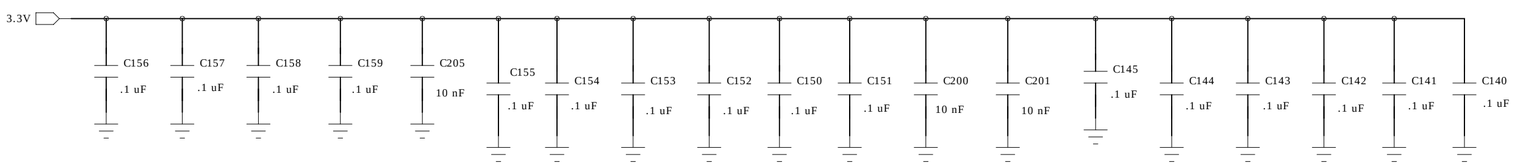
CPU Power





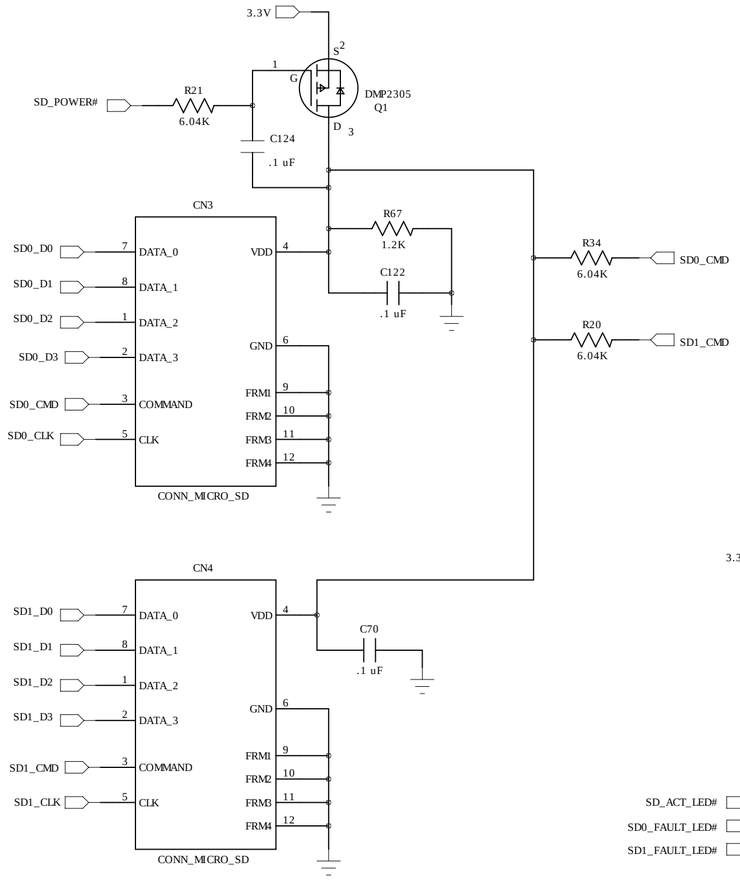




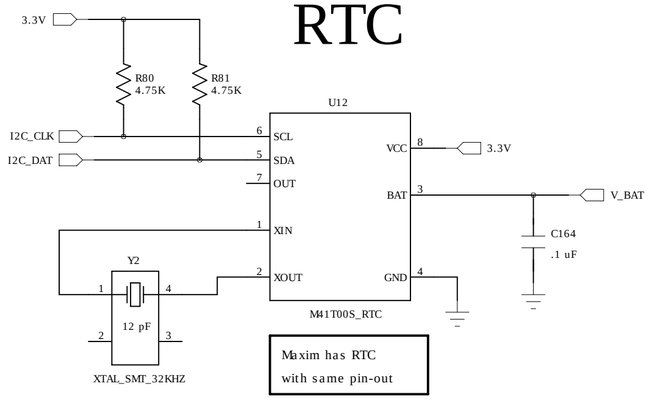


Technologic Systems		Date July 24, 2012
Title: TS-4300 CPU Power		
Rev: B	Designer	Sheet 8 of 10

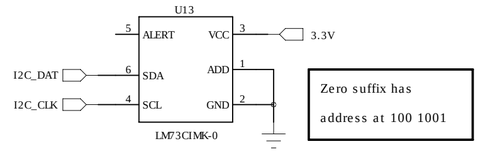
Micro SD Card Socket



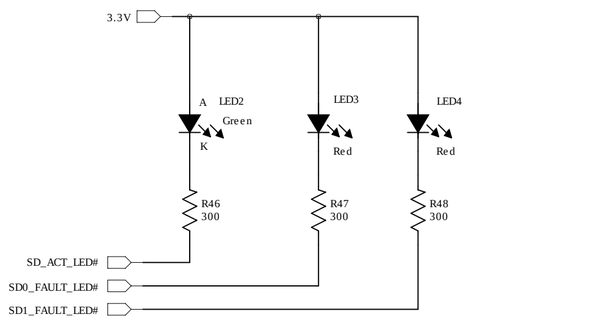
RTC

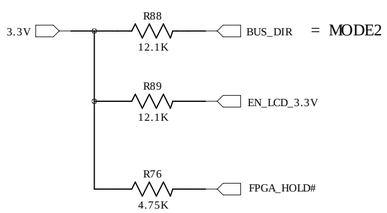


Temp Sensor

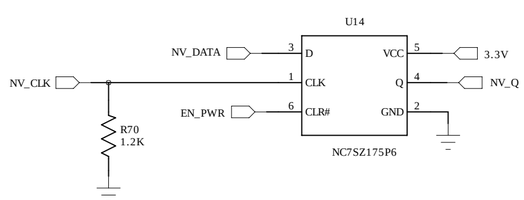


SD LEDs

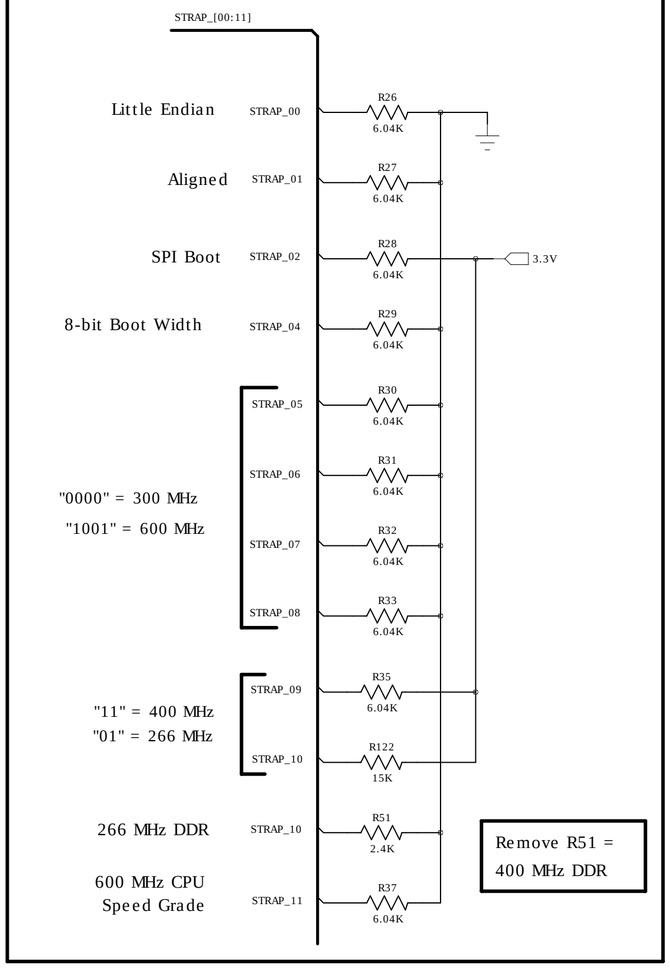




Reboot Flag



Boot Strap Bias Resistors



Technologic Systems	Date July 24, 2012	
Title: TS-4300 SD Card, Temp, RTC		
Rev: B	Designer	Sheet 9 of 10

Two 100-pin Off-board Connectors

"POWER" pins supply all power to the module
Apply 4.0V to 5.5V to these pins

OFF_BD_RESET# is an Output
used to reset all peripherals

EXT_RESET# is an Input
used to reboot the CPU

EXT_RESET# can
never be driven high
(use Open drain)

Left

CN1

FPGA JTAG: FPGA_JTAG_TMS 1, FPGA_JTAG_TCK 3, FPGA_JTAG_TDO 5, FPGA_JTAG_TDI 7, OFF_BD_RESET# 9

DIO_17 11, DIO_18 13

DIO_[00:73]: DIO_37 17, DIO_36 19, DIO_35 21, DIO_34 23, DIO_33 25, DIO_32 27, DIO_31 31, DIO_30 33, DIO_29 35, DIO_28 37, DIO_27 39, DIO_26 41, DIO_25 43, DIO_24 45, DIO_23 49, DIO_22 51, DIO_21 53, DIO_20 55, DIO_19 57, DIO_14 63, DIO_13 65, DIO_12 67, DIO_11 69, DIO_10 71, DIO_09 73, DIO_08 77, DIO_07 79, DIO_06 81, DIO_05 83, DIO_04 85, DIO_03 87, DIO_02 89, DIO_01 91, DIO_00 93

POWER 29

FLASH_CS# 59, FPGA_FLASH_CS# 61

BUS_WAIT# 97, BUS_BHE# 99

EXT_RESET# 2, EN_USB_5V 4

DIO_[00:73]: DIO_62 6, DIO_61 8, DIO_60 10, DIO_59 12, DIO_58 14, DIO_57 18, DIO_56 20, DIO_55 22, DIO_54 24, DIO_53 26, DIO_52 28, DIO_51 30, DIO_50 32, DIO_49 34, DIO_48 38, DIO_47 40, DIO_46 42, DIO_45 44, DIO_44 46, DIO_43 50, DIO_42 52, DIO_41 54

POWER 16, V_BAT 36, EN_LCD_3.3V 48

FLASH_DOUT 56, FLASH_DIN 58, FLASH_CLK 60

MUX_AD_[00:15]: MUX_AD_15 64, MUX_AD_14 66, MUX_AD_13 68, MUX_AD_12 70, MUX_AD_11 72, MUX_AD_10 74, MUX_AD_09 76, MUX_AD_08 78, MUX_AD_07 80, MUX_AD_06 82, MUX_AD_05 84, MUX_AD_04 86, MUX_AD_03 88, MUX_AD_02 90, MUX_AD_01 92, MUX_AD_00 94

BUS_ALE# 96, BUS_DIR 98, BUS_CS# 100

Data Bus or DIO

TYCO_100PIN_MODULE

Bus Control

Must have 10 nF Capacitor
very near CN2 and GND
for all "quiet" signals
(between diff pairs)

3.3V rail can supply up
to 700 mA to base board

Maximum off-board load
on CORE_1.2V and 2.5V
is 10 mA each

Maximum off-board load
on DDR_1.8V is 100 mA

CN2-79 = CPU JTAG_Vcc

Right

CN2

Ethernet: ETH_RX_P 1, ETH_RX_M 3, ETH_CT 5, ETH_TX_P 7, ETH_TX_M 9, ETH_CT 11, 3.3V 13

SATA_RX_M 17, SATA_RX_P 19

NC 23, NC 25, NC 27

USB Ports: USB_HOSTA_M 29, USB_HOSTA_P 31, CORE_1.2V 33, USB_OTG_M 35, USB_OTG_P 37, 3.3V 39, SATA_TX_M 41, SATA_TX_P 43

CPU_PCIE_TX1_M 47, CPU_PCIE_TX1_P 49

CPU_PCIE_RX1_M 53, CPU_PCIE_RX1_P 55, DDR_1.8V 57, PCIE_CLK3_M 59, PCIE_CLK3_P 61, 2.5V 63

SPI: OB_SPI_CS# 65, OB_SPI_MOSI 67, OB_SPI_MISO 69, OB_SPI_CLK 71

3.3V 79

Console: DEBUG_TXD 93, DEBUG_RXD 95

CAN or DIO: DIO_15 97, DIO_16 99

ETH_LEFT_LED 2, ETH_RIGHT_LED 4, RED_LED# 6, GREEN_LED# 8

CPU DIO: GPIO_A31 10, GPIO_B0 12

A/D

I2C or DIO: I2C_CLK 28, I2C_DAT 30, GPIO_B17 32

I2S or DIO: AUD_MCLK 34, AUD_CLK 36, AUD_FRM 38, AUD_TXD 40, AUD_RXD 42

CPU JTAG: CPU_JTAG_TMS 44, CPU_JTAG_TCK 46, CPU_JTAG_TDI 48, CPU_JTAG_TDO 50

DIO_[00:73]: DIO_73 52, DIO_72 54, DIO_71 56, DIO_70 58, DIO_69 60, DIO_68 62, DIO_67 64, DIO_66 66, DIO_65 68, DIO_64 70, DIO_63 72

USB_OTG_ID 74, USB_OTG_5V 76

Serial Ports or DIO: UART0_TXD 78, UART0_RXD 80, UART1_TXD 82, UART1_RXD 84, UART2_TXD 86, UART2_RXD 88, UART3_TXD 90, UART3_RXD 92, UART4_TXD 94, UART4_RXD 96, UART5_TXD 98, UART5_RXD 100

TYCO_100PIN_MODULE

DIO_15 and DIO_16
can be CAN_TXD
and CAN_RXD

Boot Strap

Mode 2	TS-4300 Boots from
1	SD Card
0	SD Card

BUS_DIR is latched prior to
OFF_BD_RESET# deasserted

Connect 1.5K ohm resistor
between BUS_DIR and
OFF_BD_RESET# to set low
(Boot from SD card)

BUS_DIR = MODE2

If Bus is not needed, all Bus
signals can be changed to DIO

Devices connected to this bus must never
drive it when BUS_CS# is deasserted
(must be off within 30 nS of deassertion)

Devices must pull the BUS_WAIT# line low
if they need more than 150 nS strobe

The data bus can not have more than
30 pF of off-board capacitive loading
May need data buffer chip for heavy loads

Technologic Systems	Date July 24, 2012	
Title: TS-4300 Off-board Connectors		
Rev: B	Designer	Sheet 10 of 10