LAN8710 must be biased low to enable internal 1.8V reg.

Resistor PD on pin 18 is not required per data sheet
But Jesse could not get it to work until we added it

PHY address = 0
PHY address and modes latched on rising edge of Reset#

LED1 = Activity/Link
LED2 = Speed 100 Mbit

Reset# must have no aggressor signals near 12.1K resistor
Place short as possible

RXCLK must be biased low to enable internal 1.8V reg.

LAN8710 can power sequence in any order, except when using external 1.8V Core power
Xilinx LX25T_324 FPGA

- 25K equivalent LUTs
- 15K 6-input LUTs
- 30K Flip-flops
- 52 [2K x 9] Block RAM
- 2 PLLs + 4 DCMs
- 38 18x18 Multipliers

Each Mult. has an adder and accumulator
Xilinx LX25T_324 FPGA

Gigabit Transceivers

FPGA Reload

Power and Special Functions

8MB SPI Flash

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REF_CLK Inputs have internal 100 ohm term. must be cap coupled

CORE_1.2V

FPGA_JTAG_TDI

FPGA_JTAG_TDO

FPGA_JTAG_TMS

FPGA_JTAG_TCK

FPGA_PROG#

CPU_PCIE_TX0_P

PCIE_CLK2_P

PCIE_CLK2_M

CPU_PCIE_RX0_M

CPU_PCIE_RX0_P

CORE_1.2V

FPGA_ANA_1.2V

FPGA_ANA_1.2V

FPGA_PROG#

FPGA_ANA_1.2V

FPGA_PROG#

FPGA_ANA_1.2V
PCIe 100 MHz
Clock Generator

To FPGA
must have caps

To CPU
Caps not needed?

To Off-Bd

12C interface
allows changing amplitude
and tri-stating outputs

Spread Spectrum En.
### 3.3V Power Supply

- **Power Sequence**
  - 3.3V rail comes up first
  - Then about 1 ms later
  - Core_1.2V and the 1.8V rail come up together

- **POR**
  - U10 is needed because it is possible for EN_PWR to be deasserted (3.3V rail falls to 3.0V)
  - But U4 does not trip
  - That would cause 1.2V core to collapse, but no CPU Reset

### 1.2V Power Supply

- **EN_PWR** goes low when 3.3V out of regulation

### 1.8V DDR2 Power Supply

### 2.5V Power Supply

- **FPGA Analog 1.2V Reg.**
  - Measured 165 mA load
  - 1000 mA max load
  - 100 mA Vccp deep out at 400 mA load

- **GND Test Point**
Two 100-pin Off-board Connectors

“POWER” pins supply all power to the module
Apply 4.0V to 5.5V to these pins

“POWER” pins supply all power to the module
Apply 4.0V to 5.5V to these pins

EXT_RESET# is an input needed to reset the CPU

EXT_RESET# is an Output needed to reset all peripherals

OFF_BD_RESET# is an Output needed to reset all peripherals

Bus Control

If Bus is not needed, all Bus signals can be changed to DIO

Devices connected to this bus must never drive it when BUS_CD# is deasserted
(must be off within 50 nS of deassertion)

Devices must pull the BUS_WAIT# line low if they need more than 150 nS strobs

The data bus cannot have more than 30 pF of off-board capacitive loading
May need data buffer chip for heavy loads

If the bus is not needed, all bus signals can be changed to DIO

SPI

USB Ports

Console

CAN or DIO

SPI

CAN or DIO

USB Ports

Console

GND

V_BAT

POWER

Data Bus or DIO

Bus Control

Left

Right

Ethernet

USB

I2C or DIO

I2S or DIO

CPU

CPU JTAG

Serial Ports or DIO

Two 100-pin Off-board Connectors

FPGA

JTAG

FPGA JTAG

FPGA_JTAG_TDO

FPGA_JTAG_TMS

FPGA_JTAG_TDI

BUS_WAIT#

BUS_BHE#

BUS_DIR = MODE2

BUS_DIR is latched prior to OFF_BD_RESET# deasserted

Bus Control

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Technologic Systems

July 24, 2012

Title: TS-4300 Off-board Connectors

Rev: B

Designer

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