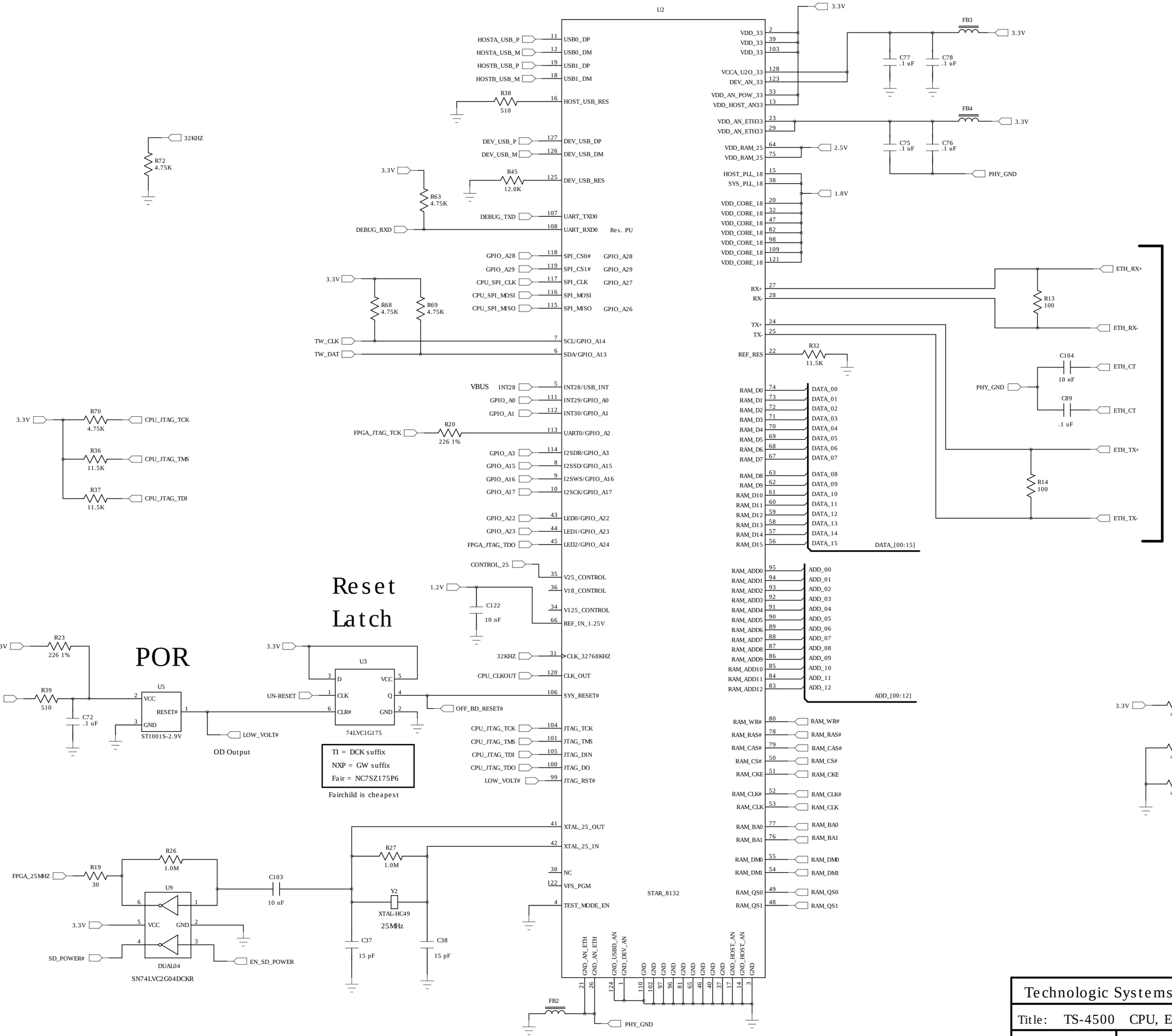


Technologic Systems	Date March 10, 2010	
Title: TS-4500 CPU, Ethernet, POR		
Rev:	Designer	Sheet 1 of 5

FPGA with 5000 LUTs

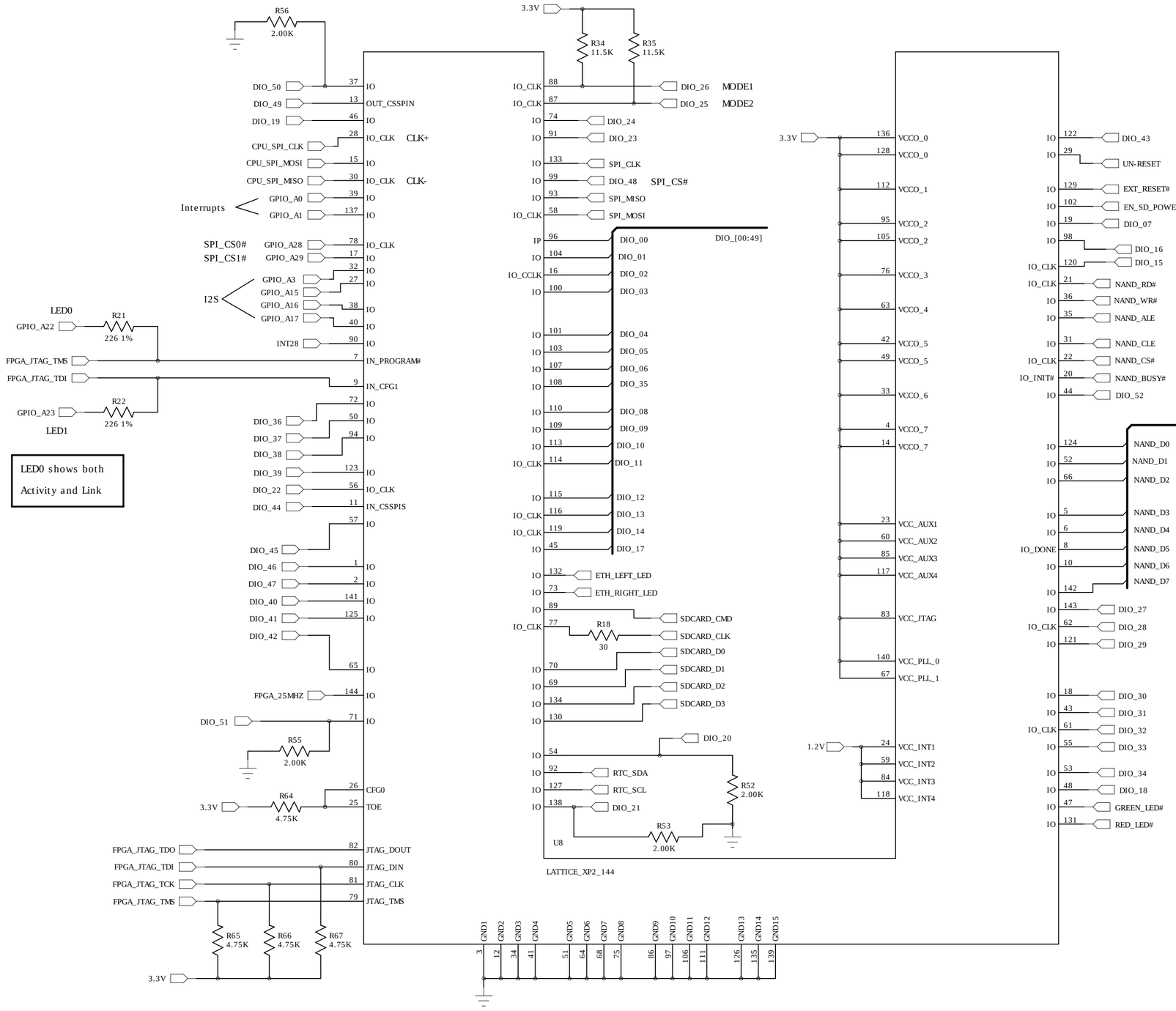
XP2-5 has:
5K LUTS 2 PLLs
9 blocks of 1Kx18 Block RAM
12 18x18 Multipliers
100 I/O with 144 pin package
"instant ON" = about 1.5 mS
input PLL clock = 10 MHz min

Boot Straps

Mode 2	Boots from
1	NAND Flash
0	SD Card

MODE1 and MODE2 states and Board ID bits are latched prior to UN_RESET# pulsed

MODE1 and MODE2 have PU resistors



LED0 shows both Activity and Link

UN-RESET rising edge, deasserts CPU Reset
(Must be careful at start up)
It has a PD resistor -- always idle low

EN_SD_POWER should initialize high

During JTAG Flash programming
the PROGRAM# pin should be high
else it can inhibit Flash --> SRAM

DONE likewise must be high
These do have weak PU resistors

Set CONFIG_MODE to NONE
This allows all pins to be used

Pull-up and pull-down resistors
are 6 to 30K ohms

PROGRAM#, DONE, and INIT# are dedicated configuration pins when CFG0 is low. When CFG0 is high they are "general purpose I/O"

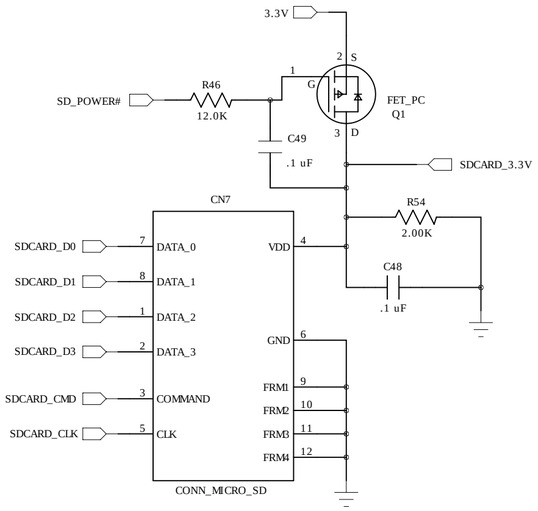
Page 4 of TN1141

Page 37 of Data Sheet (Hot Socketing)
Power Supplies can be sequenced in any order but must be monotonic

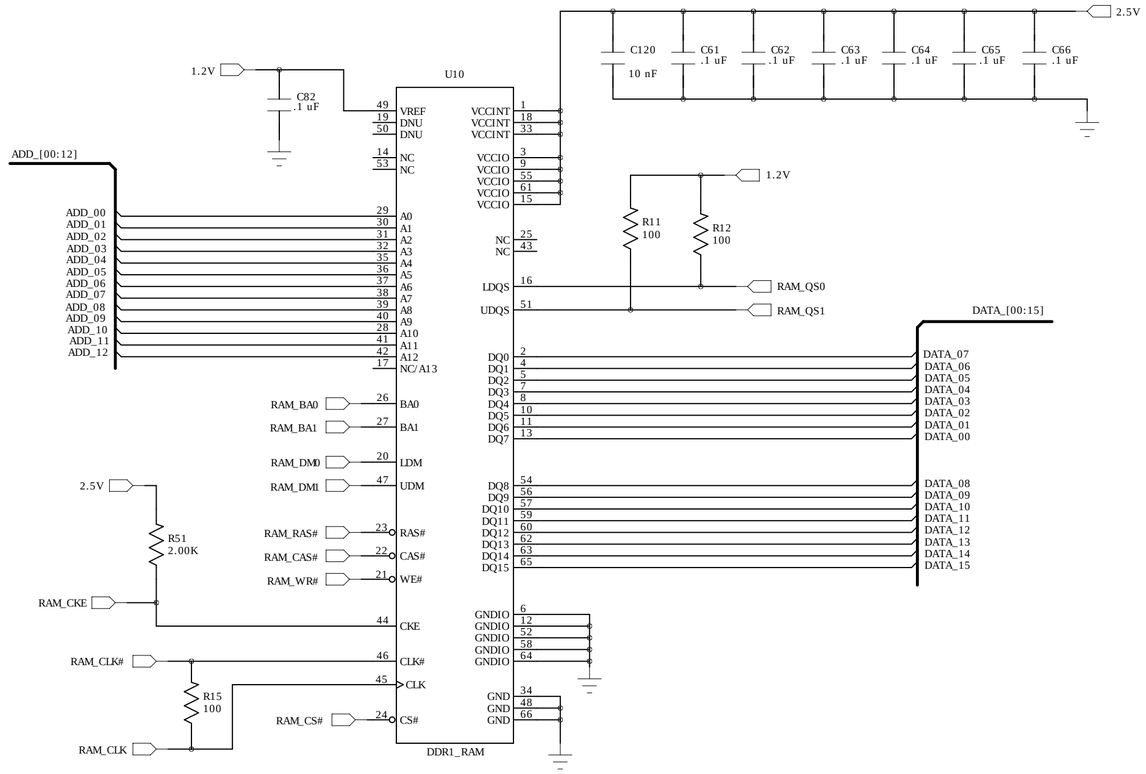
All I/O lines are tri-stated during power cycling

Technologic Systems		Date March 10, 2010
Title: TS-4500 FPGA		
Rev:	Designer RLM	Sheet 2 of 5

Micro SD Card Socket

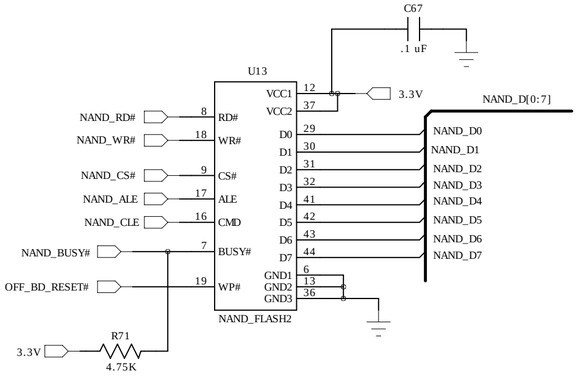


64 Mbyte
DDR1 SDRAM

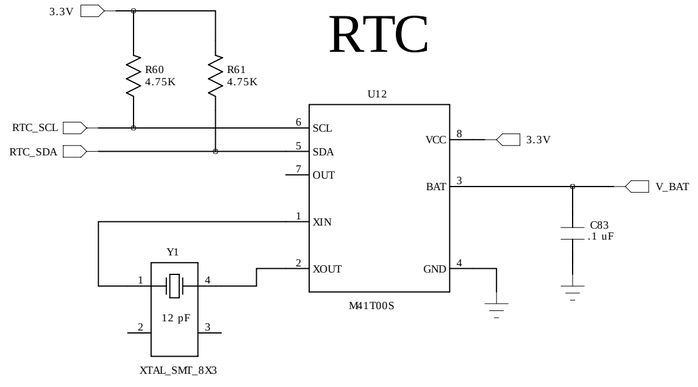


512 Mbyte or 2GB

NAND Flash

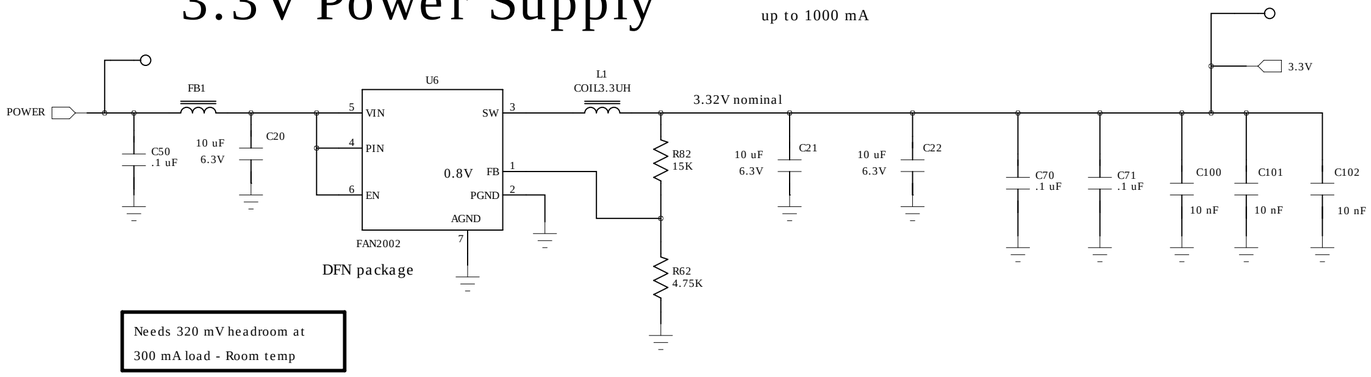


RTC

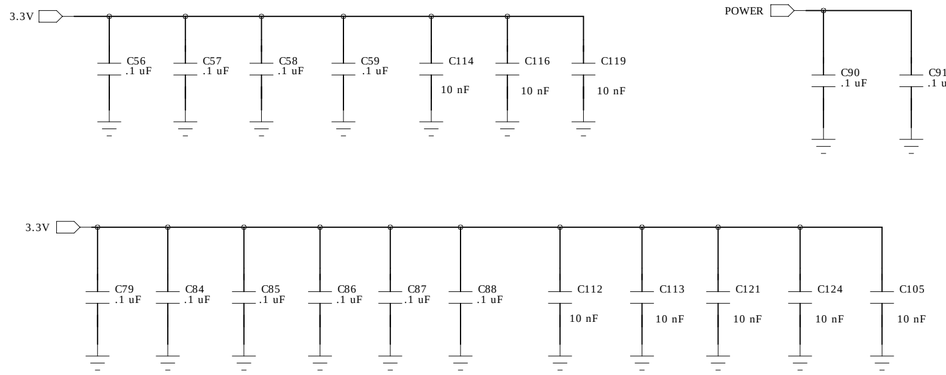


Technologic Systems		Date March 10, 2010
Title: TS-4500 RAM, RTC, Flash, SD socket		
Rev:	Designer	Sheet 3 of 5

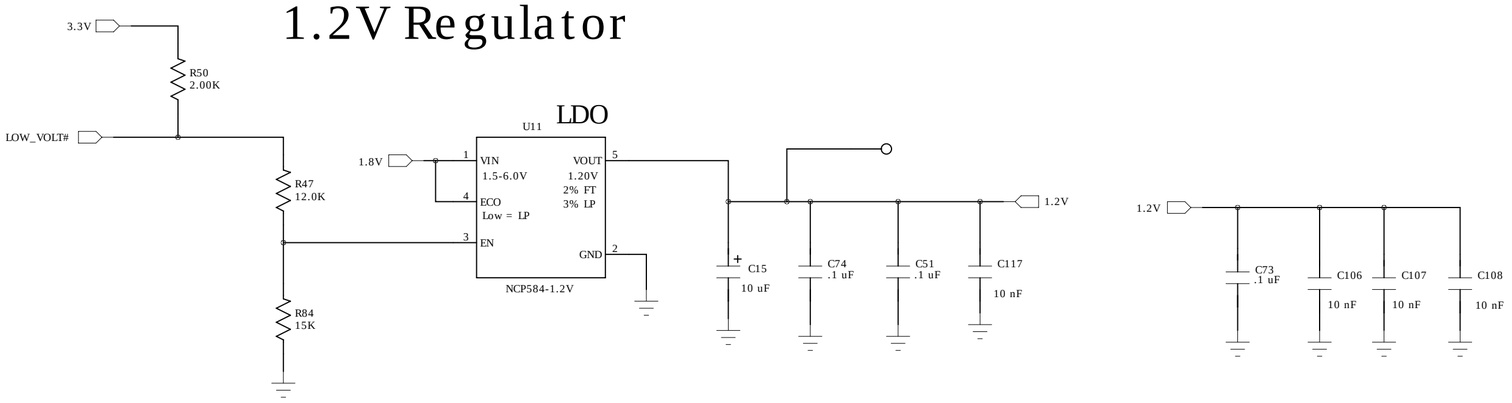
3.3V Power Supply



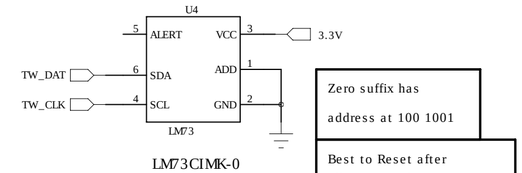
Needs 320 mV headroom at
300 mA load - Room temp



1.2V Regulator



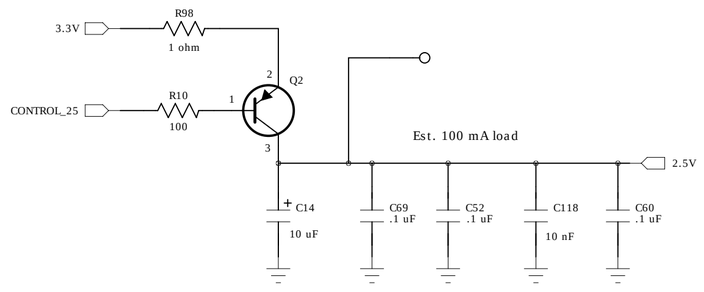
Temp Sensor



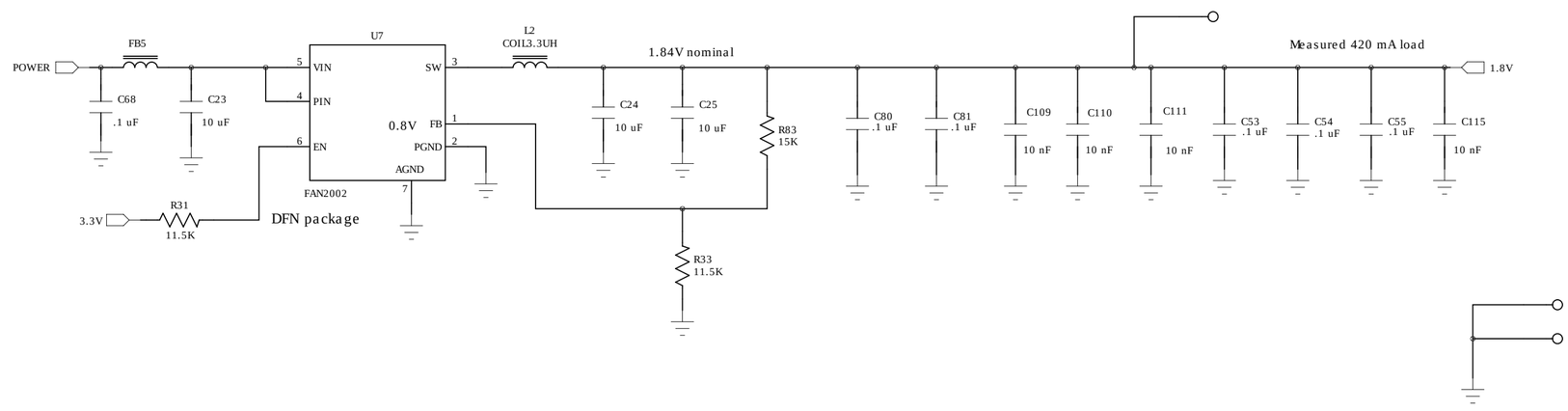
Zero suffix has
address at 100 1001

Best to Reset after
all power cycles
Set PD bit, Wait 50 mS
Then clear PD bit

2.5V Regulator



1.8V Regulator



Technologic Systems	Date March 10, 2010	
Title: TS-4500 Power Supplies, Temp Sensor		
Rev:	Designer RLM	Sheet 4 of 5

Two 100-pin Off-board Connectors

All DIO use 3.3V levels

Do not drive higher than 3.5V !

"POWER" pins supply all power to the module
Apply 3.8V to 5.5V to these pins

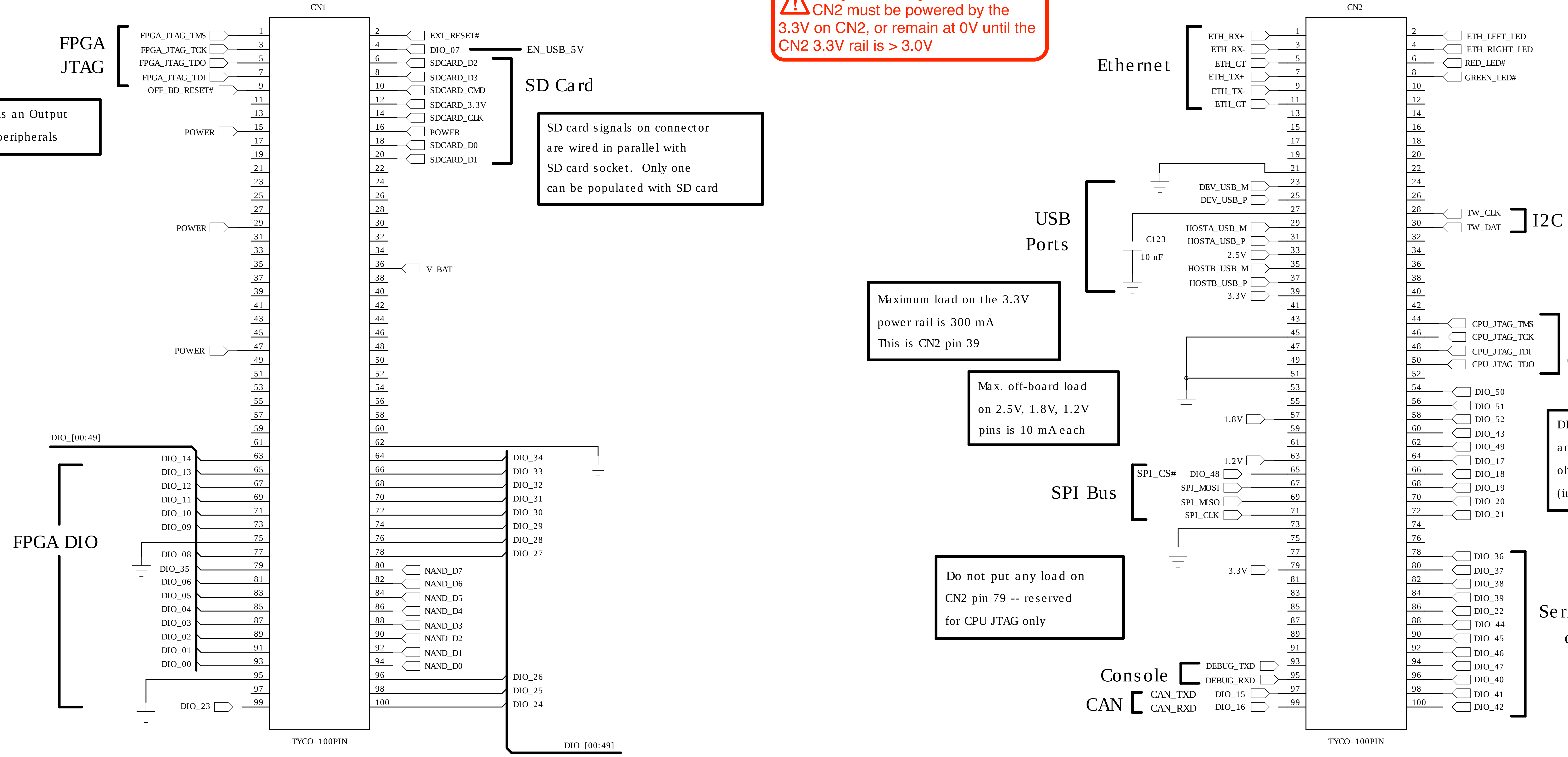
Current drain is approximately 400 mA
(less than 2 Watts)

EXT_RESET# is an Input used to reboot the CPU

Do not drive active high (use open drain)

⚠ All signals driving DIO on CN1 & CN2 must be powered by the 3.3V on CN2, or remain at 0V until the CN2 3.3V rail is > 3.0V

OFF_BD_RESET# is an Output used to reset all peripherals



Left
CN1
FPGA JTAG
FPGA_JTAG_TMS 1
FPGA_JTAG_TCK 3
FPGA_JTAG_TDO 5
FPGA_JTAG_TDI 7
OFF_BD_RESET# 9
POWER 15
POWER 29
POWER 47
2 EXT_RESET#
4 DIO_07
EN_USB_5V
SD Card
6 SDCARD_D2
8 SDCARD_D3
10 SDCARD_CMD
12 SDCARD_3.3V
14 SDCARD_CLK
16 POWER
18 SDCARD_D0
20 SDCARD_D1
36 V_BAT
DIO_[00:49]
FPGA DIO
DIO_14 63
DIO_13 65
DIO_12 67
DIO_11 69
DIO_10 71
DIO_09 73
DIO_08 77
DIO_35 79
DIO_06 81
DIO_05 83
DIO_04 85
DIO_03 87
DIO_02 89
DIO_01 91
DIO_00 93
DIO_23 99
64 DIO_34
66 DIO_33
68 DIO_32
70 DIO_31
72 DIO_30
74 DIO_29
76 DIO_28
78 DIO_27
80 NAND_D7
82 NAND_D6
84 NAND_D5
86 NAND_D4
88 NAND_D3
90 NAND_D2
92 NAND_D1
94 NAND_D0
96 DIO_26
98 DIO_25
100 DIO_24
TYCO_100PIN
Right
CN2
Ethernet
ETH_RX+ 1
ETH_RX- 3
ETH_CT 5
ETH_TX+ 7
ETH_TX- 9
ETH_CT 11
2 ETH_LEFT_LED
4 ETH_RIGHT_LED
6 RED_LED#
8 GREEN_LED#
USB Ports
DEV_USB_M 23
DEV_USB_P 25
C123
10 nF
HOSTA_USB_M 29
HOSTA_USB_P 31
2.5V 33
HOSTB_USB_M 35
HOSTB_USB_P 37
3.3V 39
28 TW_CLK
30 TW_DAT
I2C
CPU JTAG
44 CPU_JTAG_TMS
46 CPU_JTAG_TCK
48 CPU_JTAG_TDI
50 CPU_JTAG_TDO
1.8V 57
1.2V 63
SPI Bus
SPI_CS# DIO_48 65
SPI_MOSI 67
SPI_MISO 69
SPI_CLK 71
3.3V 79
54 DIO_50
56 DIO_51
58 DIO_52
60 DIO_43
62 DIO_49
64 DIO_17
66 DIO_18
68 DIO_19
70 DIO_20
72 DIO_21
Serial Ports or DIO
78 DIO_36
80 DIO_37
82 DIO_38
84 DIO_39
86 DIO_22
88 DIO_44
90 DIO_45
92 DIO_46
94 DIO_47
96 DIO_40
98 DIO_41
100 DIO_42
Console
DEBUG_TXD 93
DEBUG_RXD 95
CAN
CAN_TXD DIO_15 97
CAN_RXD DIO_16 99
TYCO_100PIN

SD card signals on connector are wired in parallel with SD card socket. Only one can be populated with SD card

Maximum load on the 3.3V power rail is 300 mA
This is CN2 pin 39

Max. off-board load on 2.5V, 1.8V, 1.2V pins is 10 mA each

Do not put any load on CN2 pin 79 -- reserved for CPU JTAG only

DIO_20, DIO_21, DIO_50 and DIO_51 have a 2K ohm resistor to GND (initializes to a logic "0")

CAN port and all UARTs can all be changed to simple DIO lines

DIO_36 = UART0_TXD
DIO_37 = UART0_RXD
DIO_38 = UART1_TXD
DIO_39 = UART1_RXD

DIO_22 = UART2_TXD
DIO_44 = UART2_RXD
DIO_45 = UART3_TXD
DIO_46 = UART3_RXD

DIO_47 = UART4_TXD
DIO_40 = UART4_RXD
DIO_41 = UART5_TXD
DIO_42 = UART5_RXD

Boot Straps

Mode 2	Boots from
1	NAND Flash
0	SD Card

DIO_26 = MODE1
DIO_25 = MODE2

On some other modules, there is a 16-bit bus for static memory type devices. But the TS-4500 does not support this functionality

The TS-4500 uses these "Bus signals" as DIO only.

MODE1 and MODE2 states are latched prior to OFF_BD_RESET# deasserted

MODE1 and MODE2 have PU resistors

Connect a 1.5K ohm resistor from DIO_25 to OFF_BD_RESET# to boot from SD card

Technologic Systems		Date March 10, 2010
Title: TS-4500 100-pin Off-Board Connectors		
Rev:	Designer RLM	Sheet 5 of 5