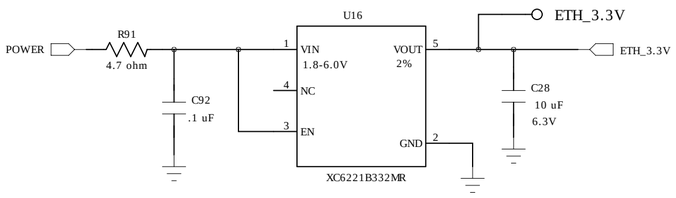
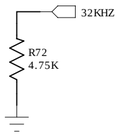
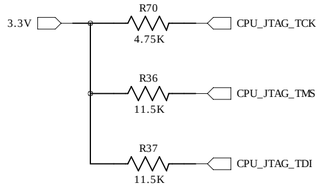
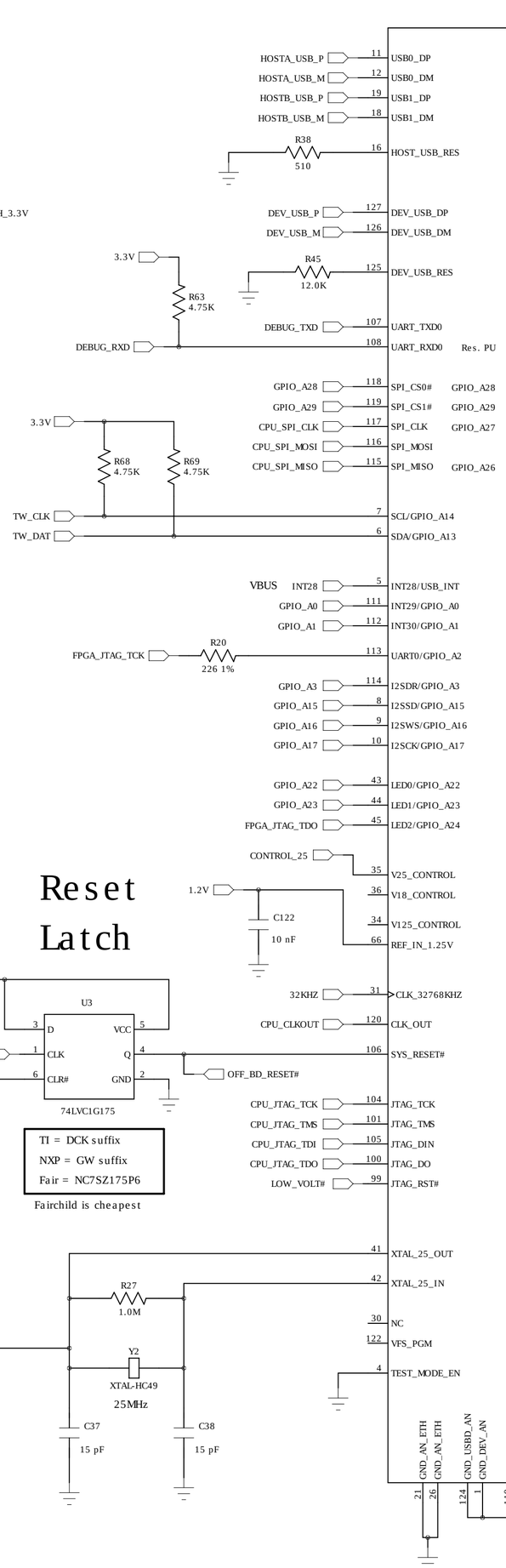
Ethernet
Analog 3.3V



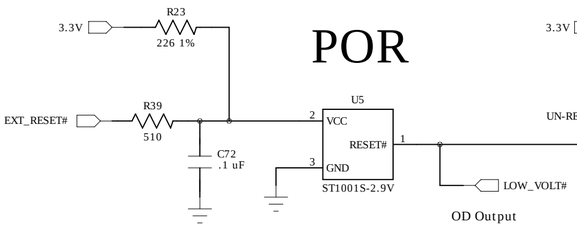






10/100 Ethernet

Reset
Latch

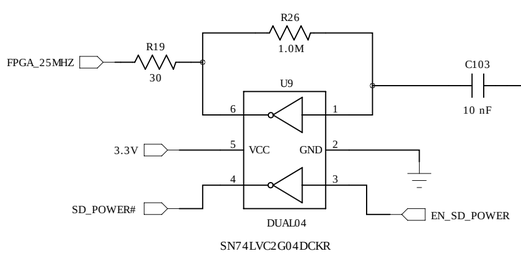


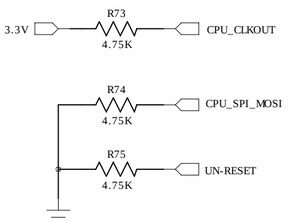
OD Output

TI = DCK suffix
NXP = GW suffix
Fair = NC7SZ175P6

Fairchild is cheapest

POR





Strap Options

CLK_OUT	ICE mode (default high)
SPI_MOSI	Low = Little Indian
RAM_CKE	High = SPI Boot

MOUNTING HOLES

MT1 MT2

Nov. 17, 2010
R33 changed to 11.0K

Rev.B to Rev.C
No stencil change

Technologic Systems		Date Sept. 20, 2011
Title: TS-4500 CPU, Ethernet, POR		
Rev: C	Designer	Sheet 1 of 5

FPGA with 5000 LUTs

XP2-5 has:
5K LUTS 2 PLLs
9 blocks of 1Kx18 Block RAM
12 18x18 Multipliers

100 I/O with 144 pin package
"instant ON" = about 1.5 mS
input PLL clock = 10 MHz min

Boot Straps

Mode 1	Mode 2	Boots from
1	1	NAND Flash
1	0	SD Card
0	1	Off-board Flash
0	0	Off-board Flash

MODE1 and MODE2 states and Board ID bits must be latched prior to UN_RESET# pulsed

MODE1 and MODE2 have PU resistors

Use 1K ohm resistor to GND to set low

Pins 87 and 88 must be read prior to UN-RESET being pulsed

Pins 54 and 138 must be read prior to UN-RESET being pulsed

EXT_RESET# must be Open Drain

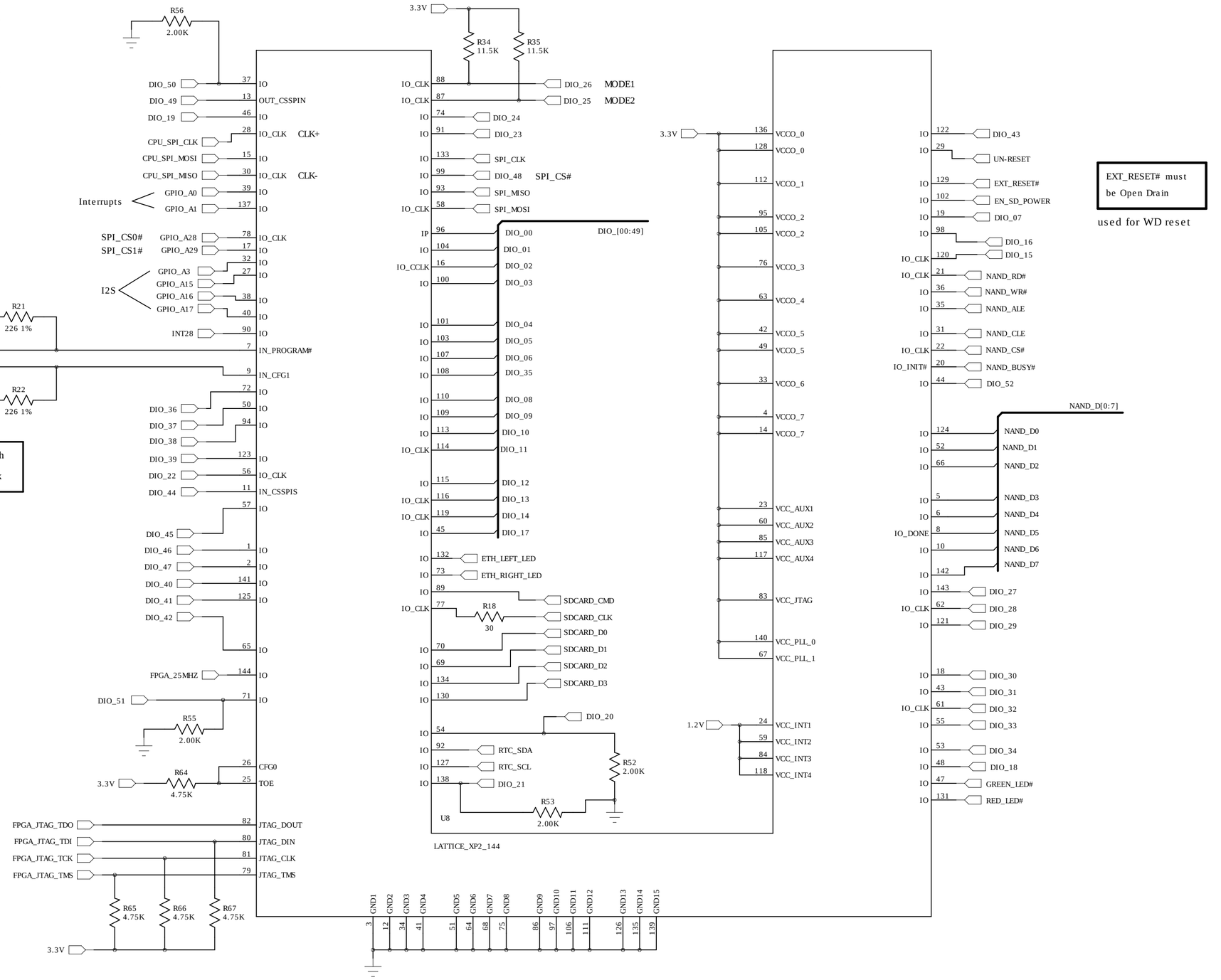
used for WD reset

Differences from TS-7500/7550/7551/7552
- ETH LEDs are inverted
- Console path not used

Board ID bits

	Pin 54 (weak PU)	Pin 138 (weak PD)	Pin 71	Pin 37	Hex
TS-7500	1	1	1	1	F
TS-7550	1	1	0	1	B
WM-7551	0	0	1	1	C
TS-7552	1	0	1	1	D
TS-7553	1	0	0	1	9
TS-7554	0	0	0	1	8
TS-7555	0	1	0	1	A
TS-4500	0	0	0	0	0

7552 and 7553 FPGA pin 93 = MISO



UN-RESET rising edge, deasserts CPU Reset
(Must be careful at start up)
It has a PD resistor -- always idle low

EN_SD_POWER should initialize high

During JTAG Flash programming the PROGRAM# pin should be high else it can inhibit Flash --> SRAM

DONE likewise must be high
These do have weak PU resistors

Set CONFIG_MODE to NONE
This allows all pins to be used

Pull-up and pull-down resistors are 6 to 30K ohms

PROGRAM#, DONE, and INIT# are dedicated configuration pins when CFG0 is low. When CFG0 is high they are "general purpose I/O"

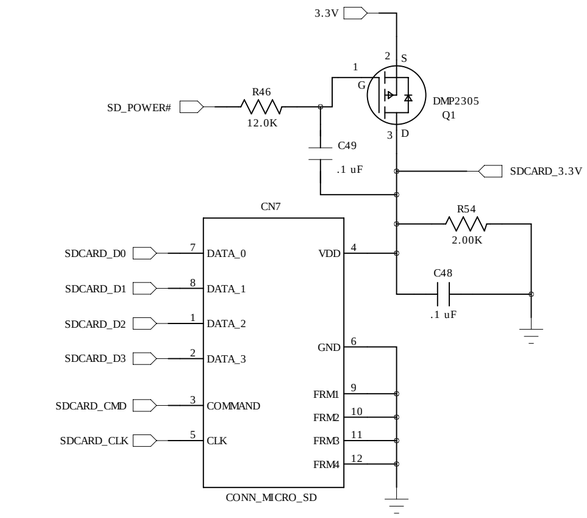
Page 4 of TN1141

Page 37 of Data Sheet (Hot Socketing)
Power Supplies can be sequenced in any order but must be monotonic

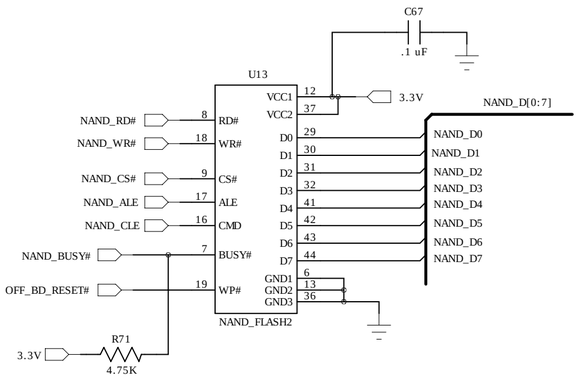
All I/O lines are tri-stated during power cycling

Technologic Systems		Date Sept. 20, 2011
Title: TS-4500 FPGA		
Rev: C	Designer RLM	Sheet 2 of 5

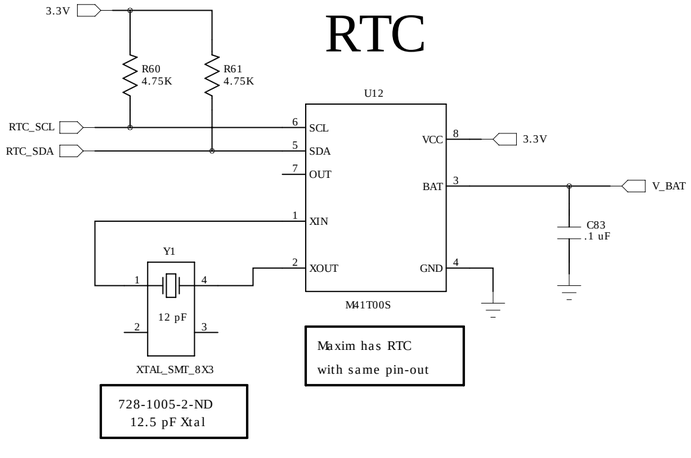
Micro SD Card Socket



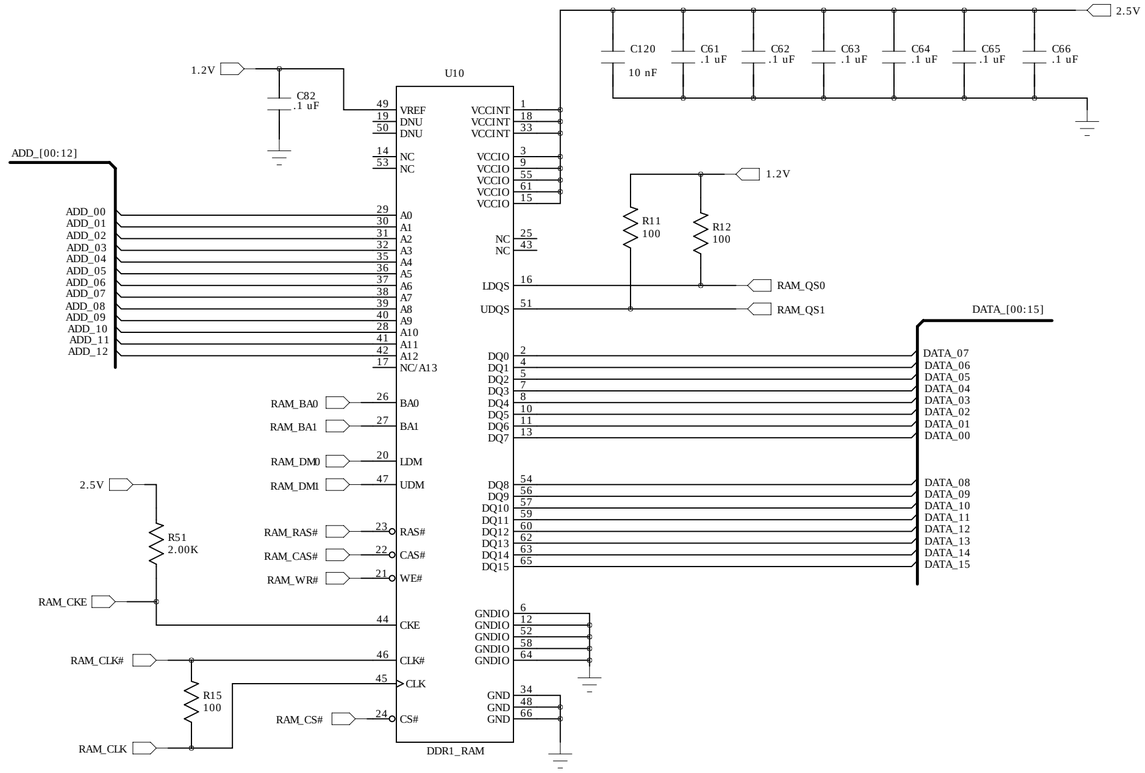
512 Mbyte
NAND Flash



RTC



64 Mbyte
DDR1 SDRAM



DDR RAM Notes

The DDR clock differential pair is the most critical trace on the entire board

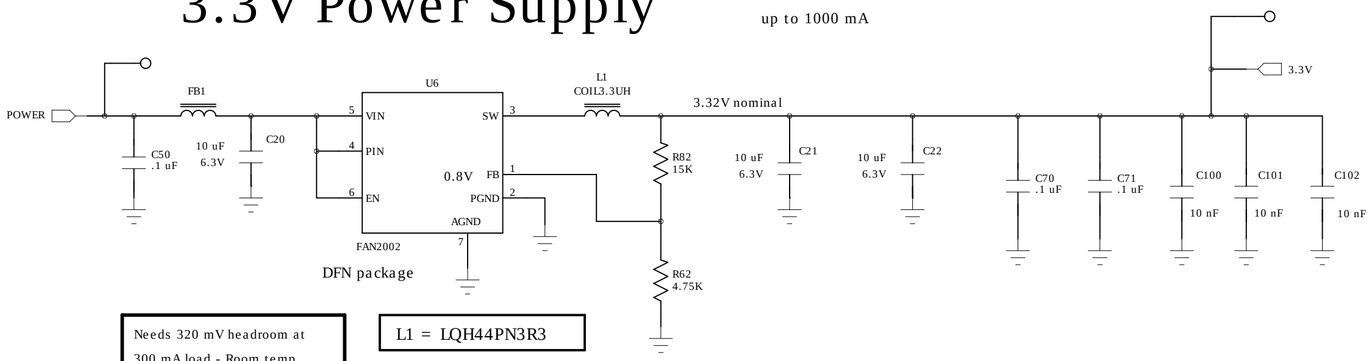
The data lines in each byte lane can be swapped on the RAM chip for optimal layout
Example: D0 and D5 can be swapped, but not D7 and D8

The trace length of each data line (in a single byte lane) and the respective QS and DM signals must be matched to within 2.5 mm

Address and Command signals can be grouped together, but must be isolated from data and M_DSQ and M_DM signals (by at least .5 mm)
Or run them on different layer

Technologic Systems		Date Sept. 20, 2011
Title: TS-4500 RAM, RTC, Flash, SD socket		
Rev: C	Designer	Sheet 3 of 5

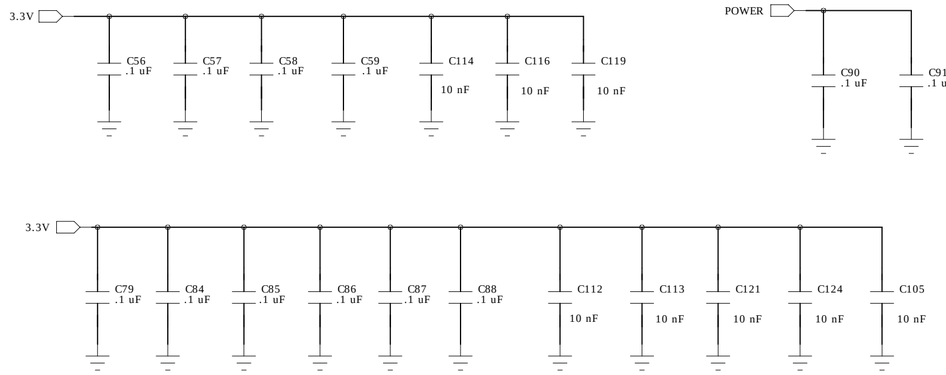
3.3V Power Supply



Needs 320 mV headroom at
300 mA load - Room temp

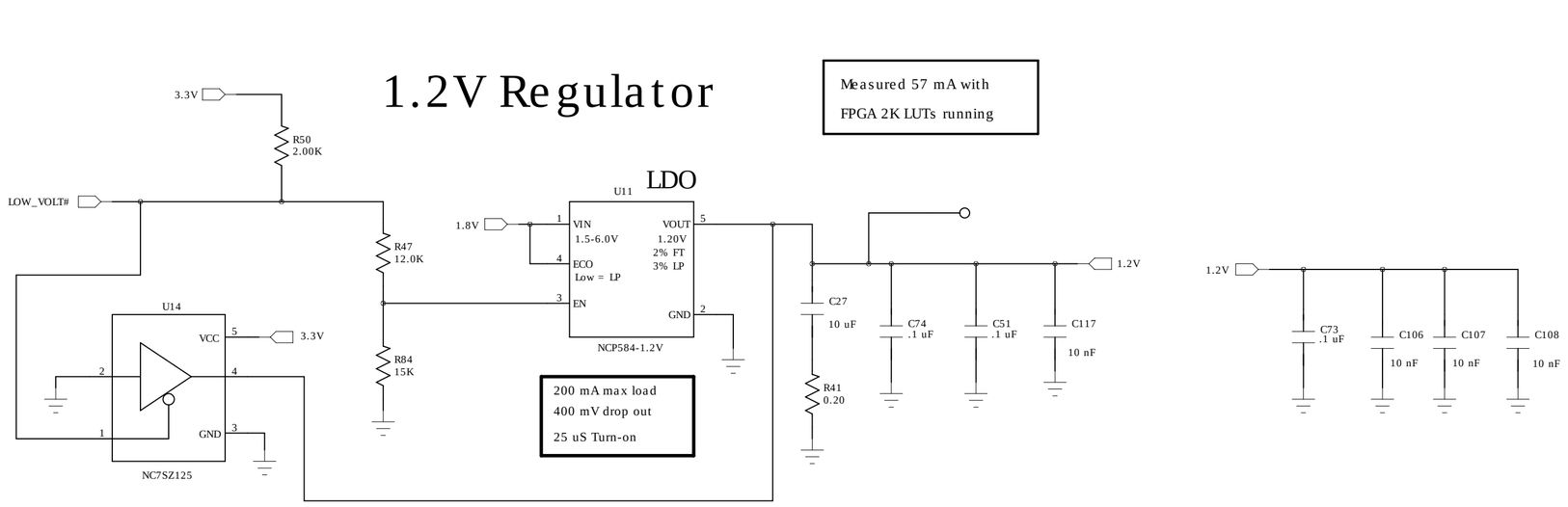
L1 = LQH44PN3R3

Max. current = 1.7 Amps

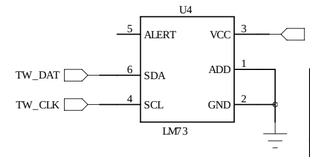


1.2V Regulator

Measured 57 mA with
FPGA 2K LUTs running



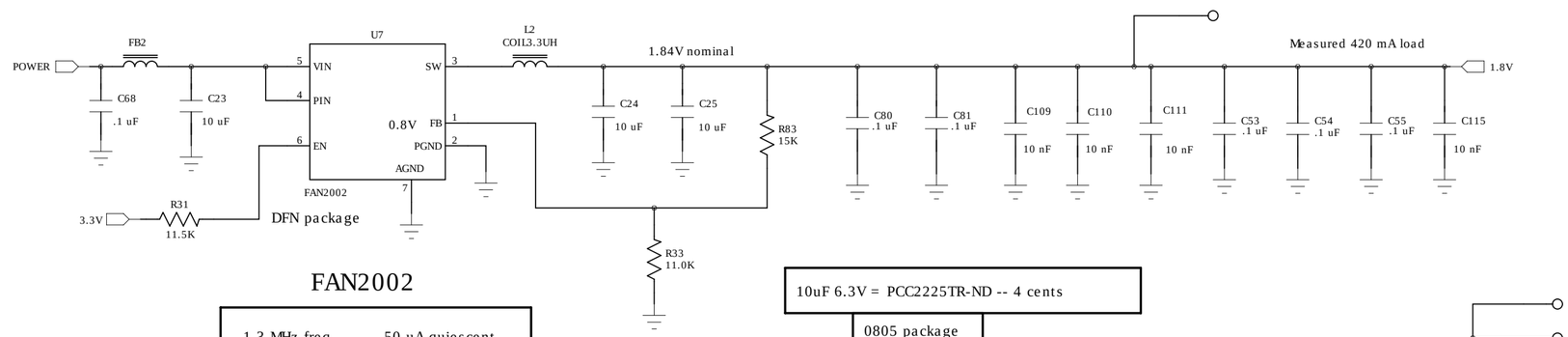
Temp Sensor



Zero suffix has
address at 100 1001

Best to Reset after
all power cycles
Set PD bit, Wait 50 mS
Then clear PD bit

1.8V Regulator



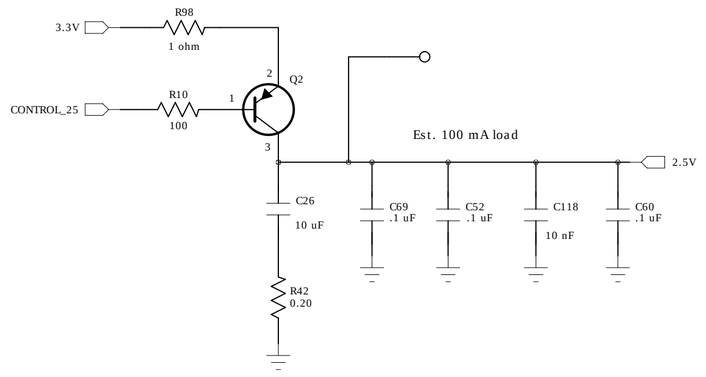
FAN2002

1.3 MHz freq. 50 uA quiescent
Vout = 800mV * [1+ Rtop/Rbot]
> 90% eff. at 100-400 mA load
1000 mA max load

10uF 6.3V = PCC2225TR-ND -- 4 cents

0805 package

2.5V Regulator



Technologic Systems	Date Sept. 20, 2011	
Title: TS-4500 Power Supplies, Temp Sensor		
Rev: C	Designer RLM	Sheet 4 of 5

Two 100-pin Off-board Connectors

"POWER" pins supply all power to the module
Apply 3.8V to 5.5V to these pins

Current drain is approximately 400 mA
(less than 2 Watts)

EXT_RESET# is an Input
used to reboot the CPU

Do not drive active high
(use open drain)

⚠ All signals driving DIO on CN1 & CN2 must be powered by the 3.3V on CN2, or remain at 0V until the CN2 3.3V rail is > 3.0V

Left

CN1

FPGA JTAG
- 1 FPGA_JTAG_TMS
- 3 FPGA_JTAG_TCK
- 5 FPGA_JTAG_TDO
- 7 FPGA_JTAG_TDI
- 9 OFF_BD_RESET#

OFF_BD_RESET# is an Output
used to reset all peripherals

POWER: 15, 29, 47

- 2 EXT_RESET#
- 4 DIO_07 — EN_USB_5V

SD Card
- 6 SDCARD_D2
- 8 SDCARD_D3
- 10 SDCARD_CMD
- 12 SDCARD_3.3V
- 14 SDCARD_CLK
- 16 POWER
- 18 SDCARD_D0
- 20 SDCARD_D1

SD card signals on connector are wired in parallel with SD card socket. Only one can be populated with SD card

- 36 V_BAT

DIO_[00:49]

FPGA DIO
- 63 DIO_14
- 65 DIO_13
- 67 DIO_12
- 69 DIO_11
- 71 DIO_10
- 73 DIO_09
- 77 DIO_08
- 79 DIO_35
- 81 DIO_06
- 83 DIO_05
- 85 DIO_04
- 87 DIO_03
- 89 DIO_02
- 91 DIO_01
- 93 DIO_00
- 99 DIO_23

- 64 DIO_34
- 66 DIO_33
- 68 DIO_32
- 70 DIO_31
- 72 DIO_30
- 74 DIO_29
- 76 DIO_28
- 78 DIO_27

- 80 NAND_D7
- 82 NAND_D6
- 84 NAND_D5
- 86 NAND_D4
- 88 NAND_D3
- 90 NAND_D2
- 92 NAND_D1
- 94 NAND_D0
- 96 DIO_26
- 98 DIO_25
- 100 DIO_24

DIO_[00:49]

TYCO_100PIN

Mode 1	Mode 2	Boots from
1	1	NAND Flash
1	0	SD Card
0	1	Off-board Flash
0	0	Off-board Flash

DIO_26 = MODE1
DIO_25 = MODE2

MODE1 and MODE2 states and Board ID bit states are latched prior to OFF_BD_RESET# deasserted

MODE1 and MODE2 have PU resistors

Use 1K ohm resistor to GND to set low

SPI Flash is Boot source when MODE1 is low.

On some other modules, there is a 16-bit bus for static memory type devices. But the TS-4500 does not support this functionality

The TS-4500 uses these "Bus signals" as DIO only.

Right

CN2

Ethernet
- 1 ETH_RX+
- 3 ETH_RX-
- 5 ETH_CT
- 7 ETH_TX+
- 9 ETH_TX-
- 11 ETH_CT
- 13 3.3V

- 2 ETH_LEFT_LED
- 4 ETH_RIGHT_LED
- 6 RED_LED#
- 8 GREEN_LED#

USB Ports
- 23 DEV_USB_M
- 25 DEV_USB_P
- 29 HOSTA_USB_M
- 31 HOSTA_USB_P
- 33 2.5V
- 35 HOSTB_USB_M
- 37 HOSTB_USB_P
- 39 3.3V

C123 10 nF

- 28 TW_CLK
- 30 TW_DAT

I2C

Maximum off-board load on 3.3V pin is 300 mA

Max. off-board load on 2.5V, 1.8V, 1.2V pins is 10 mA each

- 44 CPU_JTAG_TMS
- 46 CPU_JTAG_TCK
- 48 CPU_JTAG_TDI
- 50 CPU_JTAG_TDO

CPU JTAG

- 57 1.8V
- 63 1.2V

SPI Bus
- SPI_CS# DIO_48
- SPI_MOSI
- SPI_MISO
- SPI_CLK

- 54 DIO_50
- 56 DIO_51
- 58 DIO_52
- 60 DIO_43
- 62 DIO_49
- 64 DIO_17
- 66 DIO_18
- 68 DIO_19
- 70 DIO_20
- 72 DIO_21

DIO_20, DIO_21, DIO_50 and DIO_51 have a 2K ohm resistor to GND (initializes to a logic "0")

Pin 79 = CPU JTAG Vcc
Not 3.3V on some modules

Max. load = 20 mA

- 79 3.3V

Console
- 93 DEBUG_TXD
- 95 DEBUG_RXD

CAN
- CAN_TXD DIO_15 97
- CAN_RXD DIO_16 99

- 78 DIO_36
- 80 DIO_37
- 82 DIO_38
- 84 DIO_39
- 86 DIO_22
- 88 DIO_44
- 90 DIO_45
- 92 DIO_46
- 94 DIO_47
- 96 DIO_40
- 98 DIO_41
- 100 DIO_42

Serial Ports or DIO

TYCO_100PIN

CAN port and all UARTs can all be changed to simple DIO lines

DIO_36 = UART0_TXD
DIO_37 = UART0_RXD
DIO_38 = UART1_TXD
DIO_39 = UART1_RXD

DIO_22 = UART2_TXD
DIO_44 = UART2_RXD
DIO_45 = UART3_TXD
DIO_46 = UART3_RXD

DIO_47 = UART4_TXD
DIO_40 = UART4_RXD
DIO_41 = UART5_TXD
DIO_42 = UART5_RXD

Technologic Systems		Date Sept. 20, 2011
Title: TS-4500 100-pin Off-Board Connectors		
Rev: C	Designer RLM	Sheet 5 of 5