### FPGA with 5000 LUTs

#### Board ID bits

<table>
<thead>
<tr>
<th>Pin 54</th>
<th>Pin 138</th>
<th>Pin 71</th>
<th>Pin 37</th>
<th>Hex</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>F'</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>B</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>C</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>D</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>9</td>
</tr>
<tr>
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<td>0</td>
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<td>1</td>
</tr>
<tr>
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<td>0</td>
<td>0</td>
<td>1</td>
<td>A</td>
</tr>
<tr>
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<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

**Pin 54 and 138 must be used prior to UN-RESET being pulsed**

**Pin 54 and 138 must be used prior to UN-RESET being pulsed**

**Pin 87 and 88 must be used prior to UN-RESET being pulsed**

#### Differences from TS-7500/7550/7551/7552

- ETH LEDs are inverted
- Console path not used

#### Boot Straps

<table>
<thead>
<tr>
<th>Mode 1</th>
<th>Mode 2</th>
<th>Boot from</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>NAND Flash</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>SD Card</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>On-board Flash</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>On-board Flash</td>
</tr>
</tbody>
</table>

**MODE 1 and MODE 2**

- MODE1 and MODE2 have PU resistors
- Use 1k ohm resistor to GND or not low

**MODE and MODES**

- MODE and MODES have FU resistors
- Use 1k ohm resistor to GND or not low

**MODES**

- MODE and MODES have PU resistors
- Use 1k ohm resistor to GND or not low

### Interrupts

- DIO_51
- I2S
- DIO_47
- DIO_46
- DIO_42
- DIO_50
- DIO_44
- DIO_22
- DIO_39

**Page 37 of Data Sheet (Heat Sinking)**

Power Supplies can be sequenced in any order but must be monotonic.

All I/O lines are tri-stated during power cycling.
The DDR clock differential pair is the most critical trace on the entire board.

The data lines in each byte lane can be swapped on the RAM chip for optimal layout.

Example: DB and DB can be swapped, but not D7 and D8.

The trace length of each data line (in a single byte lane) and the respective
QS and DM signals must be matched to within 2.5 mm.

Address and Command signals can be grouped together, but must be isolated
from data and M_DSQ and M_DM signals (by at least .5 mm)
Or run them on different layer.
# 3.3V Power Supply

- **Up to 1000 mA**

## 1.2V Regulator

- Measured 57 mA with FPGA 2K LUTs running

## 1.8V Regulator

- Measured 420 mA load

## 2.5V Regulator

- 100 mA max load

## Temp Sensor

- Zero offset has address at 100 1001

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**Title:** TS-4500 Power Supplies, Temp Sensor

**Rev:** C  
**Designer:** RLM  
**Sheet:** 4 of 5

**Date:** Sept. 20, 2011
Two 100-pin Off-board Connectors

**POWER** pins supply all power to the module

Apply 3.3V to 5.0V to these pins

Current drain is approximately 400 mA

(less than 2 Watts)

**EXT_RESET** is an Input

used to reset the CPU

Do not drive active high

(see open drain)

**OFF_SD_RESET** is an Output

used to reset all peripherals

**FPGA JTAG**

**SD Card**

SD card signals on connector

are wired in parallel with

SD card output. Only one

can be populated with SD card

**FPGA DIO**

**Ethernet**

Maximum off-board load

on 3.3V pins is 300 mA

Max. off-board load

on 2.5V, 1.8V, 1.2V

pins is 10 mA each

**USB Ports**

Maximum off-board load

on 3.3V pins is 300 mA

Max. load = 20 mA

**SPI Bus**

Pin 79 = CPU JTAG Vec

Not 3.3V on some modules

**Serial Ports or DIO**

CAN port and all UARTs

can all be changed to

temporary CAN pins

**I2C**

**CPU JTAG**

DEQ_20, DEQ_21, DEQ_50

and DEQ_51 have a 2K

pull resistor to GND.

One signal is connected to a logic 0

**Technology Systems**

Title: TS-4500 100-pin Off-Board Connectors

Date: Sept. 20, 2011

Rev: C Designer RLM Sheet 5 of 5

**MODE1** and **MODE2** states

and Board SD bit states

are latched prior to

OFF_SD_RESET

**SD Flash** in Boot section

when MODE1 is low

**MODE1** and **MODE2** states

have PC access

Use JK-shares outputs to GND to set low

On some other modules, there is a

16-bit bus for static memory

type devices. But the TS-4500

does not support this functionality

The TS-4500 uses these

bus signals" as DEQ only.

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**WARNING:**

All signals driving **DIO** on CN1 & CN2 must be powered by the

3.3V on CN2, or remain at 0V until the

CN2 3.3V rail is > 3.0V

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**DIO_26** = **MODE1**

**DIO_25** = **MODE2**

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**DEQ_20** = UART5_RXD

**DEQ_21** = UART4_RXD

**DEQ_50** = UART3_RXD

**DEQ_51** = UART2_RXD

**DEQ_45** = UART1_RXD

**DEQ_46** = UART0_RXD

**DEQ_47** = UART4_TXD

**DEQ_40** = UART3_TXD

**DEQ_41** = UART2_TXD

**DEQ_42** = UART1_TXD