**Board ID bits**

<table>
<thead>
<tr>
<th>Pin 54 (weak PU)</th>
<th>Pin 56 (weak PI)</th>
<th>Pin 71</th>
<th>Pin 37</th>
<th>Hex</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>F'</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>B</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>C</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>D</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>9</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>8</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>A</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

7552 and 7553 FPGA pin 90 = MOE2

**Differences from TS-7500/7550/7551/7552**

- ETH LEDs are inverted
- Console path not used

**Boot Straps**

<table>
<thead>
<tr>
<th>Mode 1</th>
<th>Mode 2</th>
<th>Boot from</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>NAND Flash</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>SD Card</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Off-board Flash</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>Off-board Flash</td>
</tr>
</tbody>
</table>

- MODE1 and MODE2 states and Board ID bits must be latched prior to UN-RESET being pulsed
- The 1K ohm resistor on EN_SD_POWER is left low
- MODE1 and MODE2 have PU resistors
- EN_SD_POWER should initialize high
- UN-RESET rising edge, deasserts CPU Reset
- TS-4500 FPGA
- NAND Flash
- 4 blocks of 1Kx18 Block RAM
- 100 I/O with 144 pin package
- Input QNC - about 1.5 nH input PLL clock = 10 MHz

**FPGA with 5000 LUTs**

- 9 blocks of 16Kx4 BRAM
- 12 10x10 Multiplexers
- 100 I/O with 144 pin package
- Input QNC - about 1.5 nH input PLL clock = 10 MHz

**Revision Notes**

- UN-RESET signal edge; disconnect CPU Reset
- It has a PU resistor - always safe low
- NS_ID_POWER should initialize high
- During JTAG flash programming, the PROGRAM pin should be high; otherwise the flash will not be erased
- DON'T do this with the VCCO high
- It is a "general-purpose IO" (GPIO)
- Page 37 of Data Sheet (Not Soldering)
- Power Supplies can be sequenced in any order
- All I/O lines are tristated during power cycling
The DDR clock differential pair is the most critical trace on the entire board.

The data lines in each byte line can be swapped on the RAM chip for optimal layout.

Example: D6 and D5 can be swapped, but not D7 and D8.

The trace length of each data line (in a single byte lane) and the respective QS and DM signals must be matched to within 2.5 mm.

Address and Command signals can be grouped together, but must be isolated from data and M_DSQ and M_DM signals (by at least 5 mm).

Or run them on different layer.

Micro SD Card Socket

512 Mbyte NAND Flash

RTC

64 Mbyte DDR1 SDRAM

512 Mbyte NAND Flash Notes:

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- Or run them on different layer.