M0DE1 and M0DE2 states and Board ID bits must be latched prior to UN-RESET being pulsed.

The FPGA has 5000 LUTs. It has a PD resistor — always idle low.

Page 37 of Data Sheet (Ref. Soldering)
Power Supplies can be sequenced in any order but must be monotonic.
All I/O lines are tri-stated during power cycling.
The DDR clock differential pair is the most critical trace on the entire board. The data lines in each byte lane can be swapped on the RAM chip for optimal layout. Example: D0 and D1 can be swapped, but not D7 and D6. The trace length of each data line (in a single byte lane) and the respective QS and DM signals must be matched to within 2.5 mm. Address and Command signals can be grouped together, but must be isolated from data and M_DSQ and M_DM signals (by at least .5 mm) or run them on different layer.
3.3V Power Supply

1.2V Regulator

1.8V Regulator

2.5V Regulator

Temp Sensor

Technologic Systems
Title: TS-4500 Power Supplies, Temp Sensor
Rev: C  Designer RLM  Sheet 4 of 5

Date: Sept. 20, 2011
Two 100-pin Off-board Connectors

OFF_BD_RESET is an Output used to reset all peripherals

EXT_RESET# is an Input used to reboot the CPU

SD card signals on connector are wired in parallel with SD card codec. Only one can be populated with SD card

SPI Flash is Boot source

Limited boot source to 300 mA on 3.3V pin is 300 mA

Max. off-board load on 2.5V, 1.8V, 1.2V pins is 10 mA each

Max. load = 20 mA

On some other modules, there is a 16-bit bus for static memory type devices. But the TS-4500 does not support this functionality

The TS-4500 uses these

Bus signals as DIO only.

Some FPGA ports are left open

Some FPGA DIO states and Board ID bit states are left open prior to

OFF_BD_RESET asserted

SPI Flash is Boot source when MODE0 is low

Serial Ports or DIO

Power supply to all power to module

Current drain is approximately 400 mA

(for less than 2 watts)

Two 100-pin Off-board Connectors

FPGA DIO

FPGA JTAG

Off-board Flash

FPGA JTAG

SD Card

JTAG Ethernet

Serial Ports

Two 100-pin Off-board Connectors

CPU JTAG

SPI Bus

Console

USB Ports

Ethernet

TS-4500 100-pin Off-Board Connectors

Power" pins supply all power to the module

Apply 5.0V to 5.3V to these pins

Use 1K ohm resistor to GND to set low

MODE1 and MODE2 states are latched prior to

OFF_BD_RESET asserted

Use the active high

"MODE2 state to boot

/mode2

MODE1 and MODE2 have no function

Pin 59 = CPU JTAG Vcc

Not 3.3V on some modules

Maximum off-board load on 3.3V pin is 300 mA

Max. off-board load on 2.5V, 1.8V, 1.2V pins is 10 mA each

Max. load = 20 mA

On some other modules, there is a 16-bit bus for static memory type devices. But the TS-4500 does not support this functionality

The TS-4500 uses these

Bus signals as DIO only.

Some FPGA ports are left open

Some FPGA DIO states and Board ID bit states are left open prior to

OFF_BD_RESET asserted

SPI Flash is Boot source when MODE0 is low

Serial Ports or DIO

Power supply to all power to module

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(for less than 2 watts)