MX283 ARM® CPU

UARTs, ADC

Audio

SD Card

SPI Boot

NAND, PWM

JTAG, I2C

Rev. A Problems:
- Ethernet LEDs wrong!
- No CAN connected
- No A/D connected
- Add WiFi!
- Add low power modes?
- Pwr switch to PHY?
- Remove FPGA?

12 MHz default boot clock
Max SPI clock rate = 20 MHz

Page 1311 - Winbond SPI i2 and i4 supported
EVK schematic references a 35MHz Winbond chip

PWM outputs can be 24 MHz divided by 16-bit integer
Allows clock 12MHz and lower

All JTAG have 47K internal pull except RTCK

Technologic Systems

Title: TS-4600 MX283 CPU

Date: Feb. 21, 2014

Rev: A

Designer

Sheet 1 of 9
CPU Power

Diagram of the CPU Power system, showing various components and connections such as USB, DCDC, and others.
MX283 DDR2 SDRAM (128 or 256 MByte)
Auto MDIX is supported
Polarity Correction also supported
MX283 SPI Boot and FPGA Config Flash

SPI Boot Flash

64 bytes of OTP

Not Populated?

RTC and Temp. Sensor

FPGA Bypass Caps

BAT must be > 2.7V for temp comp to work

Temp takes 68 uA for 22 ms
Once every 1 or 10 min.
Micro SD Card Sockets

SD LEDs

Ethernet LED Buffer
Two 100-pin Off-board Connectors

- **POWER** pins supply all power to the module. Apply 4.5V to 5.5V to these pins.
- Current drain is approximately 200 mA.

- OFF_BD_RESET is an Output used to reset all peripherals.
- Use an open drain, not active high.

- REBOOT# is an Input used to reboot the CPU. Do not drive active high (use open drain).

- 3.3V rail can supply up to 400 mA to base board.

- JTAG:
  - SPI or DIO
  - CPU JTAG

- Serial Ports or DIO

- Two 100-pin Off-board Connectors
  - Left and Right

- FPGA DIO
  - FPGA JTAG

- 16 bit Data Bus or DIO

- Primary Ethernet
  - USB Ports
  - USB Host

- CPU Ports
  - Console

- LCD Pix CLK
  - LCD HSYNC
  - LCD D17
  - LCD D16
  - LCD D14
  - LCD D13
  - LCD D11
  - LCD D10
  - LCD D09

- UARTs:
  - UART0 RXD
  - UART1 RXD
  - UART0 TXD
  - UART2 RXD
  - UART3 RXD
  - UART4 RXD
  - UART5 RXD

- UARTs:
  - UART0 TXD
  - UART1 RXD

- Audio Ports:
  - AUD RXD
  - AUD FRM
  - AUD CLK

- Debug Ports:
  - DEBUG RXD
  - DEBUG TXD

- I2C:
  - I2C DAT
  - I2C CLK

- 2nd Ethernet Port

- 12S or DIO

- CPU JTAG

- HDMI Ports

- Two 100-pin Off-board Connectors
  - Left and Right

- FPGA DIO
  - FPGA JTAG

- 16 bit Data Bus or DIO

- Primary Ethernet
  - USB Ports
  - USB Host

- CPU Ports
  - Console

- LCD Pix CLK
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- UARTs:
  - UART0 RXD
  - UART1 RXD

- UARTs:
  - UART0 TXD
  - UART1 RXD

- Audio Ports:
  - AUD RXD
  - AUD FRM
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- Debug Ports:
  - DEBUG RXD
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- I2C:
  - I2C DAT
  - I2C CLK

- 2nd Ethernet Port

- 12S or DIO

- CPU JTAG

- HDMI Ports