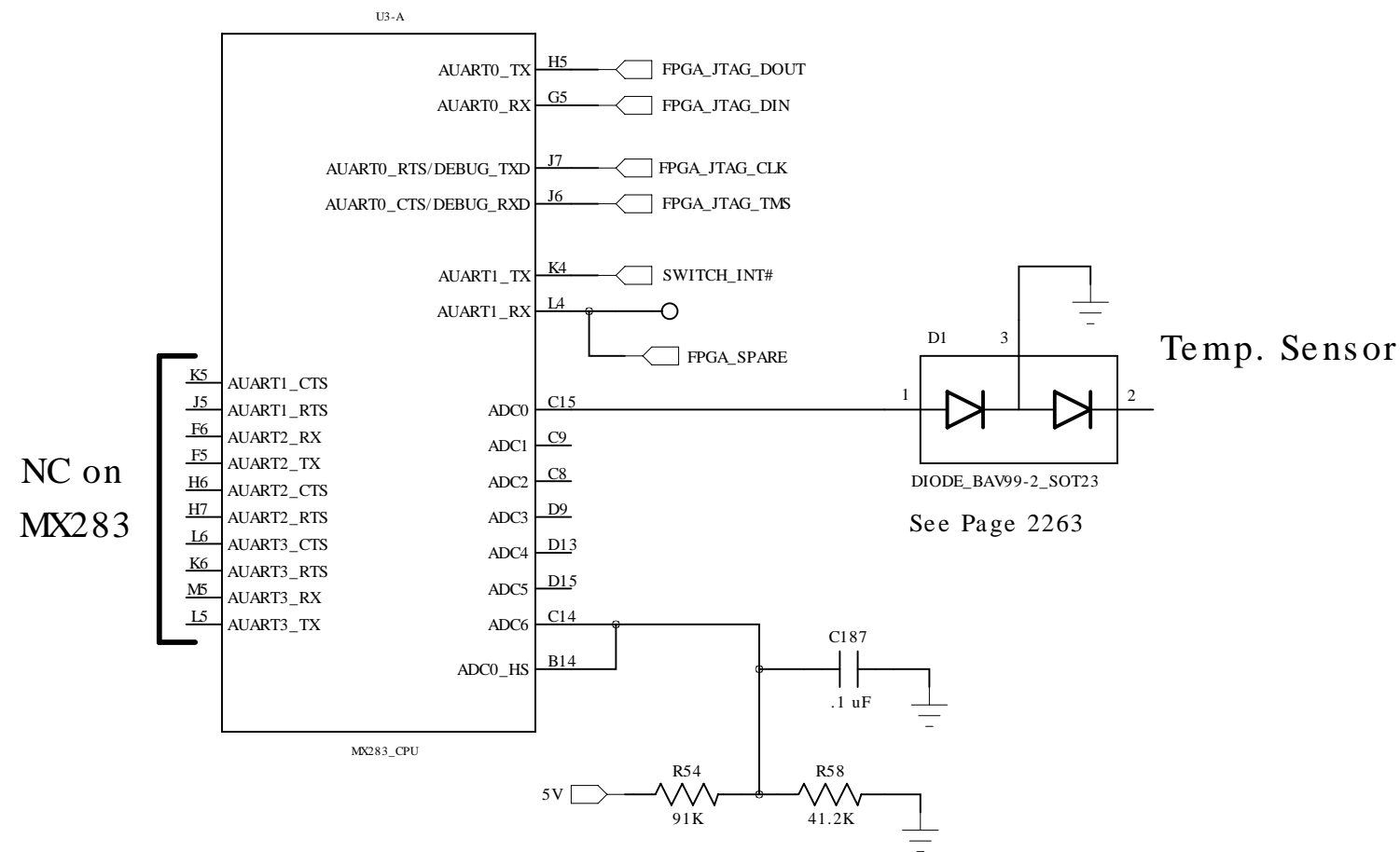


# MX283 ARM9 CPU

## UARTs, ADC

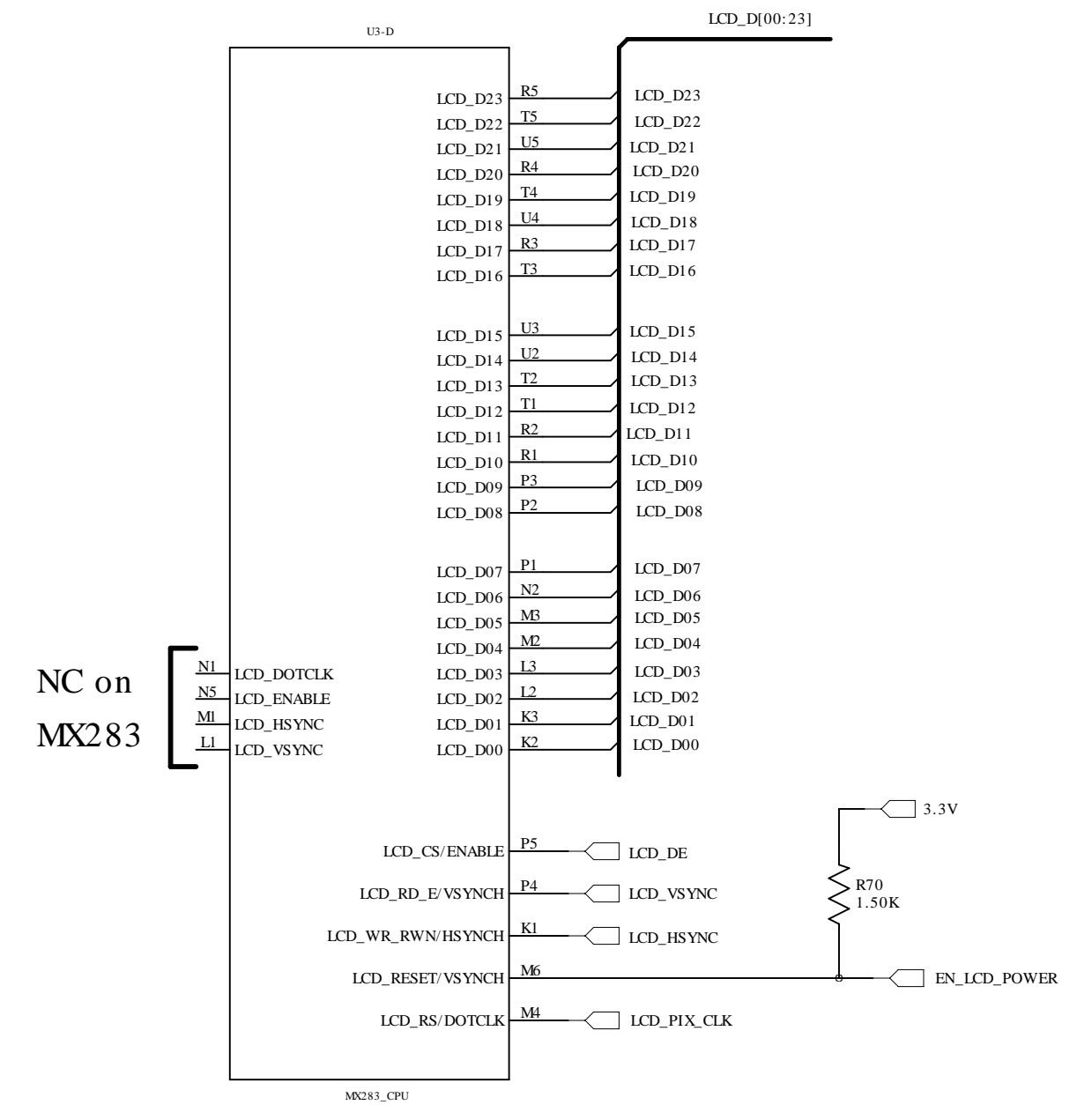


NC on MX283

## Re v. A Problems:

- Ethernet LEDs wrong !
- No CAN connected
- No A/D connected
- Add WiFi !
- Add low power modes ?
- Pwr switch to PHY ?
- Remove FPGA ?

## LCD



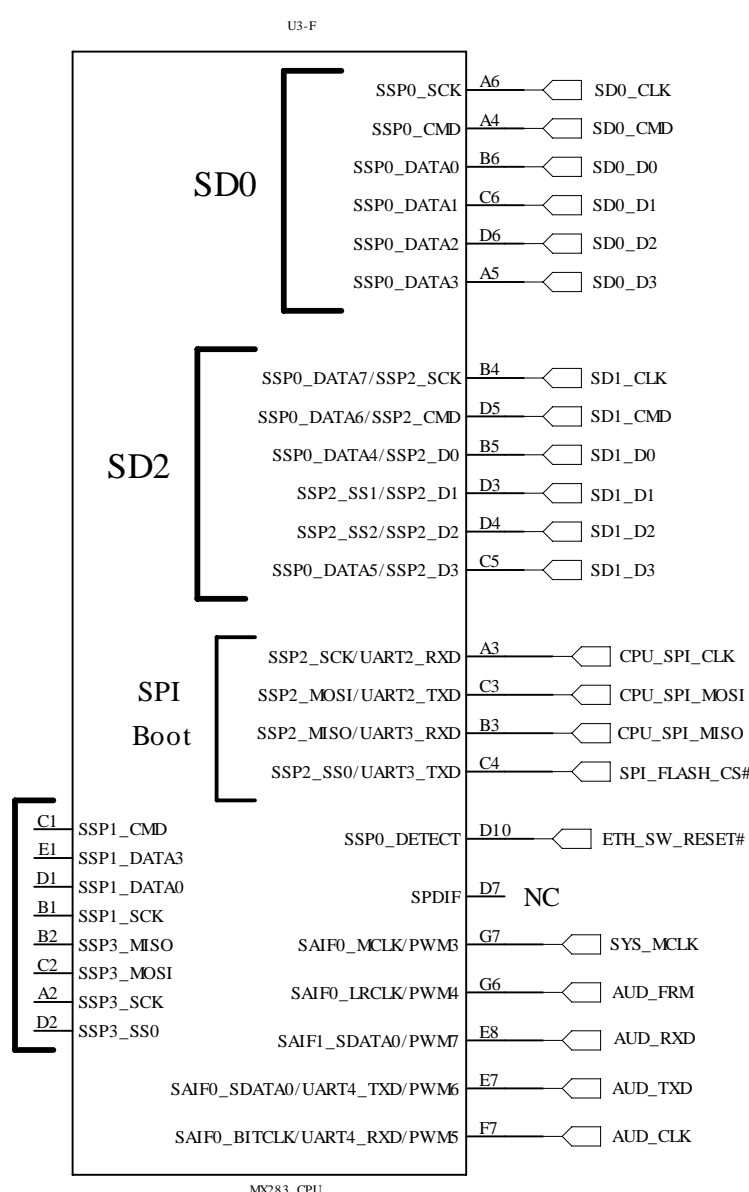
NC on MX283

LCD\_00 thru LCD\_04  
Control Boot Source

SPI = MSB 0 0 0 1 0 LSB

LCD\_05 and 06 bias low  
LCD\_RS biased high  
LCD\_RS low = use OTP  
See: EVK schematic, Page 15

## Audio SD Card SPI Boot



NC on MX283

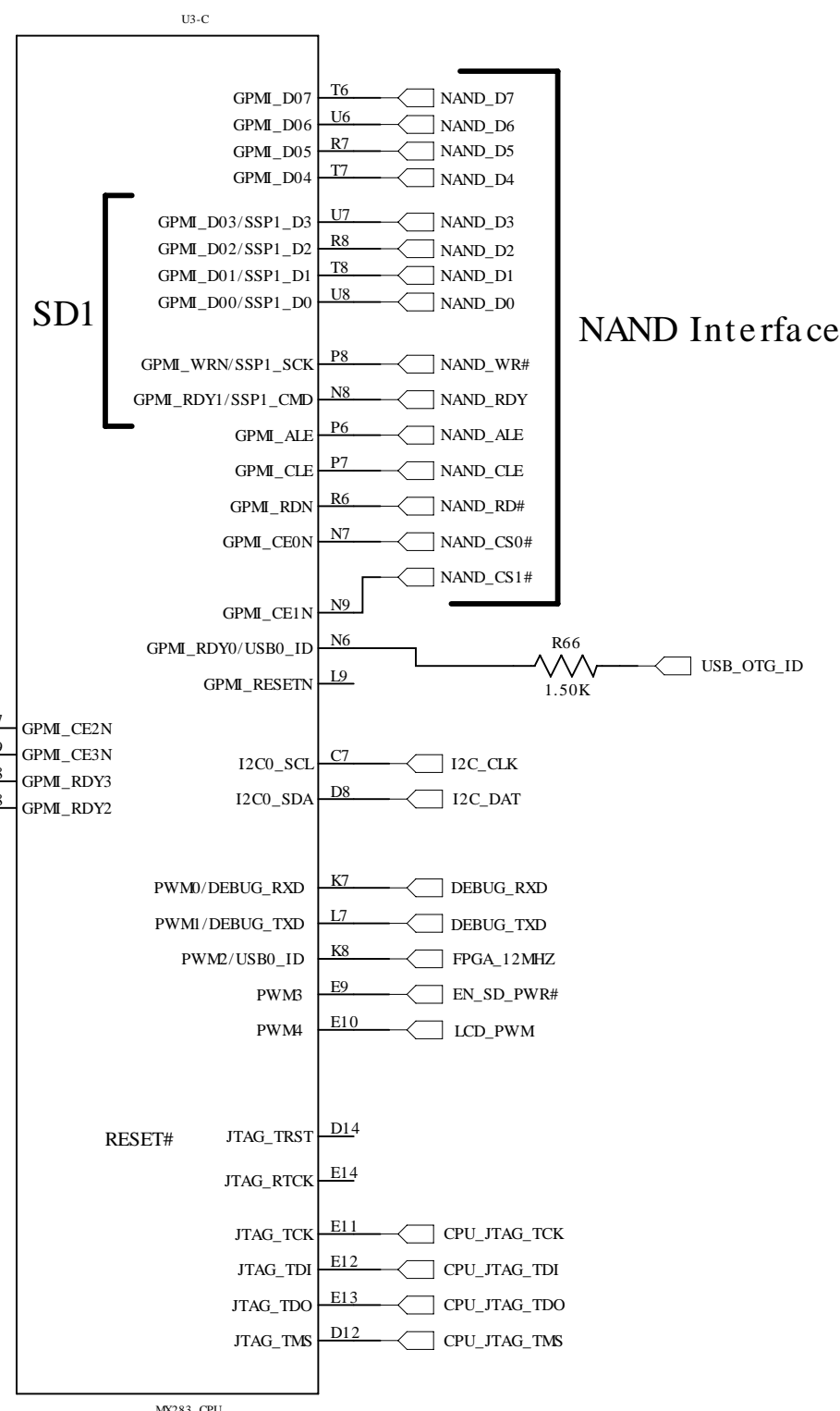
12 MHz default boot clock  
Max SPI clock rate = 20 MHz

U3.D3 and U3.D4 are extra  
2 data lines for SPI x4 read  
Page 1313 of Data sheet

Page 1311 - Winbond SPI x2 and x4 supported  
EVK schematic references a 8Mbit Winbond chip

## NAND, PWM JTAG, I2C

SPI  
SCK = CLK  
CMD = MOSI  
D0 = MISO  
D3 = CS#



NC on MX283

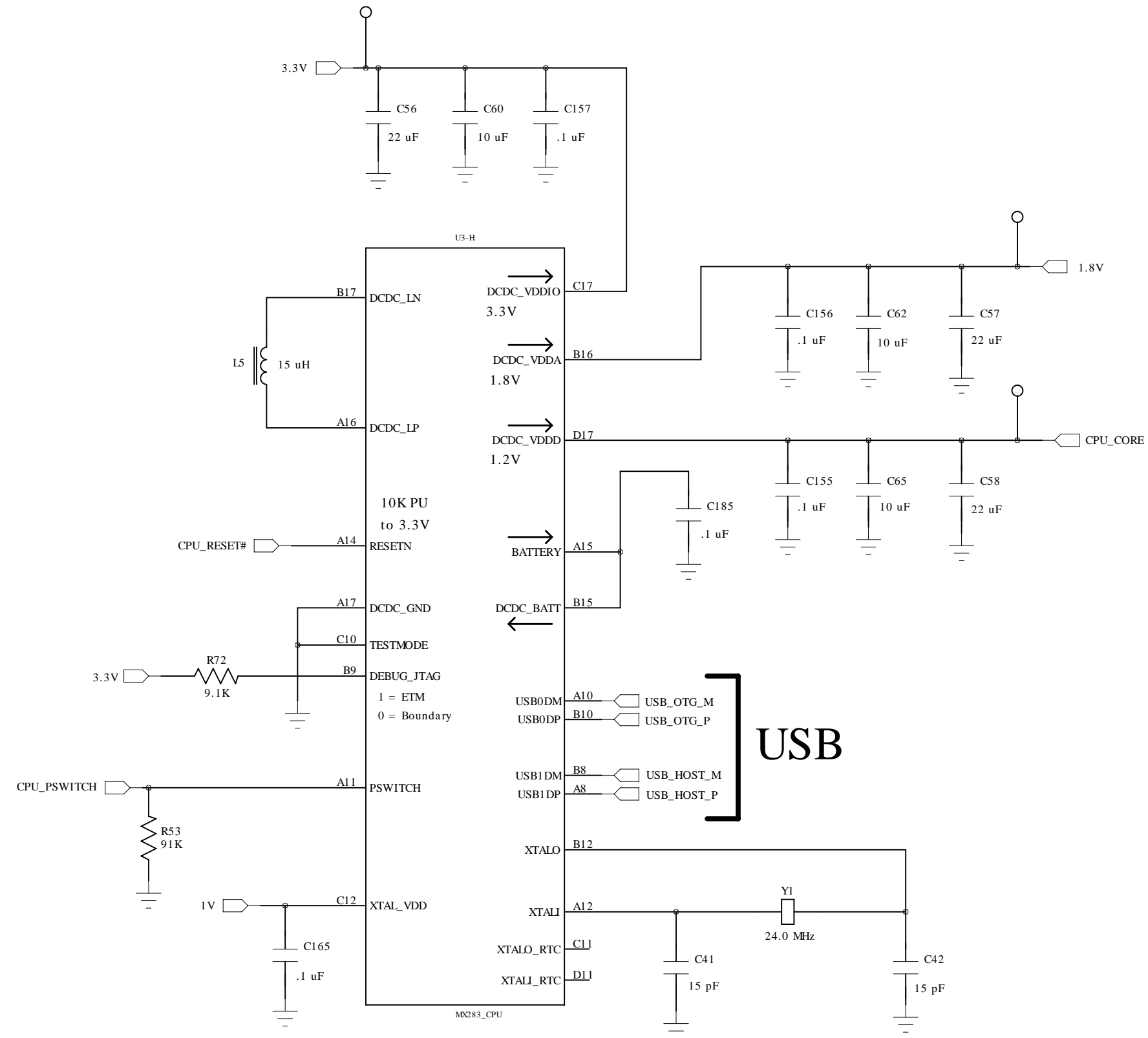
F3 is EVK ETH\_RESET#  
F5, F6 are EVK USB\_PWR\_EN  
E1 is EVK Eth\_PWR\_EN  
C7 and D8 = EVK I2C  
J5 is EVK USB\_0\_ID  
K8 is EVK LCD PWM  
K7 and L7 are EVK console

E10 is EVK SD1\_PWR\_EN  
E9 is SD0\_PWR\_EN on both EVK and Green schematics

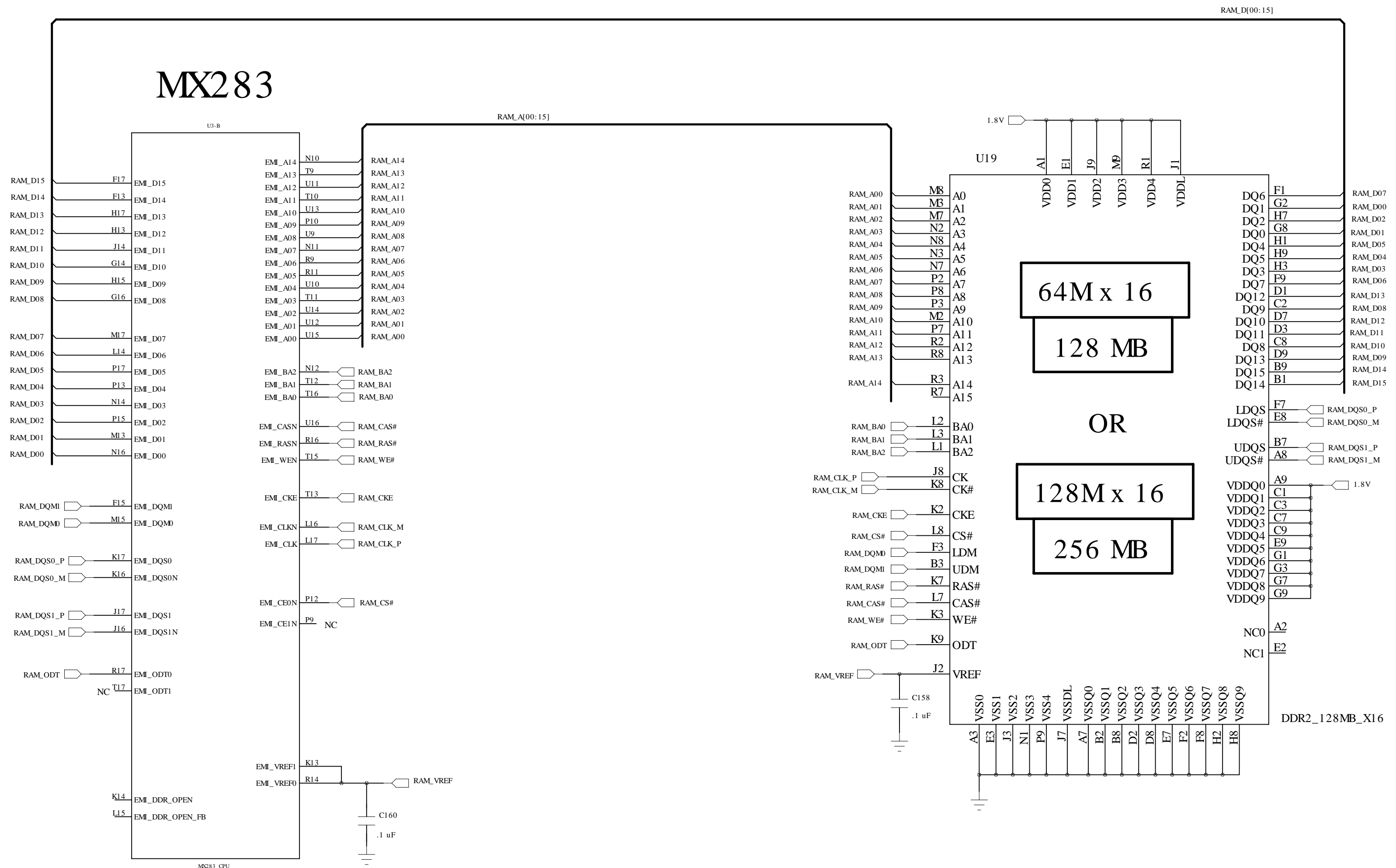
PWM outputs can be 24 MHz  
divided by 16-bit integer  
Allows clock 12MHz and lower

All JTAG have 47K internal PU except RTCK

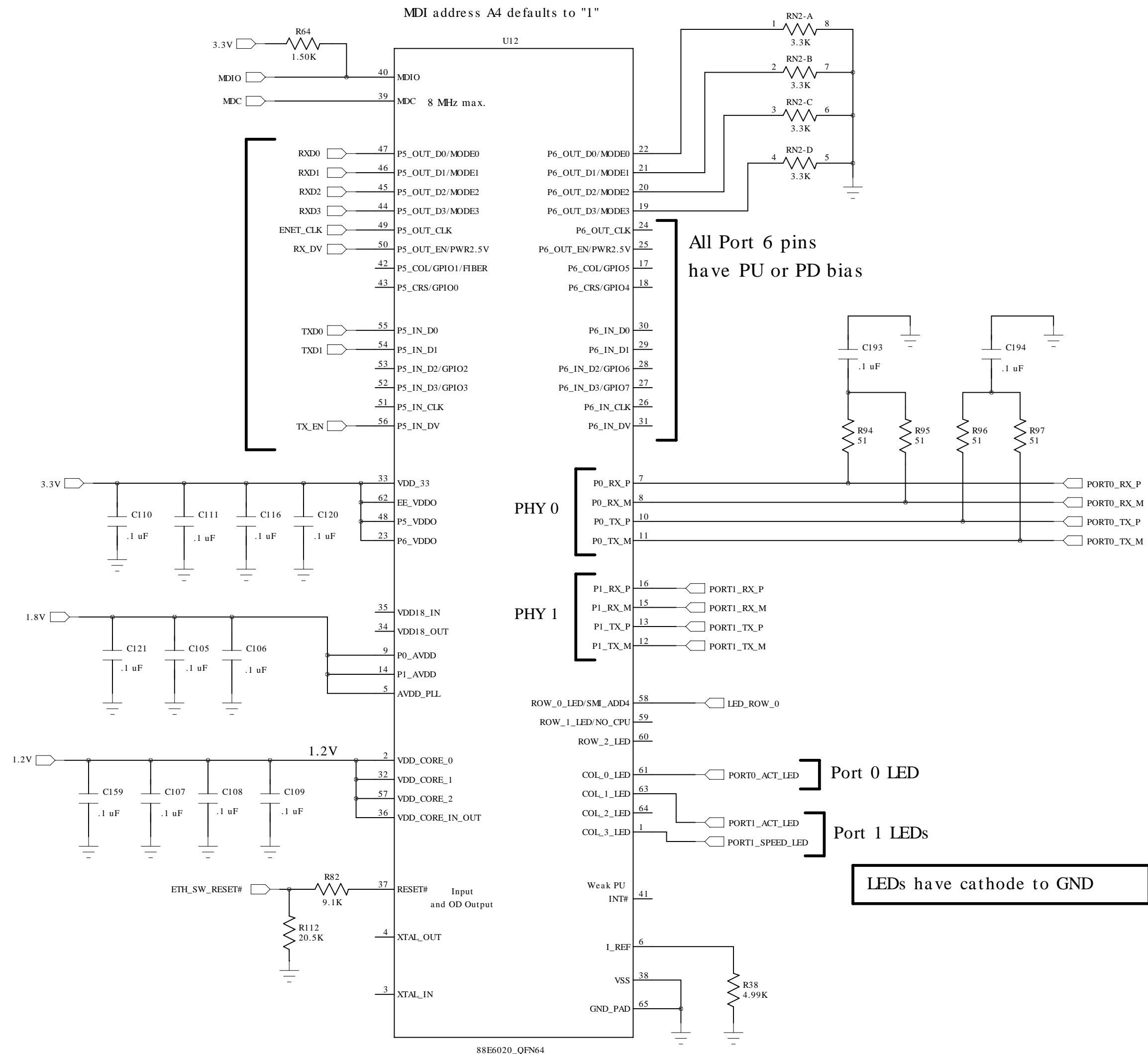
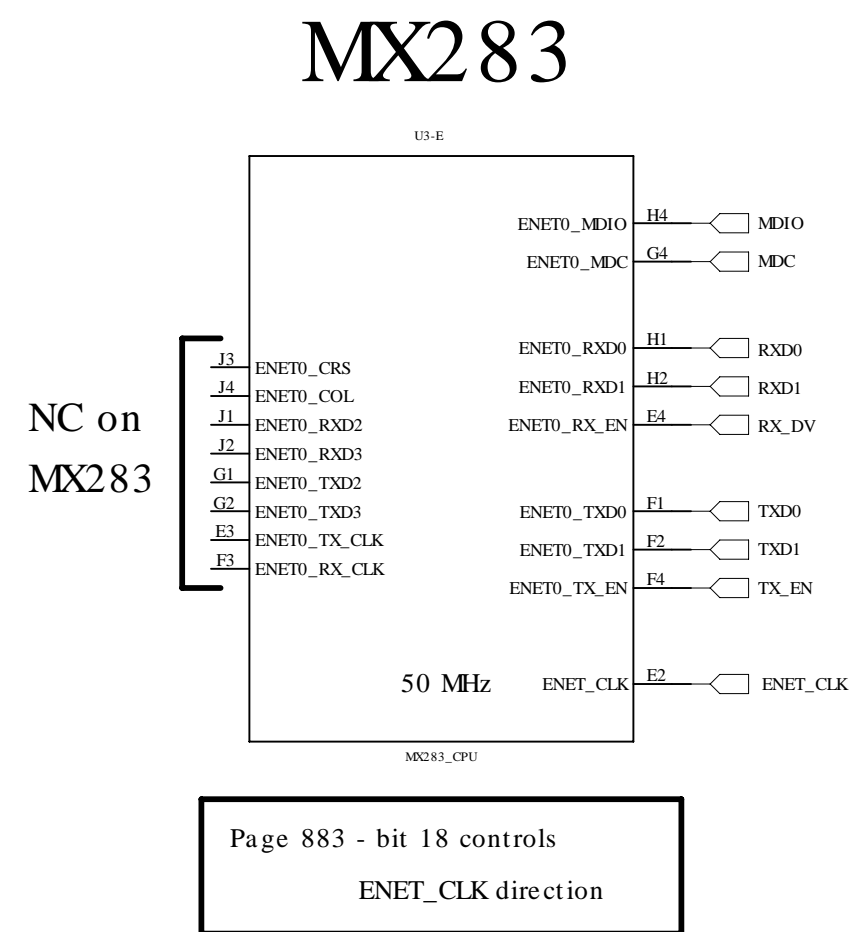
# CPU Power



# DDR2 SDRAM (128 or 256 MByte)



# 10/100 Ethernet 4-Port Switch

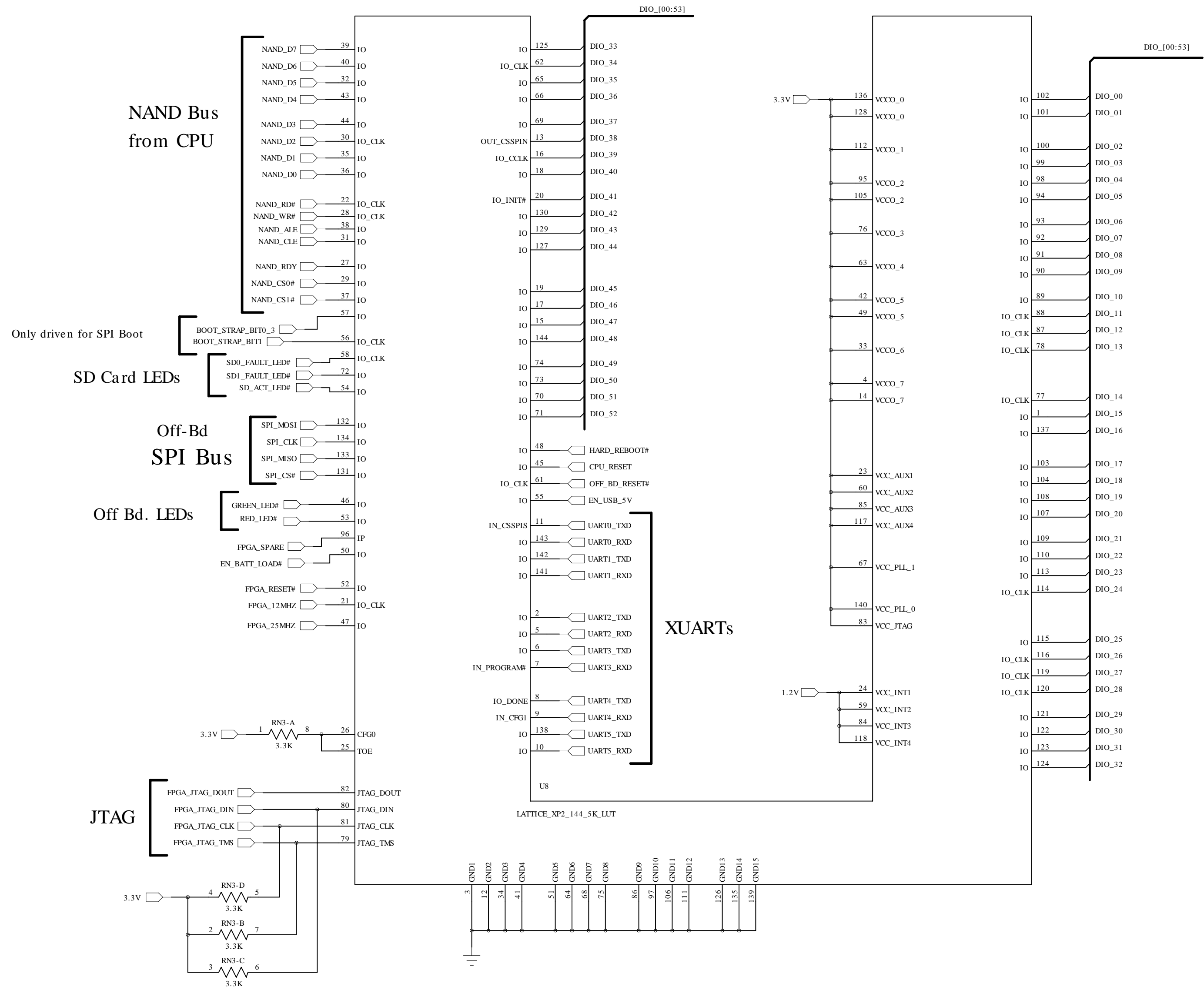


Total 88E6020 100 Mbit
Current Drain includes 2 Ports with Mag CT
3.3V Rail = 20 mA
1.8V Rail = 80 mA
1.2V Rail = 62 mA
Power Down mode
42 mA on 1.2V rail
0 mA on other rails

Auto MDIX is supported  
Polarity Correction also supported

Technologic Systems	Date Feb. 21, 2014
Title: TS-4600 Ethernet Switch	
Rev: A	Designer
Sheet 4 of 9	

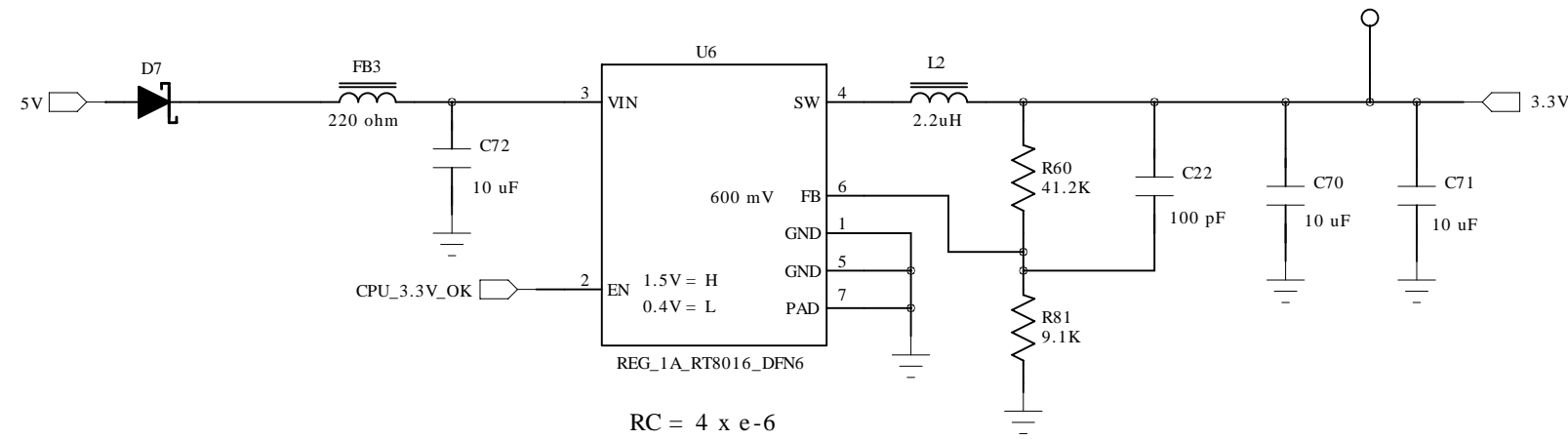
# FPGA with 5K LUTs



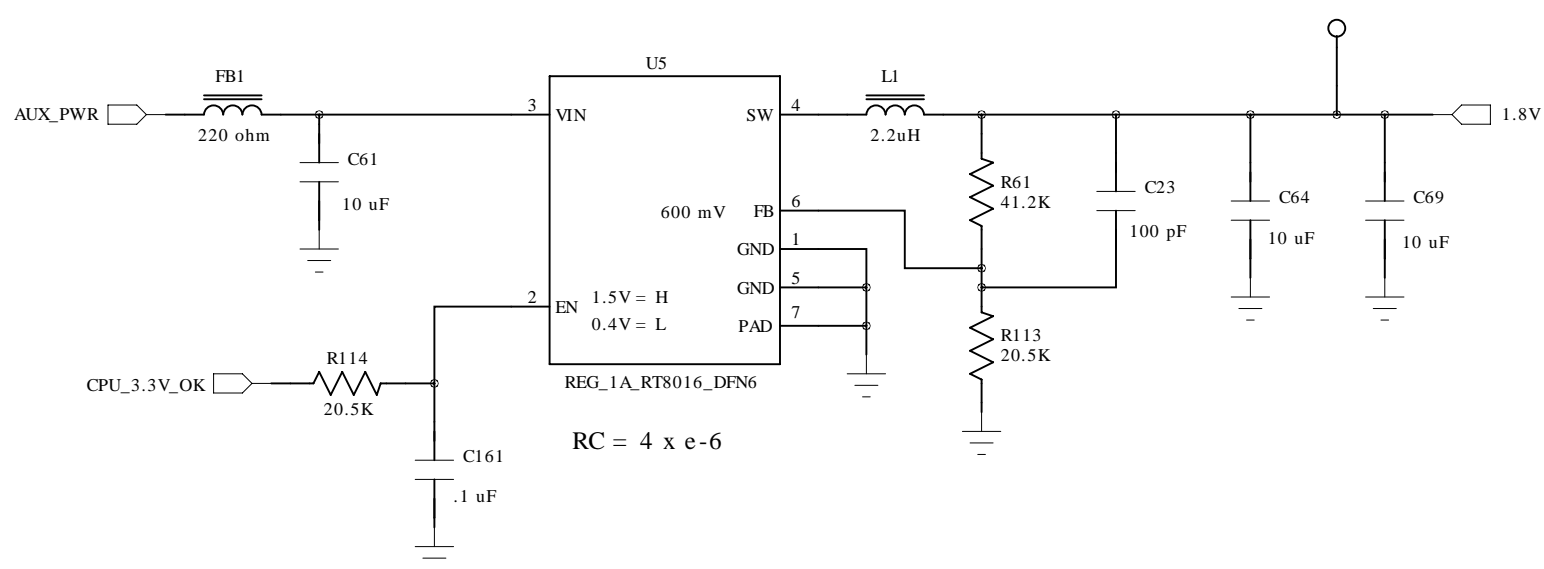
DIO\_09 is sometimes a Push switch input

# Boot Strap Bias Res.

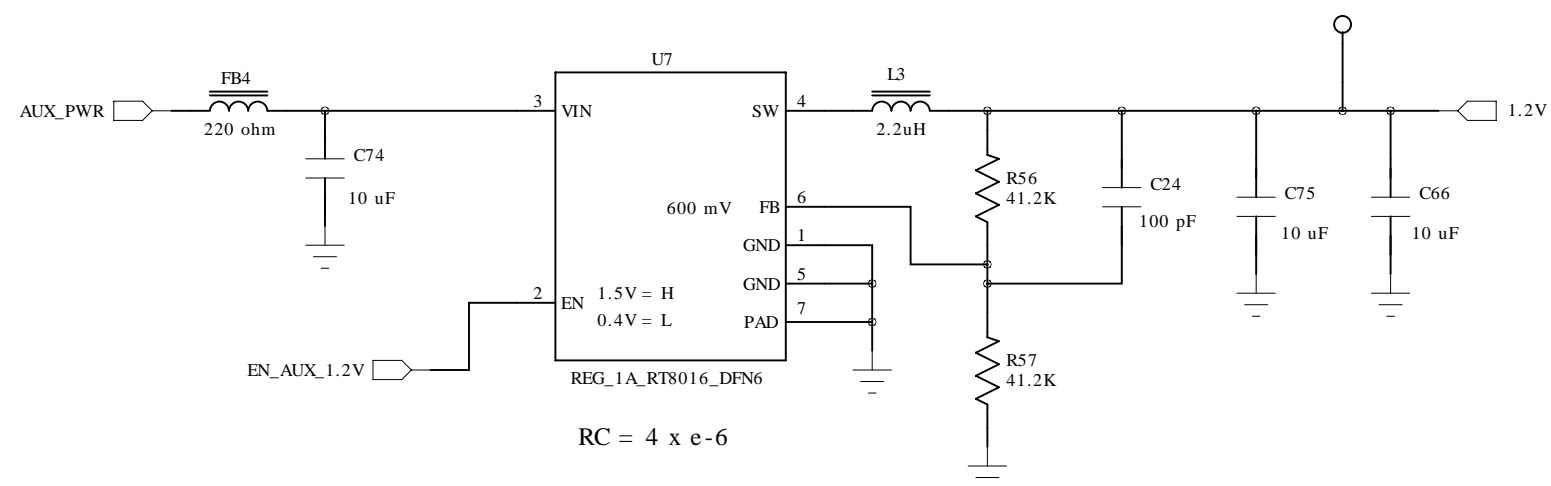
## 3.3V Reg



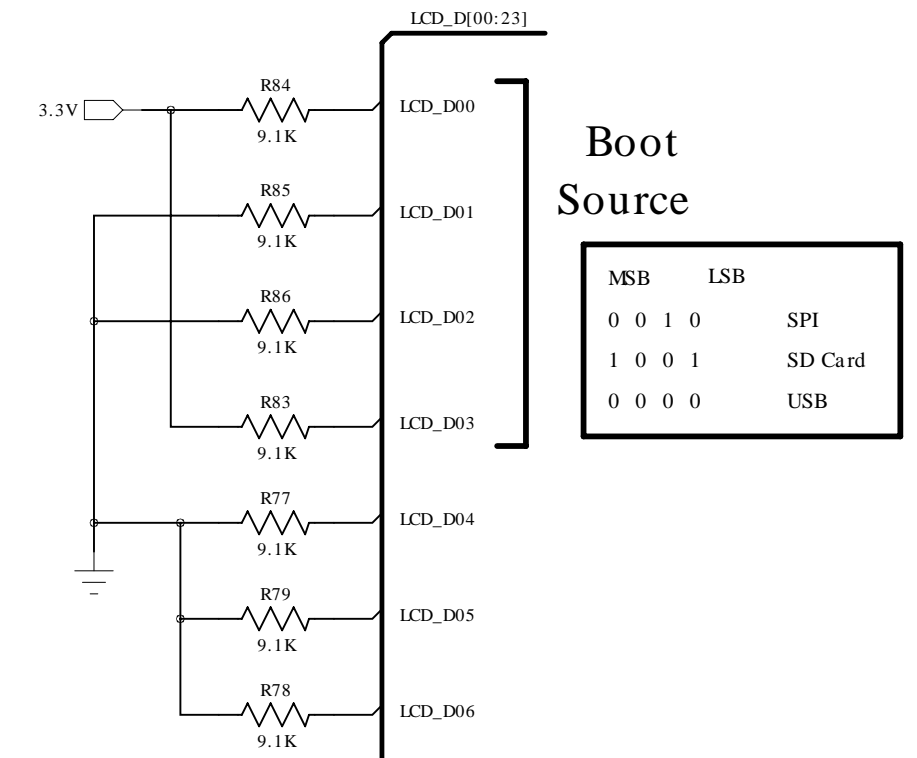
## 1.8V Reg



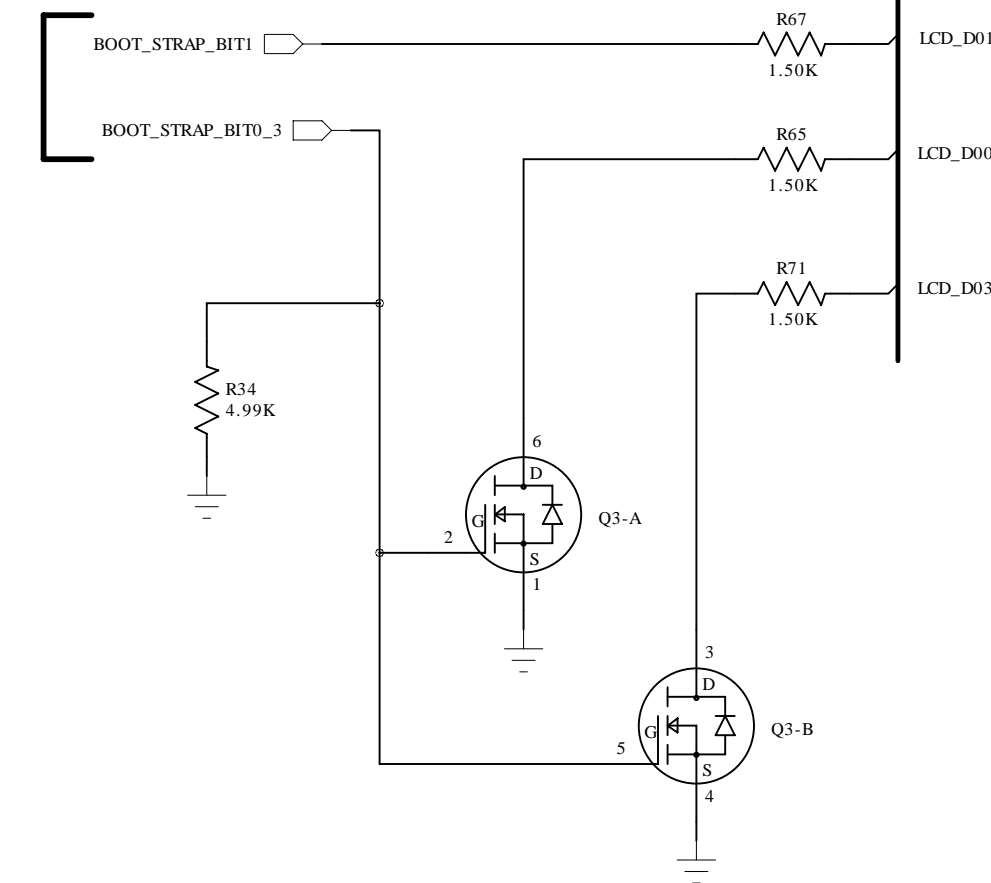
## 1.2V Reg.



Defaults  
to SD Card



FPGA can force  
SPI Flash Boot  
or USB Boot



GND Test Point

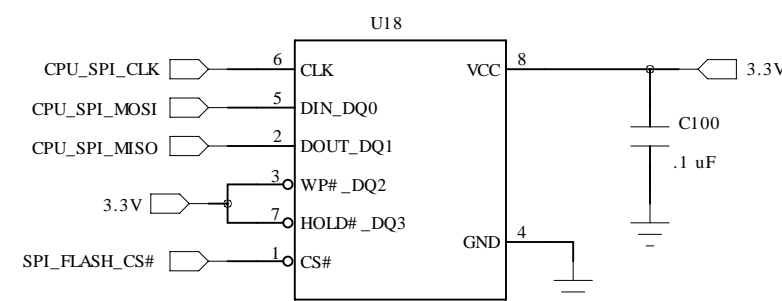


Technologic Systems	Date Feb. 21, 2014
Title: TS-4600 Power Reg. and Boot Straps	
Rev: A	Designer
Sheet 6 of 9	

# MX283 SPI Boot

# and FPGA Config Flash

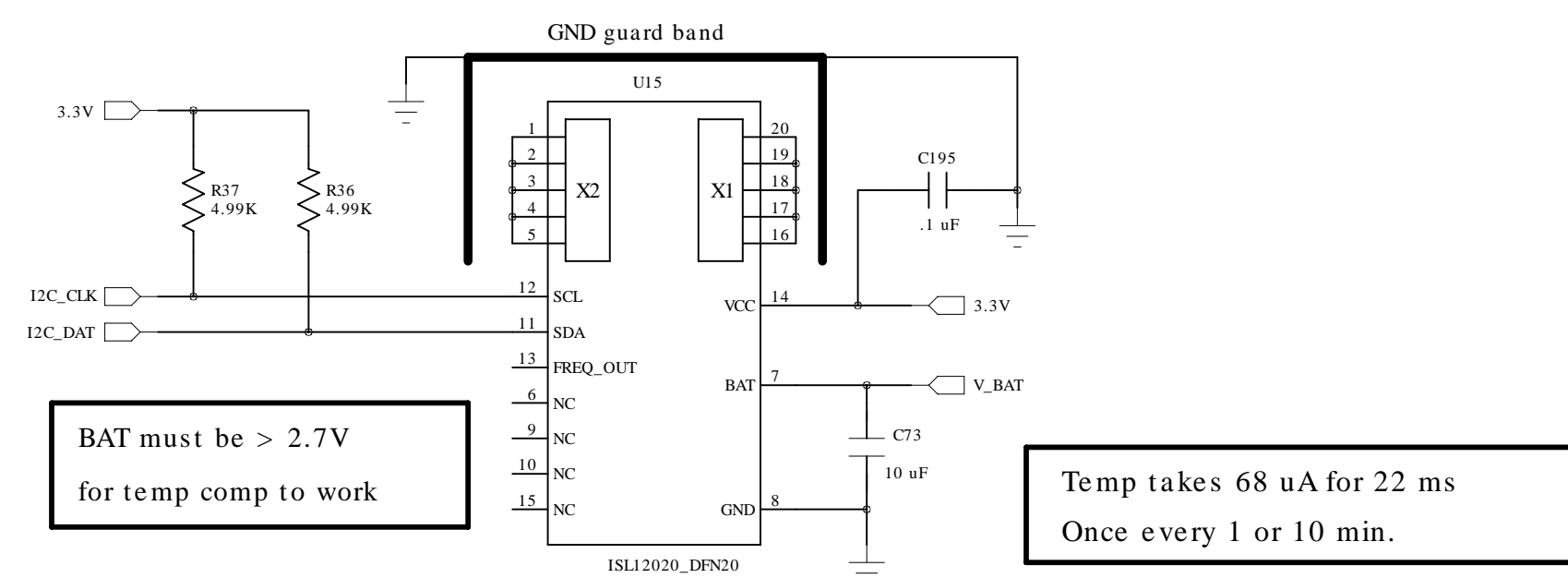
## SPI Boot Flash



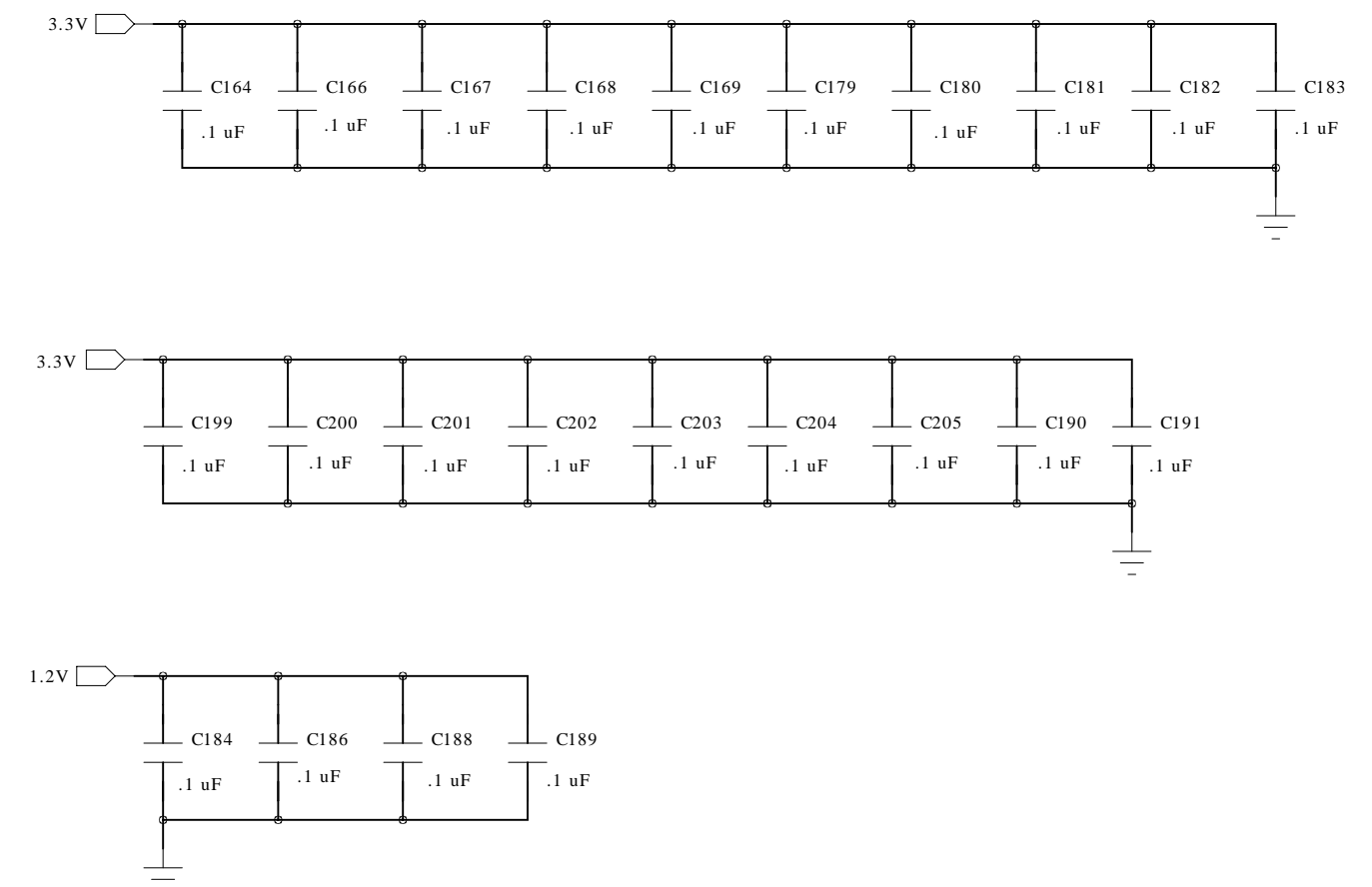
64 bytes of OTP

Not Populated ?

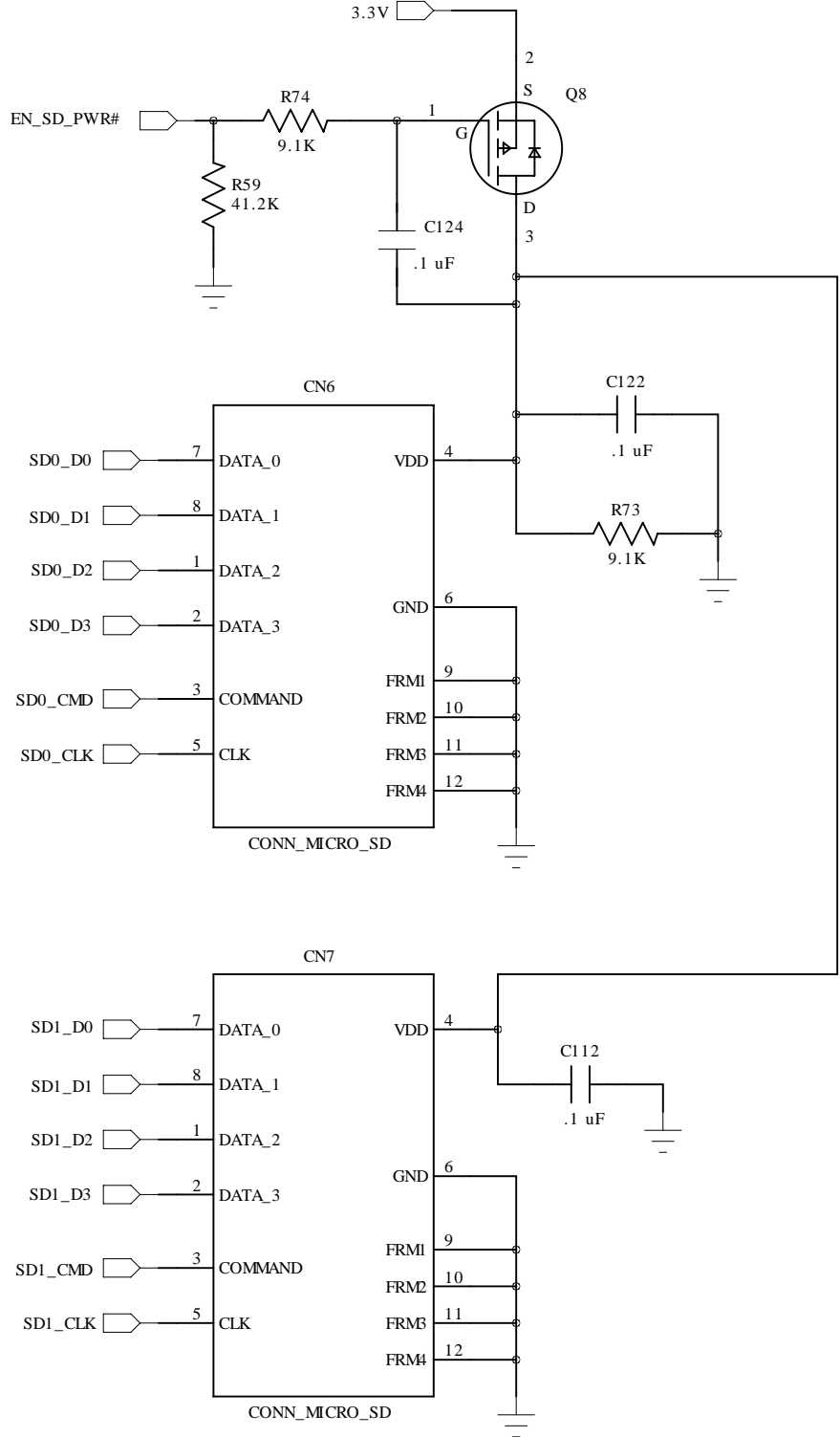
## RTC and Temp. Sensor



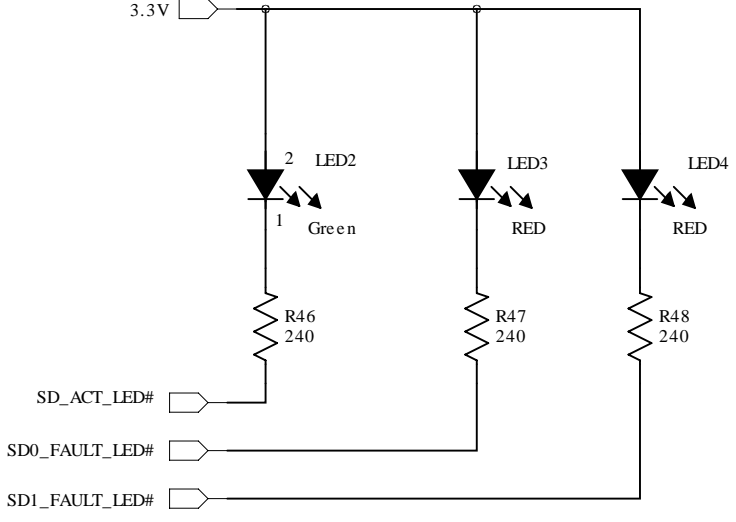
## FPGA Bypass Caps



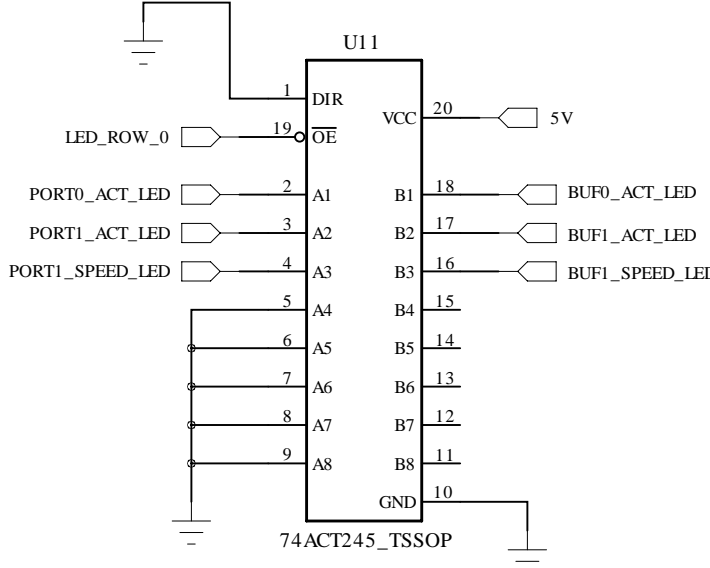
# Micro SD Card Sockets



# SD LEDs



# Ethernet LED Buffer





# Two 100-pin Off-board Connectors

"POWER" pins supply all power to the module  
Apply 4.5V to 5.5V to these pins

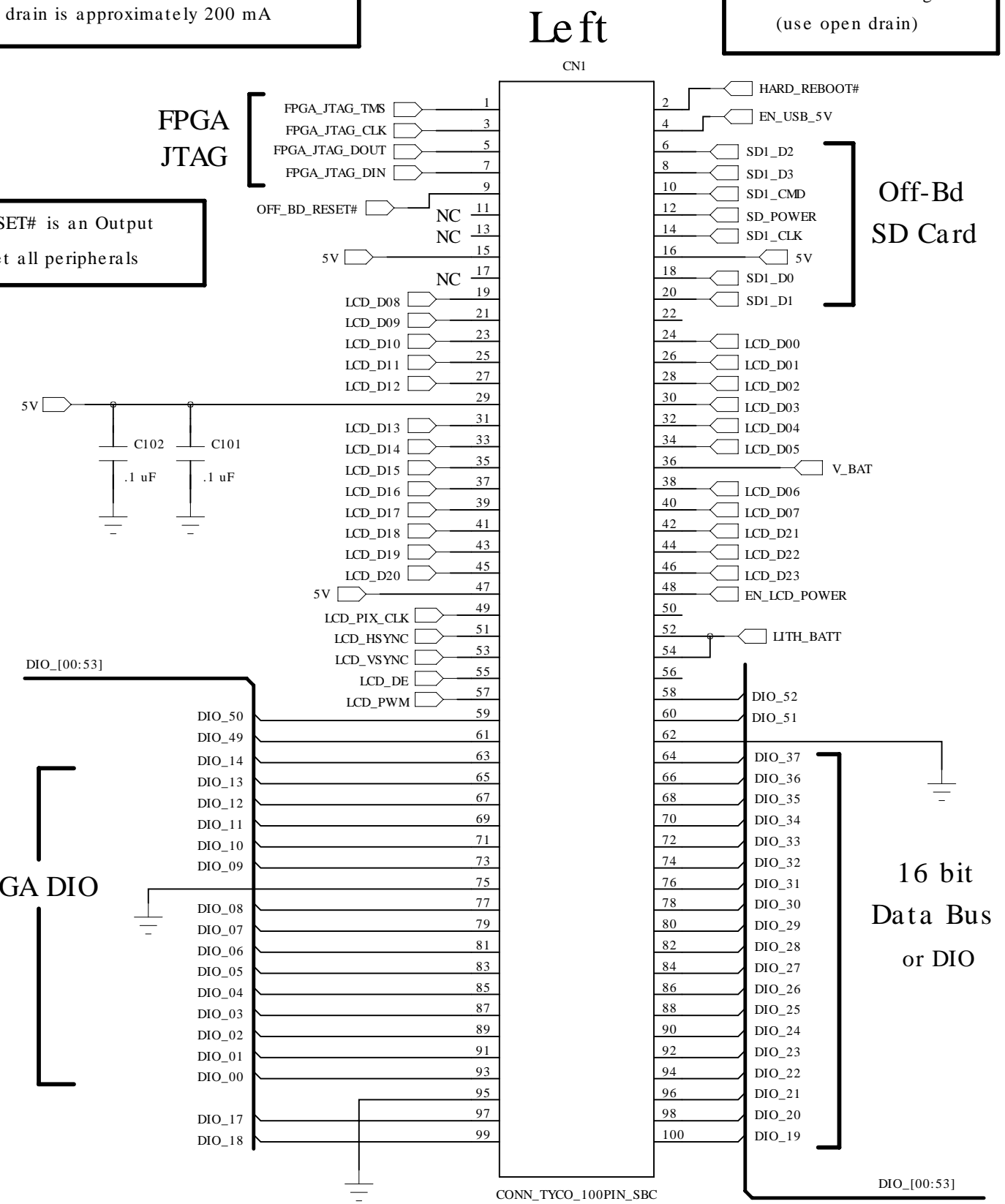
Current drain is approximately 200 mA

REBOOT# is an Input  
used to reboot the CPU

Do not drive active high  
(use open drain)

**!** All signals driving DIO on CN1 & CN2 must be powered by the 3.3V on CN2, or remain at 0V until the CN2 3.3V rail is > 3.0V

OFF\_BD\_RESET# is an Output  
used to reset all peripherals



FPGA DIO

16 bit  
Data Bus  
or DIO

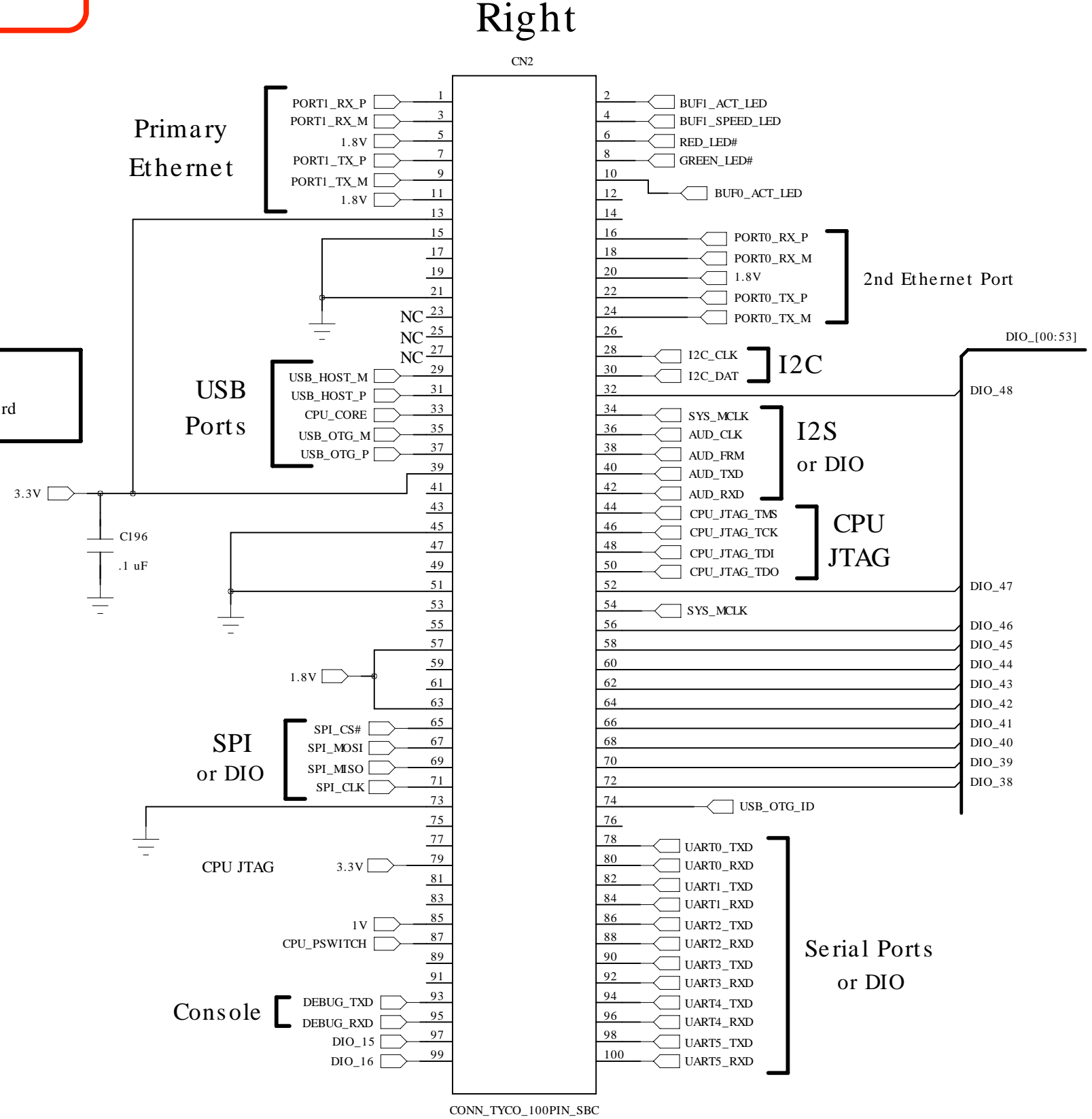
DIO\_[00:53]

If Bus is not needed, all Bus  
signals can be changed to DIO

Devices connected to this bus must never  
drive it when BUS\_CS# is deasserted  
(must be off within 30 nS of deassertion)

Devices must pull the BUS\_WAIT# line low  
if they need more than 150 nS strobe

3.3V rail can supply up  
to 400 mA to base board



Primary  
Ethernet

USB  
Ports

SPI  
or DIO

Console

2nd Ethernet Port

I2C

I2S  
or DIO

CPU  
JTAG

Serial Ports  
or DIO