Rev. A Problems:
- Ethernet LEDs wrong!
- No CAN connected
- No A/D connected
- Add WiFi!
- Add low power modes?
- Pwr switch to PHY?
- Remove FPGA?

Audio
SD Card
SPI Boot

UARTs, ADC

NAND, PWM
JTAG, I2C

Max SPI clock rate = 20 MHz

12 MHz default boot clock

NC on MX283

NC on MX283

NC on MX283

NC on MX283

NC on MX283

NC on MX283

NC on MX283

NC on MX283

NC on MX283
Battery pin supplies current to charge battery

DCDC_BAT pin is power input for DCDC converters - connect direct to battery

FPGA is fully functional when CPU Reset# deasserted

PSWITCH can be driven to 3.3V if a series 10K resistor is used
DDR2 SDRAM (128 or 256 MByte)

MX283

Length of this trace is equal to [CLK + Data] lengths
Data = Average length of all data traces

64M x 16
128 MB

OR

128M x 16
256 MB

Date: May 20, 2014
Title: TS-4600 DDR2 RAM
Rev: B
Designer
Sheet 3 of 9
10/100 Ethernet 4-Port Switch

MX283

Strapped for RMI MAC mode with 3.3V Levels

3.3V → 1.8V

Auto MDIX is supported
Polarity Correction also supported

Port 1 LEDs

Port 0 LEDs

All Port 6 pins have PU or PD bias

Pull-downs default P6 to port disabled mode

Power up with no config

Do Not Populate

LEDs have cathode to GND

Enet CL K direction

50 MHz

NC on MX283

Page 883 - bit 18 controls ENET_CLK direction
MX283 SPI Boot and FPGA Config Flash

### SPI Boot Flash

- **64 bytes of OTP**
- **Not Populated?**

### Reset Sequencer

- **20 ms delay**

### RTC and Temp. Sensor

- **BAT must be > 2.7V for temp comp to work**
- **Temp takes 68 uA for 22 ms Once every 1 or 10 min.**

### FPGA Bypass Caps
Micro SD Card Sockets

SD LEDs

Ethernet LED Buffer
"POWER" pins supply all power to the module
Apply 4.5V to 5.5V to these pins

Current drain is approximately 200 mA

OFF_BD_RESET# is an Output
used to reset all peripherals
Do not drive active high (use open drain)

Current drain is approximately 200 mA

FPGA DIO

5V

DIO_00
DIO_01
DIO_03
DIO_06
DIO_07
DIO_08
DIO_10
DIO_11
DIO_12
DIO_13
DIO_14
DIO_49
DIO_50
DIO_51
DIO_18 DIO_19

C101
C102

OFF_BD_RESET#
FPGA JTAG_DOUT
FPGA JTAG_TMS
FPGA JTAG_DIN

LCD_PIX_CLK
LCD_VSYNC
LCD_D20
LCD_D19
LCD_D18
LCD_D17
LCD_D15
LCD_D14
LCD_D11
LCD_D10
LCD_D09
LCD_D08

USB_HOST_M
USB_HOST_P
USB_OTG_M
USB_OTG_P
PORT0_TX_P
PORT0_RX_M
PORT0_RX_P

USB HOST M
PORT1_RX_M
PORT1_TX_M
PORT1_TX_P

HD44780

EN_USB_5V
EN_LCD_POWER

I2C_DAT
I2C_CLK
AUD_RXD
AUD_TXD
AUD_CLK

CPU_JTAG_TDI
CPU_JTAG_TCK
CPU_JTAG_TM S

I2C or DIO
Serial Ports or DIO

CPU or DIO

FPGA JTAG

16 bit Data Bus or DIO

Off-Bd SD Card

Primary Ethernet

USB Ports

2nd Ethernet Port

CPU JTAG

12C

UART0_TXD
UART1_TXD
UART1_RXD
UART0_RXD
UART2_TXD
UART2_RXD
UART3_TXD
UART3_RXD
UART4_RXD
UART4_TXD
UART5_TXD

3.3V and can supply up to 400 mA to base board

May 20, 2014

Title: TS-4600 100 pin Connectors

Rev: B Designer

Sheet 9 of 9

Technologic Systems