MAX283 ARM®9 CPU

UARTs, ADC

NAND, PWM

JTAG, I2C

Audio

SD Card

SPI Boot

MX283 ARM®9 CPU

Rev. A Problems:

Ethernet LEDs wrong!
No CAN connected
No A/D connected
Add WiFi!
Add low power modes?
Pwr switch to PHY?
Remove FPGA?

See Page 2263

Page 1311 - Winbond SPI i2 and i4 supported
EVK schematic references a 3MHz Winbond chip

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12 MHz default boot clock
Max SPI clock rate ≈ 20 MHz

U3.3D and U3.4D are extra
2 data lines for SPI s4 read
Page 1313 of Data sheet

PWM outputs can be 24 MHz divided by 16-bit integer
Allows clock 12MHz and lower

Page 1311 - Winbond SPI i2 and i4 supported
EVK schematic references a 3MHz Winbond chip

Technologic Systems

Date: May 20, 2014

Title: TS-4600 MAX283 CPU

Rev: B

Designer

Sheet 1 of 9
Battery pin supplies current to charge battery.

DCDC_BAT pin is power input for DCDC converters -- connect direct to battery.

FPGA is fully functional when CPU Reset# deasserted.

PSWITCH can be driven to 3.3V if a series 10K res is used.
DRR2 SDRAM  (128 or 256 MByte)

Length of this trace is equal to [CLK + Data] lengths
Data = Average length of all data traces
"0111" = RMII MAC mode

3.3V → 1.8V

Auto MDIX is supported
Polarity Correction also supported
The page describes various FPGA signals and their functions, including DIO_05 returns values, DIO_20 is latched when OFF_BD_RESET# is deasserted, 0 = SD Card Boot, 1 = SPI Flash Boot. It also mentions AUX_3.3V power supply and SPI flash boot setup.
MX283 SPI Boot and FPGA Config Flash

SPI Boot Flash

64 bytes of OTP
Not Populated?

RTC and Temp. Sensor

FPGA Bypass Caps

BAT must be > 2.7V for temp comp to work
Temp takes 68 uA for 22 ms Once every 1 or 10 min.
Micro SD Card Sockets

SD LEDs

Ethernet LED Buffer
Two 100-pin Off-board Connectors

"POWER" pins supply all power to the module. Apply 4.5V to 5.5V to these pins.
Current drain is approximately 200 mA.

OFF BD RESET# is an Output used to reset the peripherals.

"POWER" pins supply all power to the module.
Apply 4.5V to 5.5V to these pins.
Current drain is approximately 200 mA.

REBOOT# is an Input used to reboot the CPU.
Do not drive active high (use open drain).

Must have 10 off-Capacitors very near CN2 and OBD for all "power" signals.
(Not next pin pair).

Pin 1 is the top left corner pin on the connector. All of the pins on the left are odd numbered. This may differ from the connector manufacture's datasheet.

3.3V rail can supply up to 400 mA to host board.

AUX_1.8V (between differential pairs)

16 bit Data Bus or DIO

If Bus is not needed, all Bus signals can be changed to DIO.

Devices connected to this bus must never drive it when BUS_CS# is deasserted (must be off within 50 nS of deassertion).

Devices must pull the BUS_WS/#W low if they need more than 150 nS strobe.

Any I/O routed to a user accessible connector should have additional ESD protection placed on the carrier board.

"POWER" pins supply all power to the module.