Two 100-pin Off-board Connectors

"POWER" pins supply all power to the module
Apply 4.5V to 5.5V to these pins
Current drain is approximately 400 mA

EXT_RESET# is an input
used to reboot the CPU
Do not drive active high
(see open drain)

OFF_RD_RESET# is an output
used to reset all peripherals

FPGA JTAG

FPGA DIO

Bus Control

Device connected to this bus must never
drive it when BUS_CS# is deasserted
(must be off within 30 nS of deassertion)

Devices must pull the BUS_WAIT# line low
if they need more than 150 nS strobe

The data bus can not have more than
30 pF of off-board capacitive loading
May need data buffer chip for heavy loads

If Bus is not needed, all Bus
signals can be changed to DIO

Boot Strap

Mode 2

TS-4700
Boots from
1 NAND Flash
0 SD Card

BUS_DIR = MODE2

Bus_DIR is asserted prior to
OFF_RD_RESET# deasserted

Connect 1.5K ohm resistor
between BUS_DIR and
OFF_RD_RESET# to set low
(Busfrom SD Card)

Connect I2C or DIO

USB Ports

SPI or DIO

Camera or DIO

Console

CAN

Gateway

DIO_10 and DIO_16
can be CAN_TXD
and CAN_RXD

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Title: TS-4700 Off-board Connectors
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