DDR3 RAM

Termination

Power Supply

Termination Resistors
FPGA with 5K or 8K LUTs

CPU

USB Power

SD Cards

SPI Bus

Reset Latch

FPGA 1.2V Reg.

SMC Bus

Off Bd. LEDs

From CPU

DDR 1.5V

EN

PGOOD

VIN

1.5-5.5V

L D39100PUR_DFN6

Off Bd. L EDs

U6

0.8V

from CPU

7PAD

5FB

2GND

4VOUT

1.20V typ.

3.3V

FPGA_RESET#

12.1K

R120

6.04K

R13

6.3V

10 uF

C44

.1 uF

C190

.1 uF

C163

10 nF

C216

SM C Bus

IN

10 I/O with 144 pin package

T S-4710 FPGA

Jan. 3, 2013

of Designer Rev: A

Sheet 5 of 10

Technologic Systems

Date Jan. 3, 2013

Title: TS-4710 FPGA
Power Supplies

# 1 3.3V Power Supply

Up to 2000 mA

Power Supply Sequence:
- When POWER < 4.1V all rails are OFF
- After POWER is > 4.1V
  - Then wait 200 ms
  - Turn on 3.3V Rail
  - Wait 4 ms
  - Then enable:
  - #4 DDR 1.5V Rail
  - #3 FPGA 1.2V ramps simultaneously with DDR 1.5V
  - #6 FPGA controls delay until AVID_OTG rail is enabled

# 2 Analog

1.8V Regulator

# 3 CPU Core Supply

Delay from Blinks to Power up is approx. 50 ms

# 4 DDR3 1.5V Reg.

Technologic Systems
Date Jan. 3, 2013
Title: TS-7110 Power Supplies
Rev: A Designer Sheet 6 of 10
CPU Power

PXA168 PCIe rails must be connected to AVDD OSC (1.8V)

CPU

3.3V

CPU_CORE

DDR_1.5V

AVDD_OTG

AN_1.8V

SBC_USB_5V
Micro SD Card Sockets

RTC and Temp. Sensor

CPU

Debug UART

Reboot Flag

SD Card LEDs

3.3V --> 5V Level Shifter

OFF BD. SD Card Power

- BAT must be > 2.7V for temp comp to work
- Temp takes 68 uA for 22 ms Once every 1 or 10 min.

- Keep normally at logic zero

- 3.3V --> 5V for logic zero

- Micro SD Card Sockets

- CPU

- Debug UART

- Reboot Flag

- SD Card LEDs

- 3.3V --> 5V Level Shifter

- OFF BD. SD Card Power

Technologic Systems
Date Jan. 3, 2013
Title: TS-4710 SD card, RTC, Temp.
Rev: A Designer Sheet 8 of 10
PCIe 100 MHz Clock Generator

12C interface allows changing amplitude and tri-stating outputs

Spread Spectrum En.

CPU PCIe

PCIe not supported on PXA166

Inputs

Temp Readout

Technologic Systems Date Jan. 3, 2013
Title: TS-4710 PCIe Clock and CPU PCIe
Rev: A Designer Sheet 9 of 10
Two 100-pin Off-board Connectors

“POWER” pins supply all power to the module. Apply 4.5V to 5.5V to these pins.

 Current drain is approximately 400 mA

EXT_RESET# is an Input used to reset the CPU. Do not drive active high (but open circuit).

EXT_RESET# is an Output used to reset all peripherals.

Max. source 20mA of Output for all “power” signals (between chip pairs).

Bus Control

If Bus is not needed, all Bus signals can be changed to DIO.

Any I/O routed to a user accessible connector should have additional ESD protection placed on the carrier board.

Devices connected to this bus must never drive it when BUS_CM is deasserted (must be off within 50 nS of deassertion).

Devices must pull the BUS_3.3V low if they need more than 150 nS strobe.

The data bus can not have more than 30 pF of off-board capacitive loading. May need data buffer chip for heavy loads.

Off-Bd Reset is an Output used to reset the CPU. Do not drive active high (but open circuit).

Apply 4.5V to 5.5V to these pins.

“POWER” pins supply all power to the module.

Camera drain is approximately 400 mA

Current drain is approximately 400 mA

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FPGA

SD Card

Ethernet

USB

SPI

Camera

Serial Ports

Technologic Systems

Date: Jan. 3, 2013

Title: TS-4710 Off-board Connectors

Rev: A    Designer    Sheet: 10 of 10