DDR3 RAM
Termination
Power Supply

Termination
Resistors
10/100 Ethernet

CPU

LED1 = Activity/Link
LED2 = Speed 100 Mbit

Technologic Systems
Title: TS-4710 Ethernet
Date Jan. 3, 2013
Rev. A
Designer RLM
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# 1 3.3V Power Supply  up to 2000 mA

Power Supply Sequence:

When POWER < 4.1V all rails OFF
After POWER > 4.1V

Then wait 200 ms

# 1 Turn on 3.3V Rail

# 2 AVDD (1.8V) is always slightly lower than 3.3V rail

Then wait 4 ms, and enable

# 3 CPU Core rail

Wait 4 ms, then enable

# 4 DDR 1.5V Rail

# 5 FPGA 1.2V ramps simultaneously

with DDR_1.5V rail

# 6 FPGA controls delay until

AVDD_OTG rail is enabled

All Power rails are turned off at the same time (within 5 ms)

# 2 1.8V Regulator

# 3 CPU Core Supply

# 4 DDR3 1.5V Reg.
CPU Power

PXA168_PCIE rails must be connected to AVDD_OSC (1.8V)

CPU

CPU_CORE

3.3V

AN_1.8V

SBC_USB_5V
**Micro SD Card Sockets**

**RTC and Temp. Sensor**

**CPU**

- Debug UART
- (Console)

**Reboot Flag**

- Temp takes 68 uA for 22 ms
- Once every 1 or 10 min.

**SD Card LEDs**

**3.3V --> 5V Level Shifter**

**OFF BD. SD Card Power**

- BAT must be > 2.7V for temp comp to work
I2C interface
allows changing amplitude
and tri-stating outputs

Spread Spectrum En.