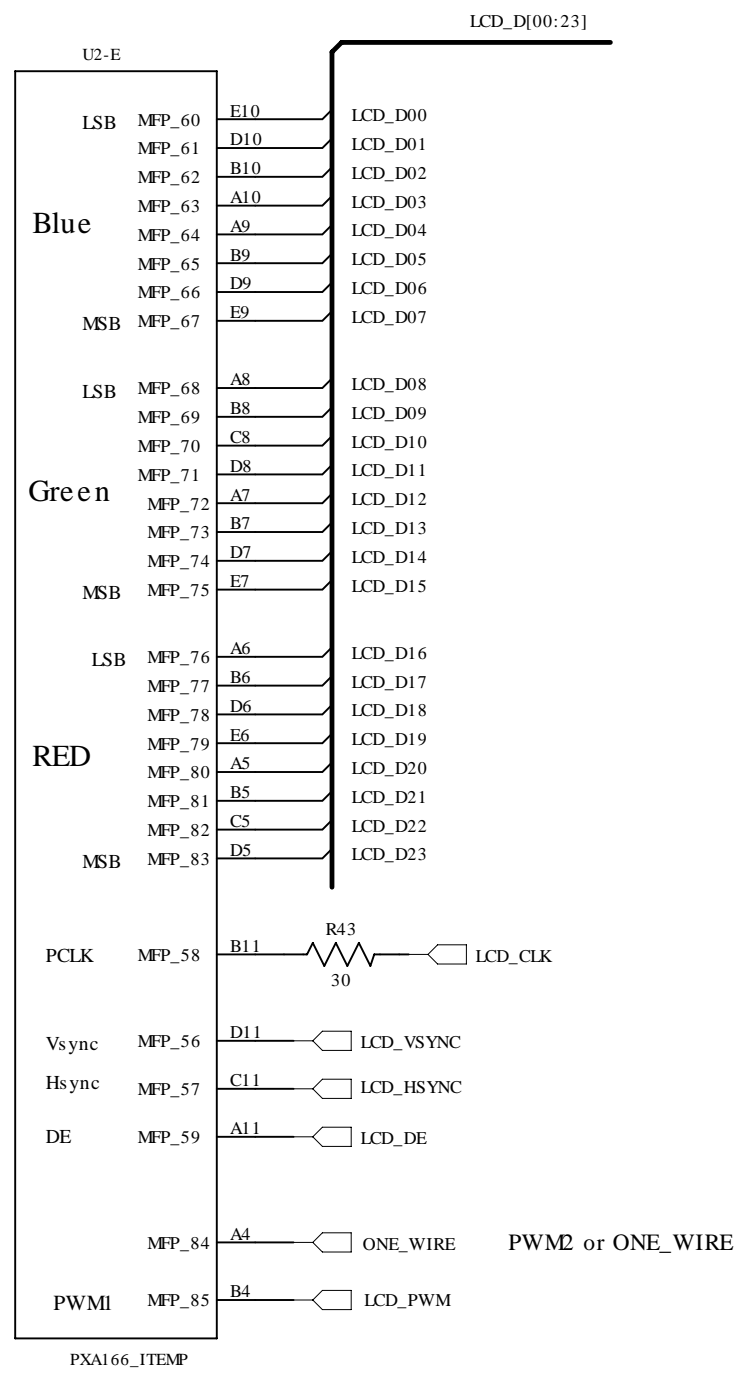
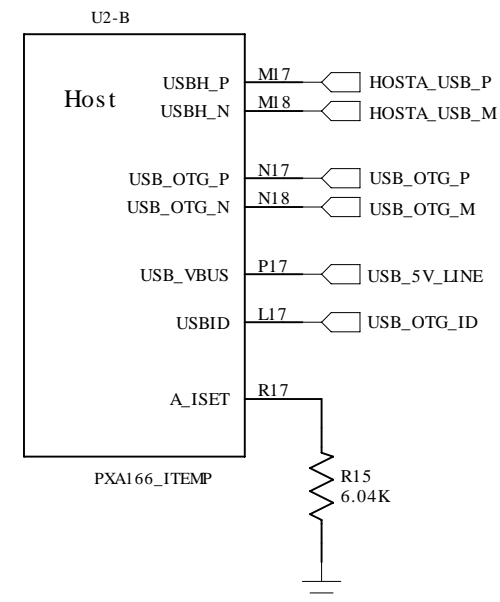


PXA166 800 MHz - PXA168 1066 MHz

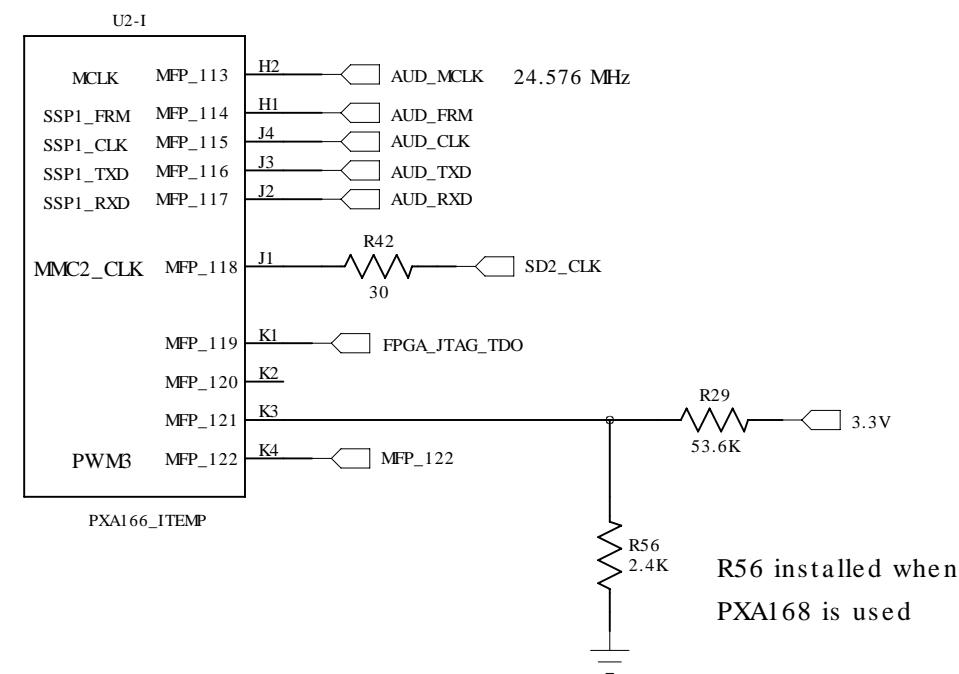
LCD



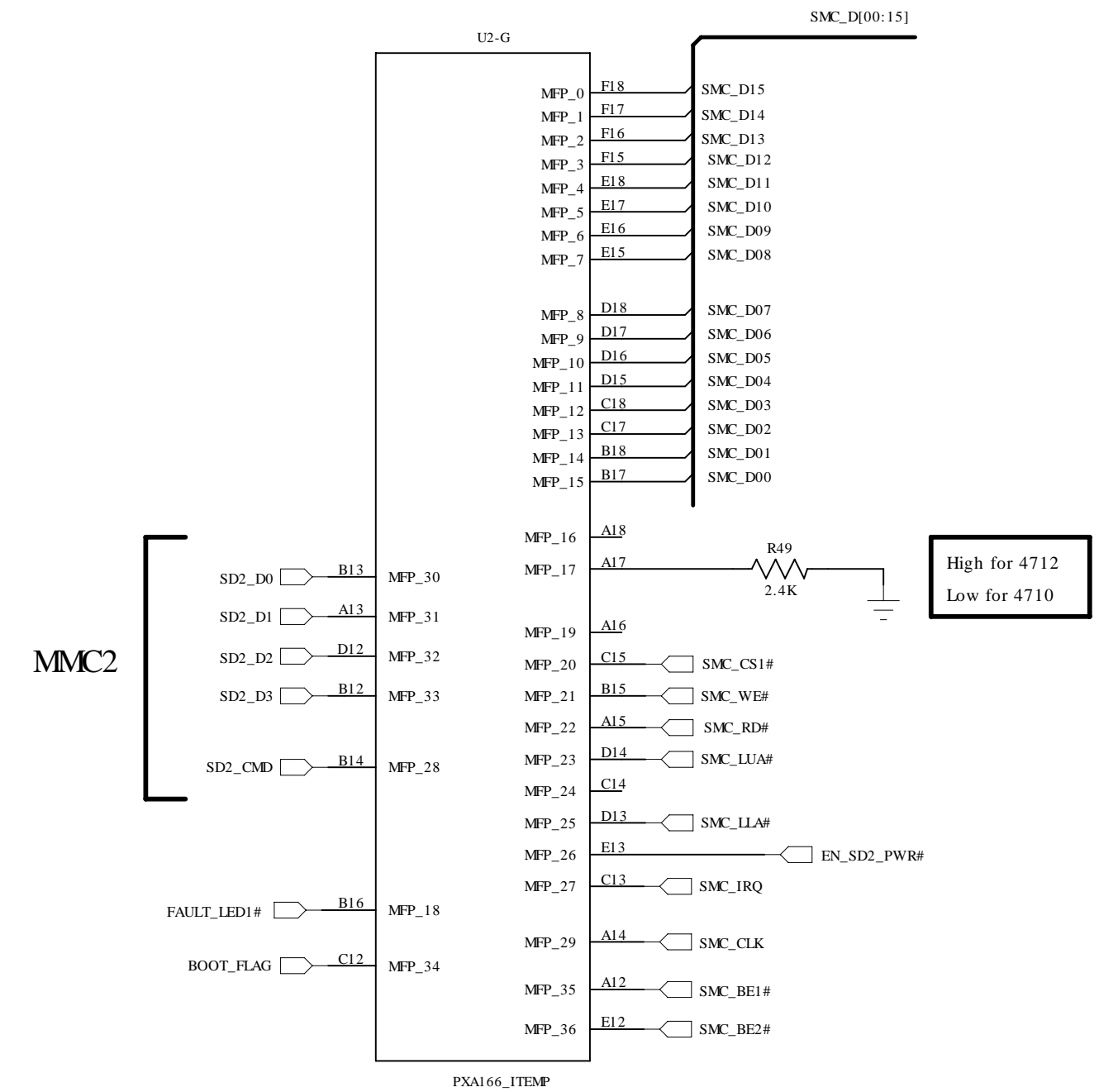
USB Ports



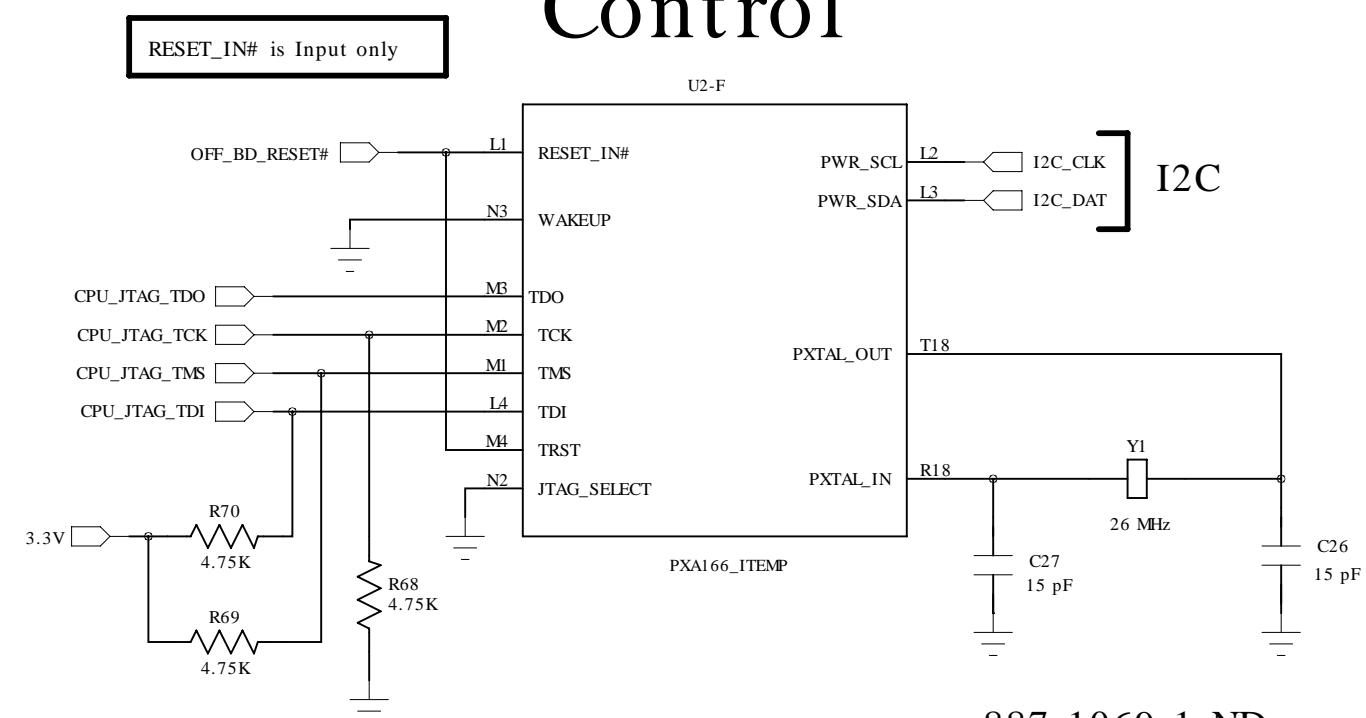
I2S



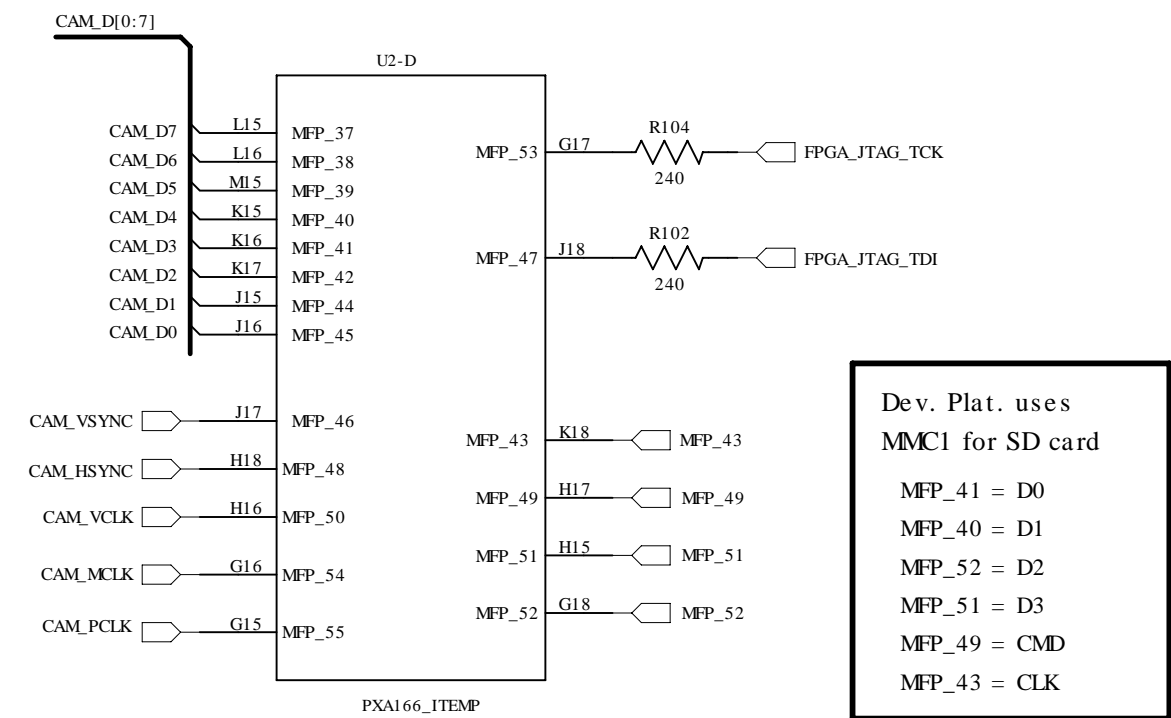
SMC Bus



Control



Camera

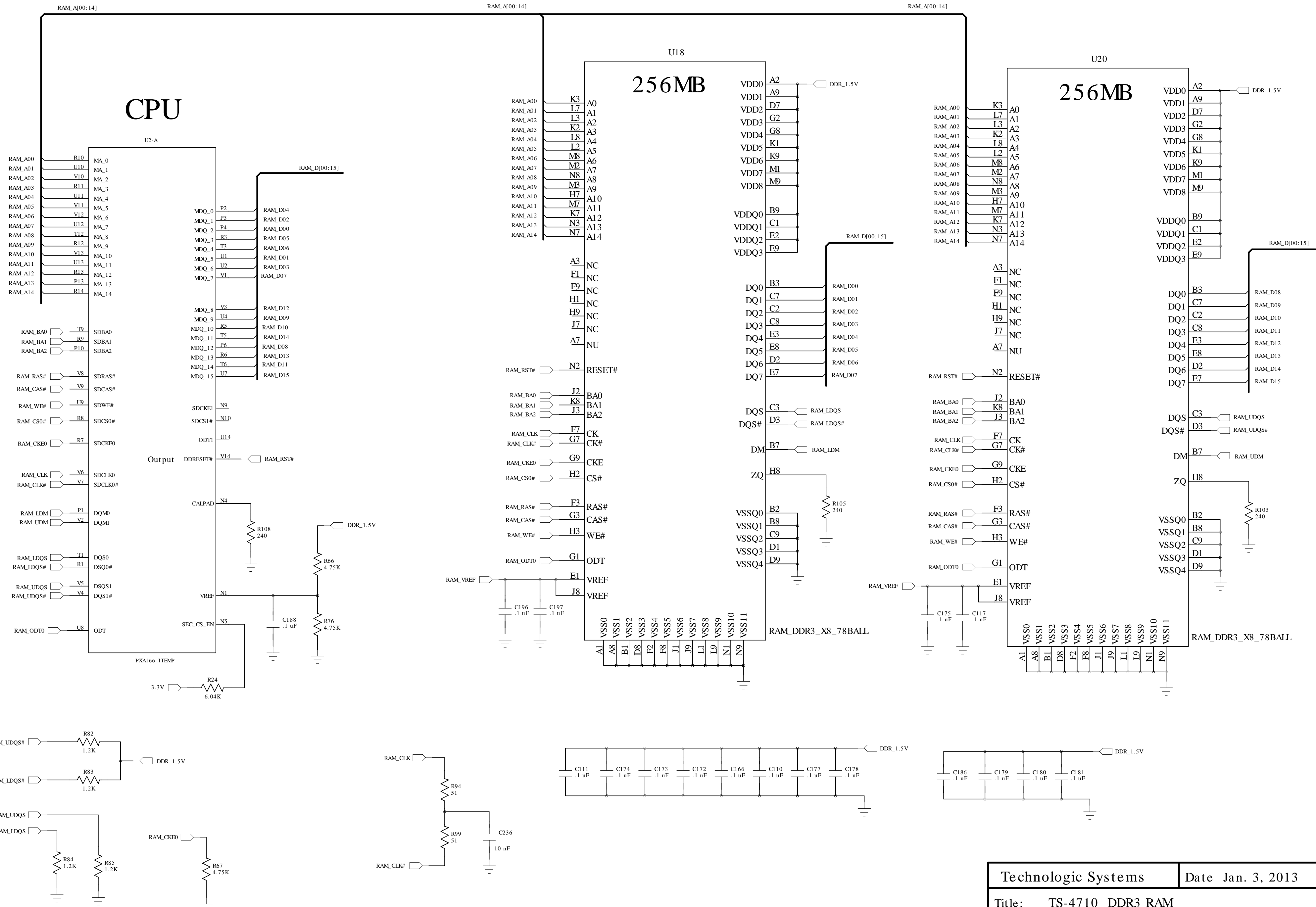


887-1069-1-ND

DDR3 x8 RAM

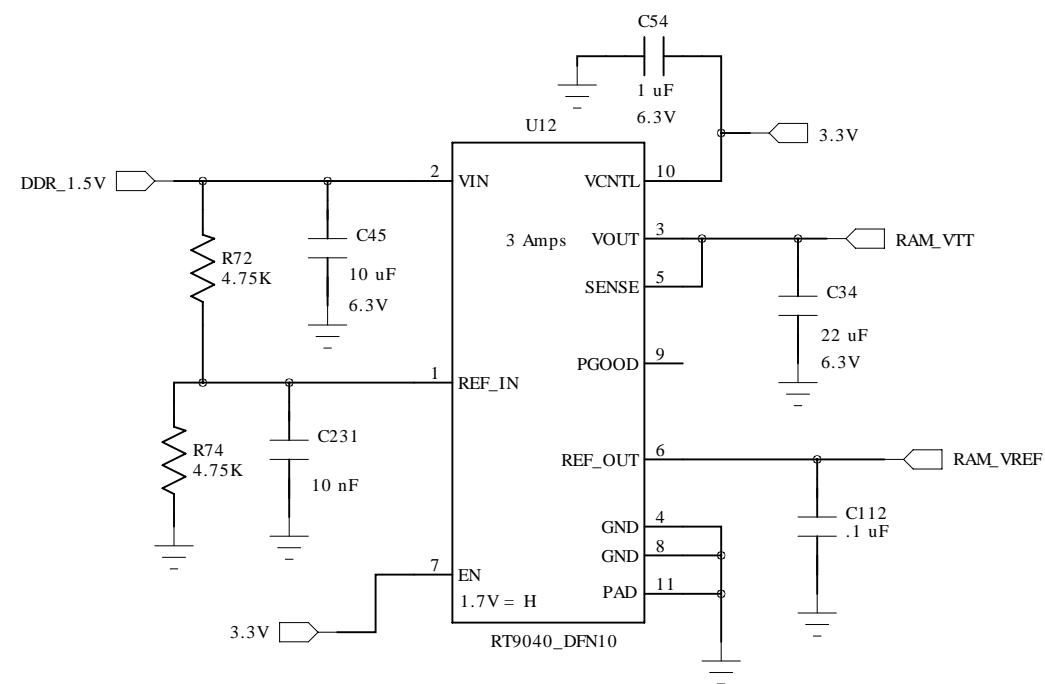
2 Gbit RAM chips

512 MB RAM Total

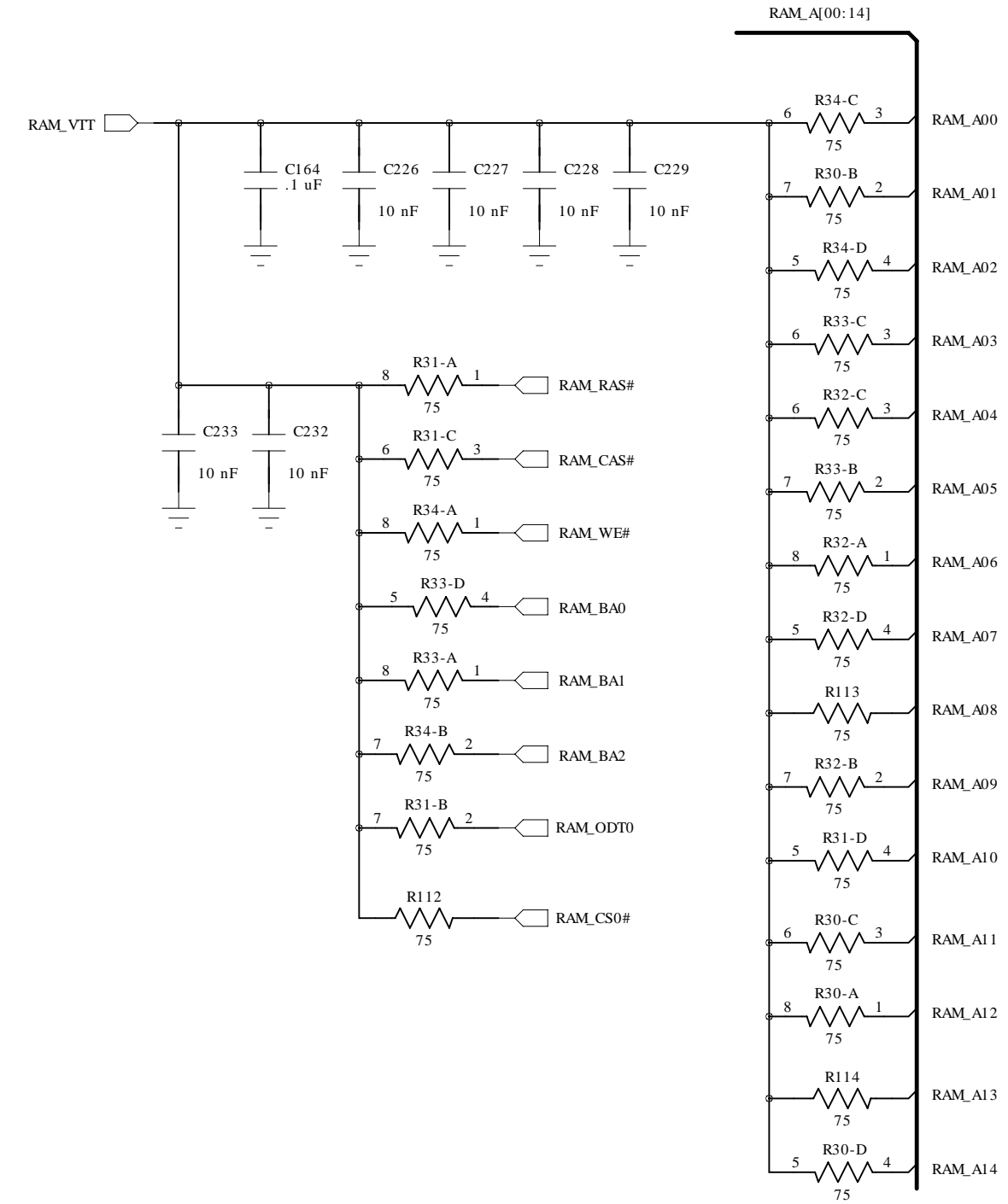


Technologic Systems	Date Jan. 3, 2013
Title: TS-4710 DDR3 RAM	
Rev: A	Designer
Sheet 2 of 10	

DDR3 RAM Termination Power Supply



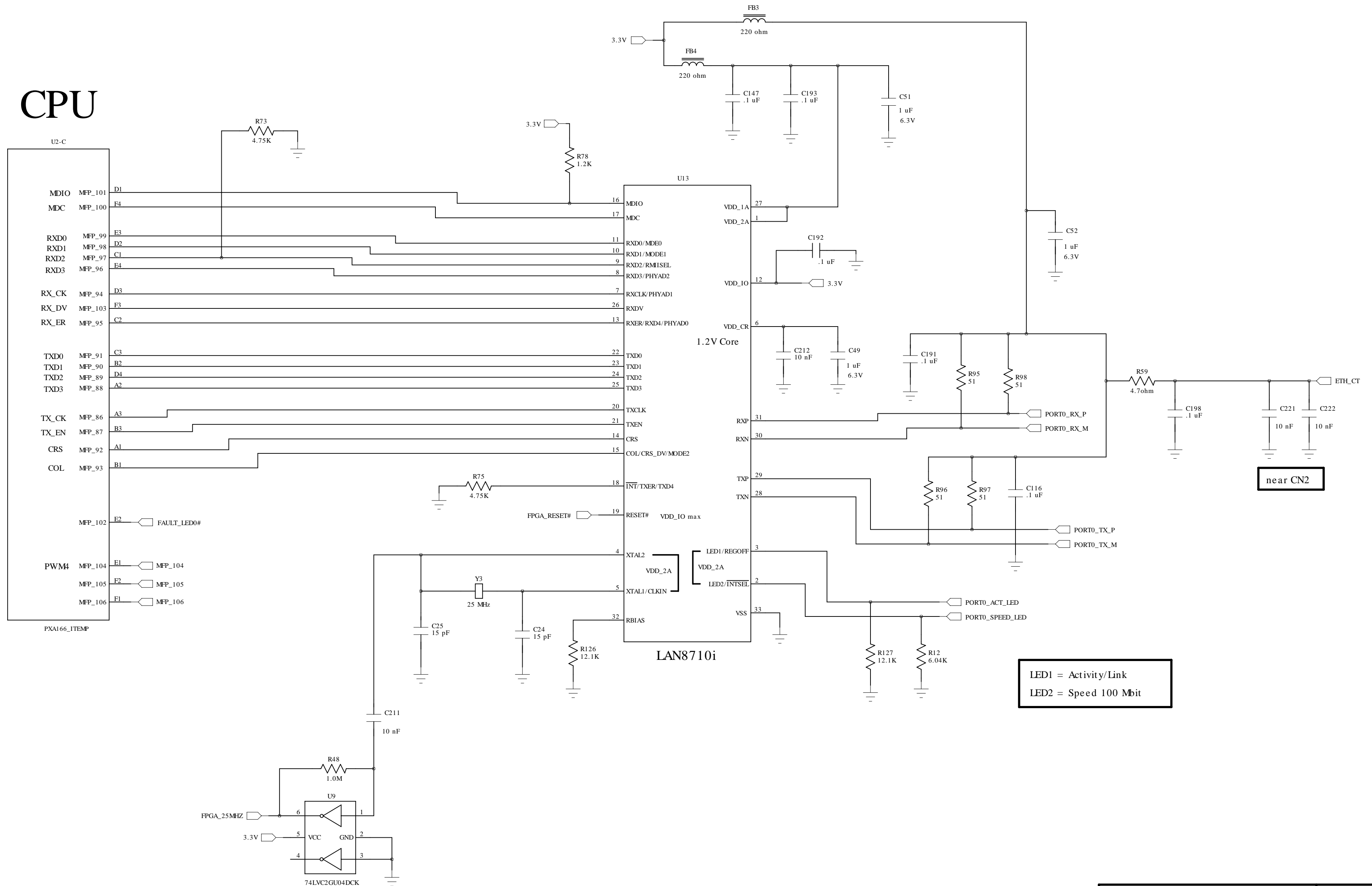
Termination Resistors



Technologic Systems	Date Jan. 3, 2013
Title: TS-4710 DDR3 RAM	
Rev: A	Designer
Sheet 3 of 10	

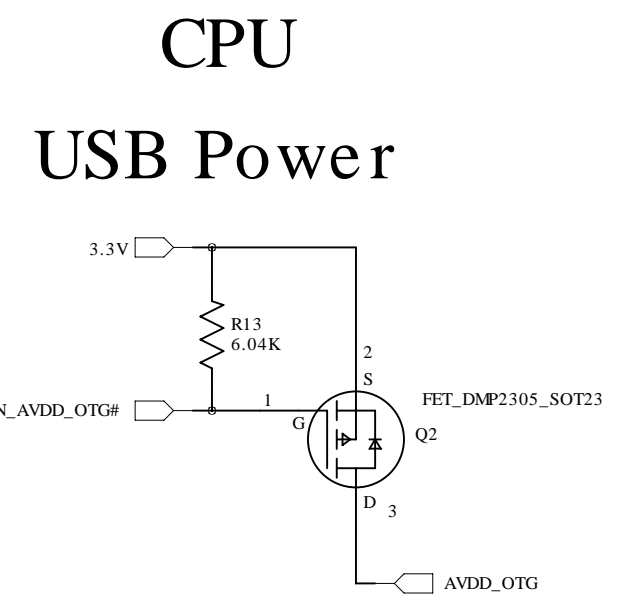
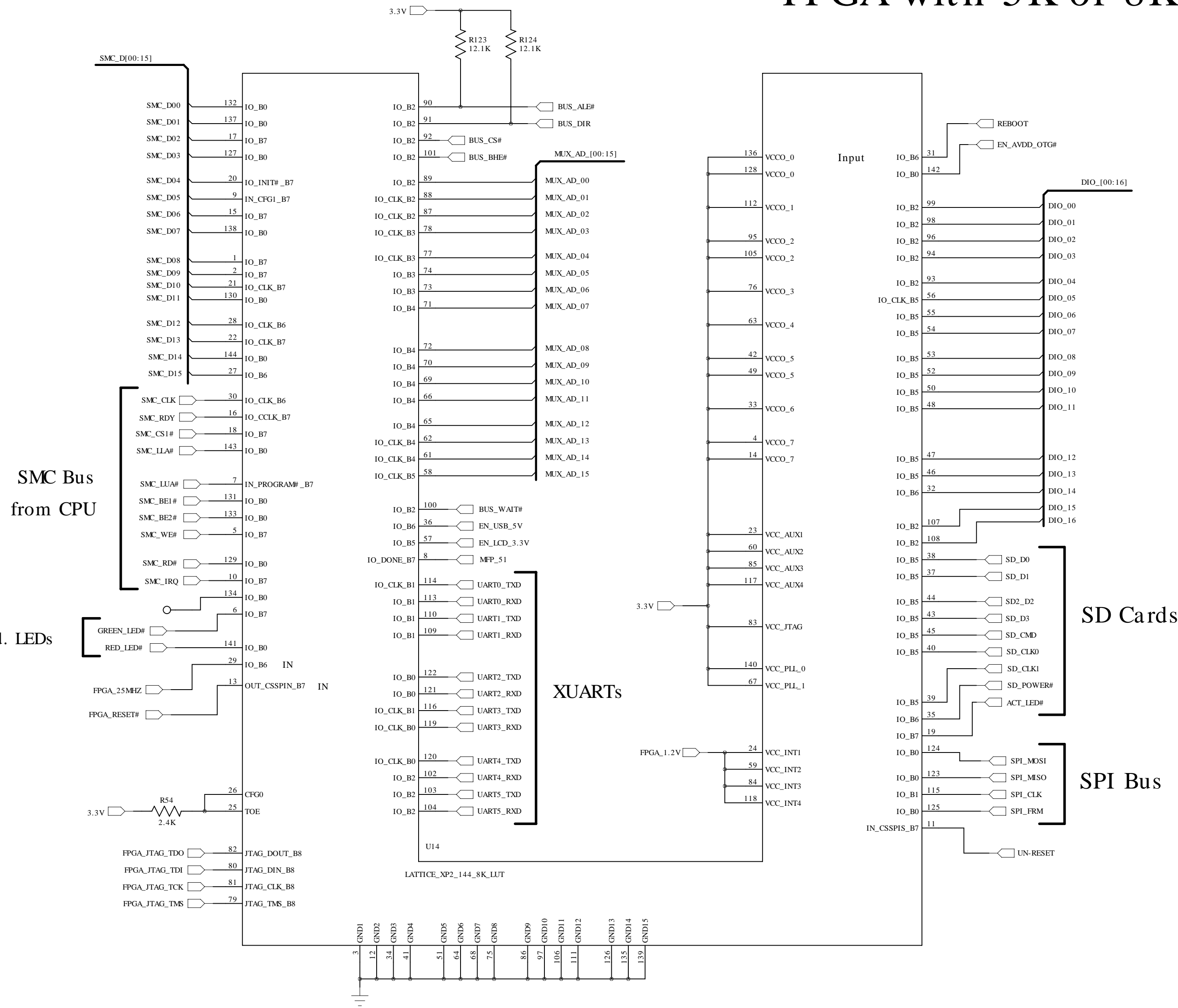
10/100 Ethernet

CPU



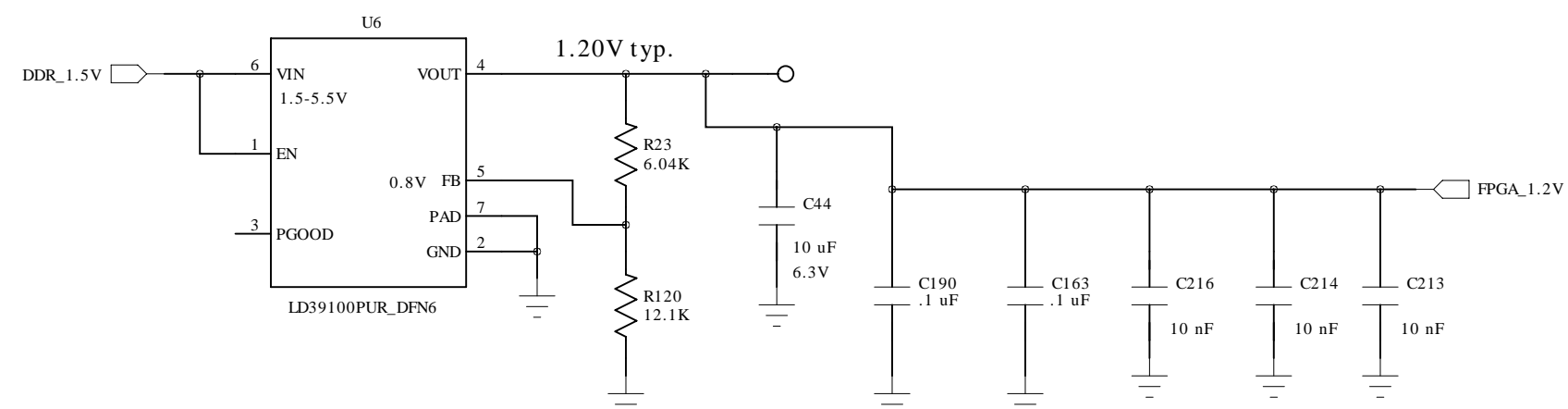
Technologic Systems		Date Jan. 3, 2013
Title: TS-4710 Ethernet		
Rev: A	Designer RLM	Sheet 4 of 10

FPGA with 5K or 8K LUTs

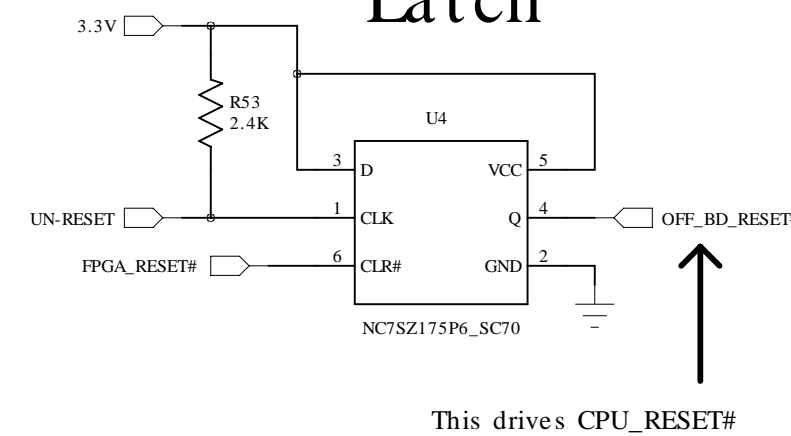


XP2-5 has:
 5K or 8K LUTS 2 PLLs
 9/12 blocks of 1Kx18 Block RAM
 12 18x18 Multipliers
 100 I/O with 144 pin package
 "instant ON" = about 1.5 mS
 input PLL clock = 10 MHz min

FPGA 1.2V Reg.

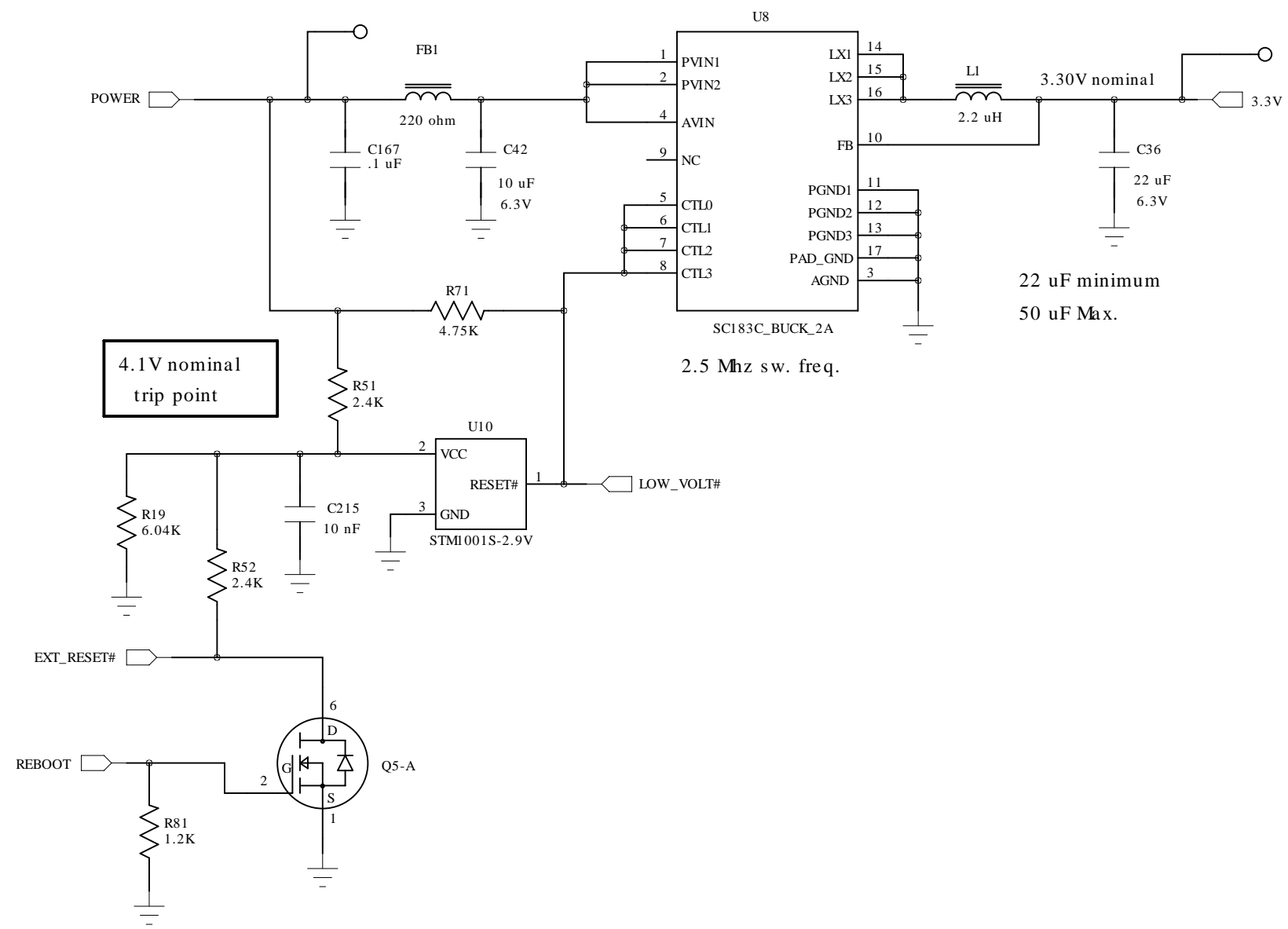


Reset Latch



1 3.3V Power Supply

up to 2000 mA



Power Supply Sequence:

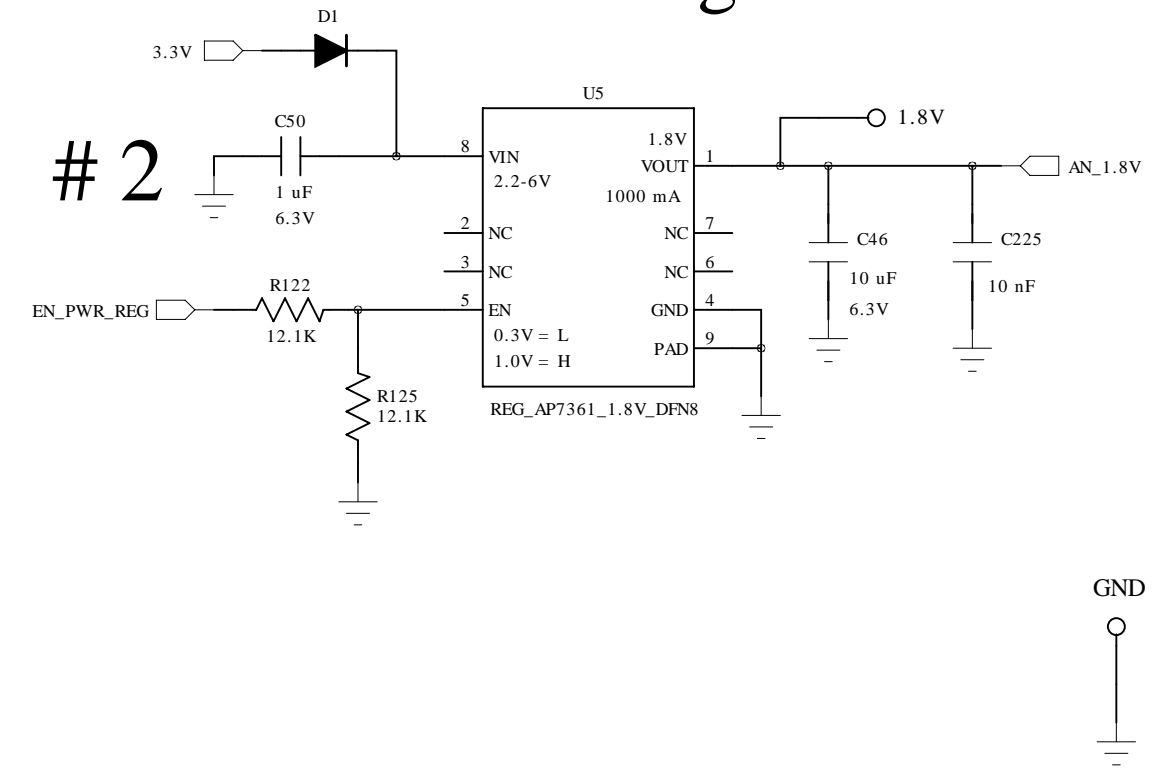
When POWER < 4.1V all rails OFF
After POWER is > 4.1V
Then wait 200 mS

- # 1 Turn on 3.3V Rail
- # 2 AVDD (1.8V) is always slightly lower than 3.3V rail
Then wait 1 mS, and enable
- # 3 CPU Core rail
Wait 4 ms then enable:
- # 4 DDR 1.5V Rail
- # 5 FPGA 1.2V ramps simultaneous with DDR_1.5V rail
- # 6 FPGA controls delay until AVDD_OTG rail is enabled

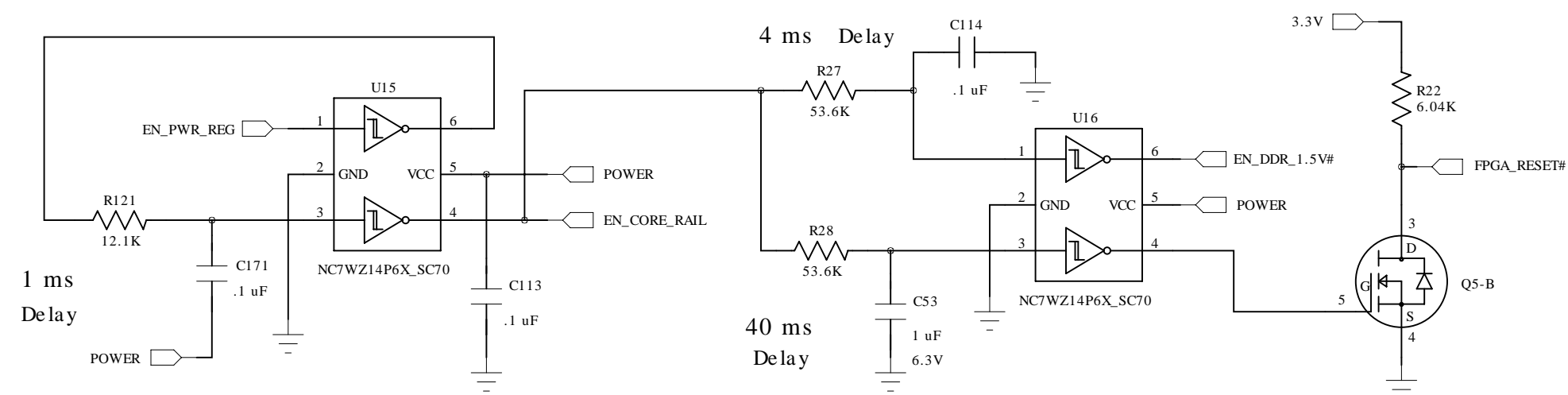
All Power rails are turned off at the same time (within 5 ms)

Power Supplies

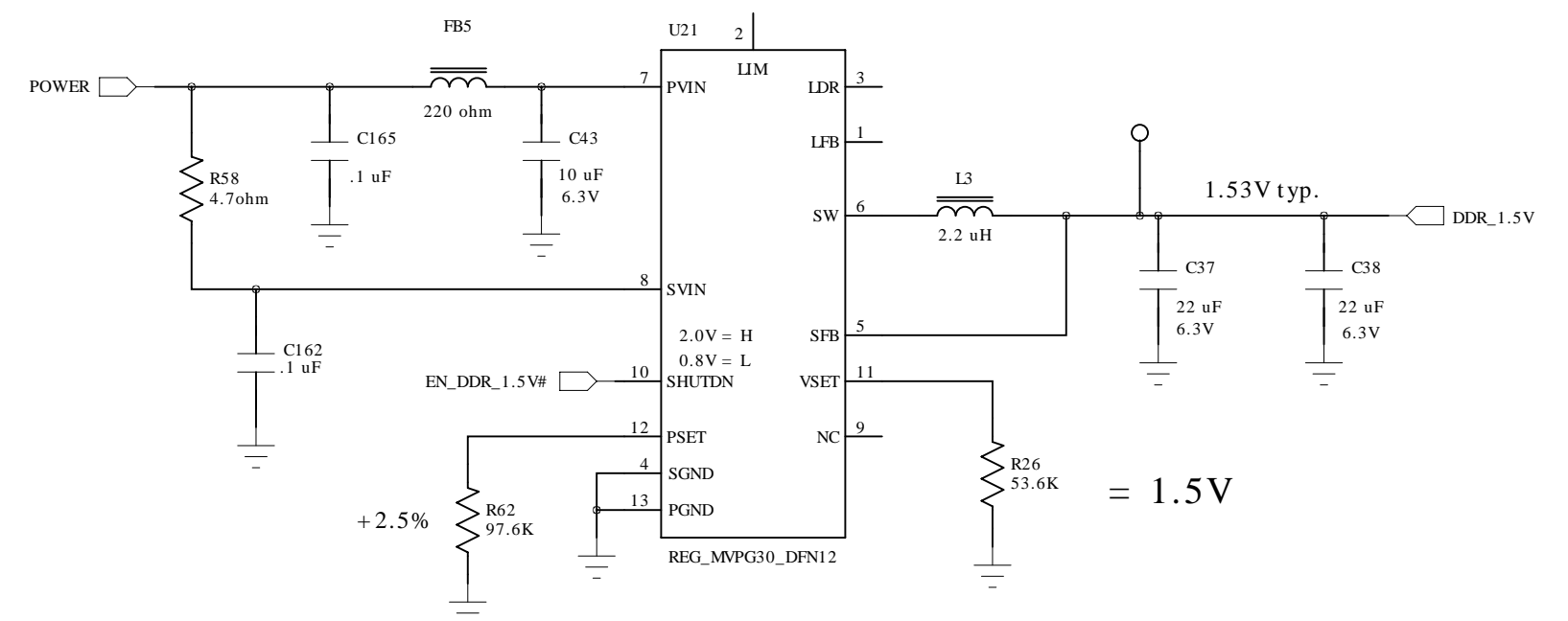
Analog 1.8V Regulator



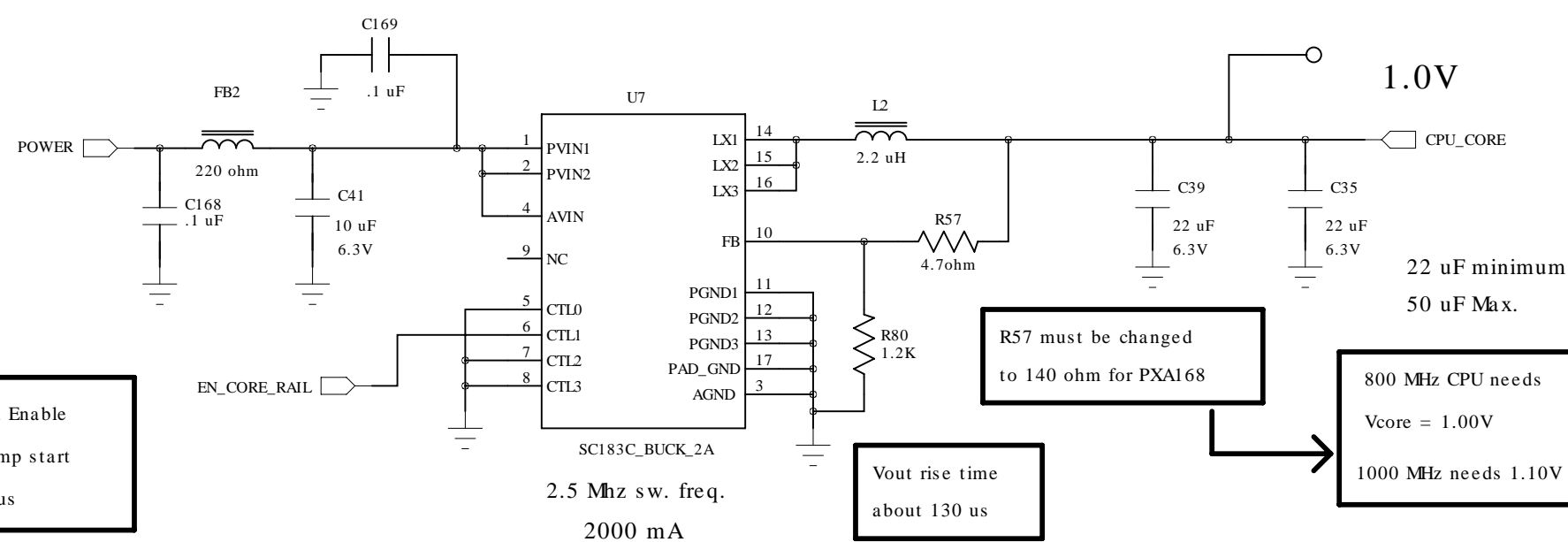
Power Sequencer



4 DDR3 1.5V Reg.



3 CPU Core Supply



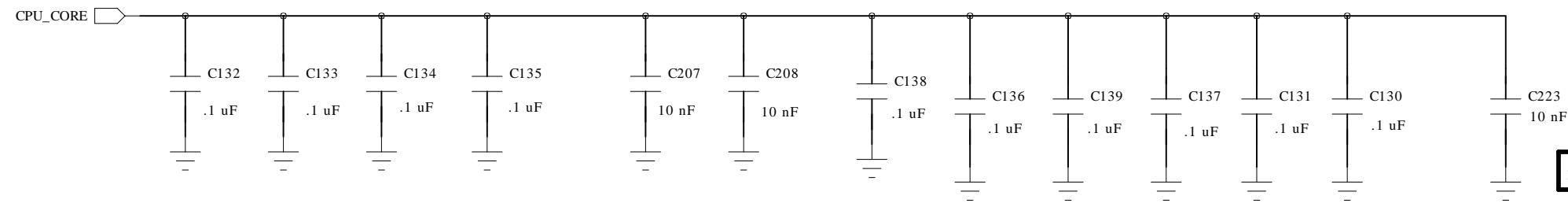
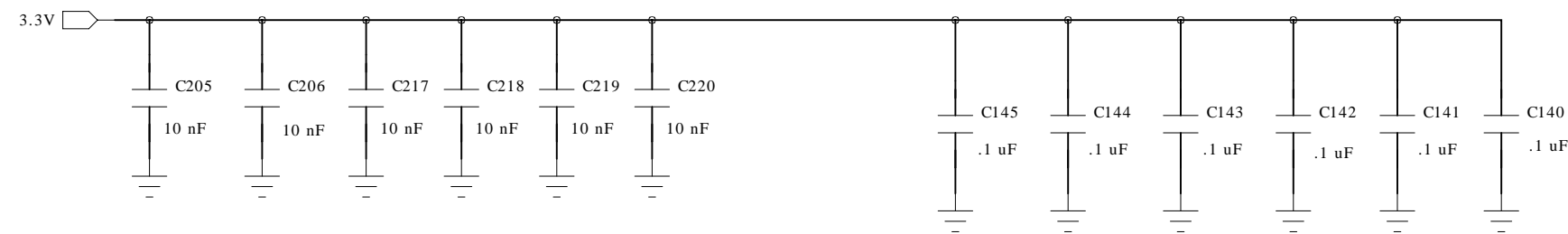
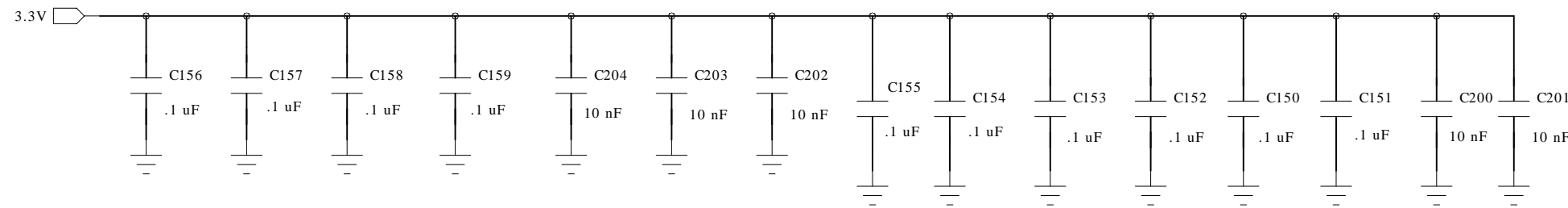
Delay from Enable to Vout ramp start is typ. 50 us

Vout rise time about 130 us

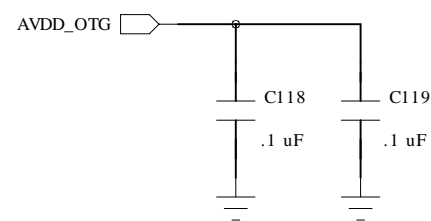
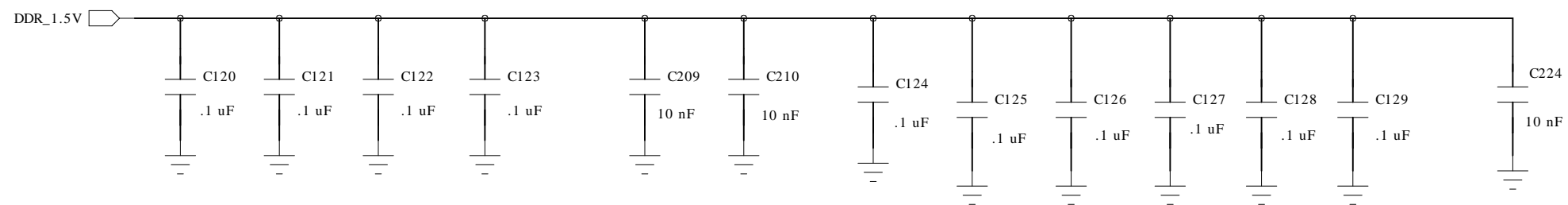
800 MHz CPU needs Vcore = 1.00V
1000 MHz needs 1.10V

Technologic Systems	Date Jan. 3, 2013
Title: TS-4710 Power Supplies	
Rev: A	Designer
Sheet 6 of 10	

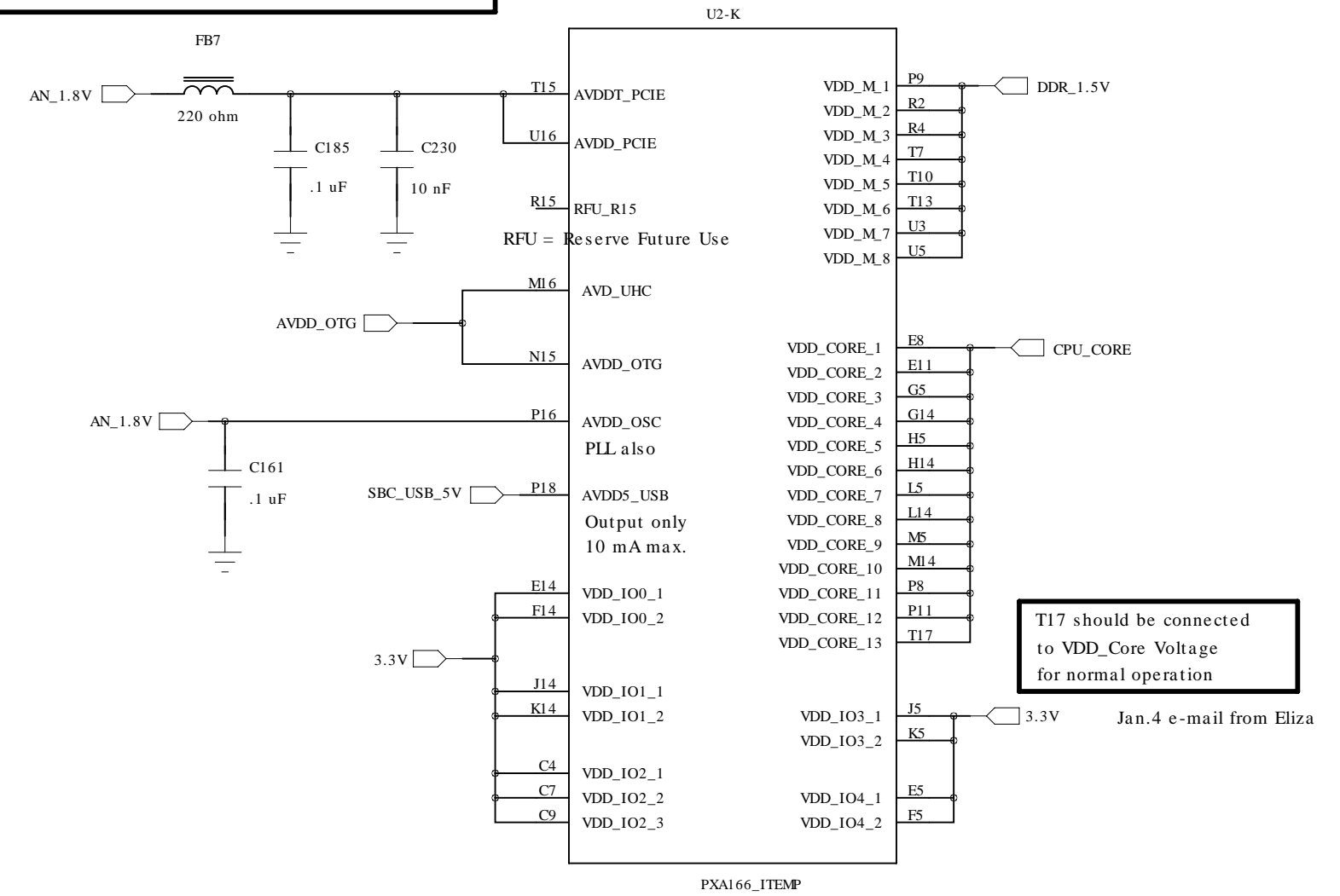
CPU Power



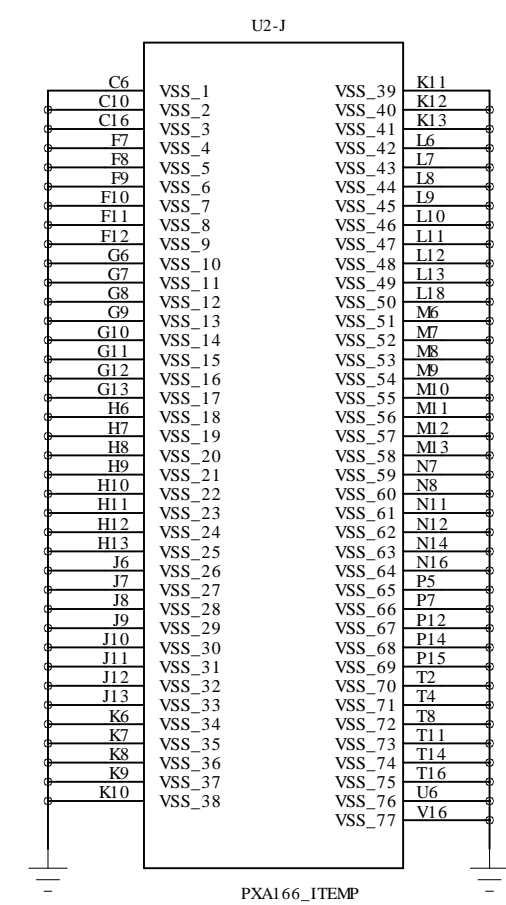
near CN2



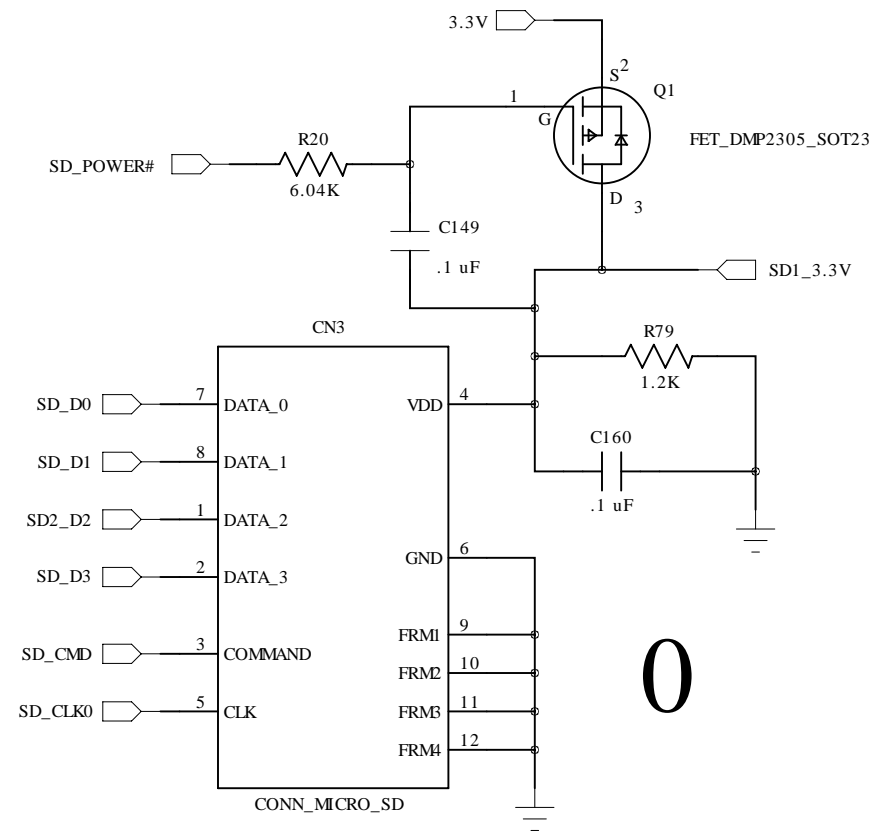
PXA168 PCIe rails must be connected to AVDD_OSC (1.8V)



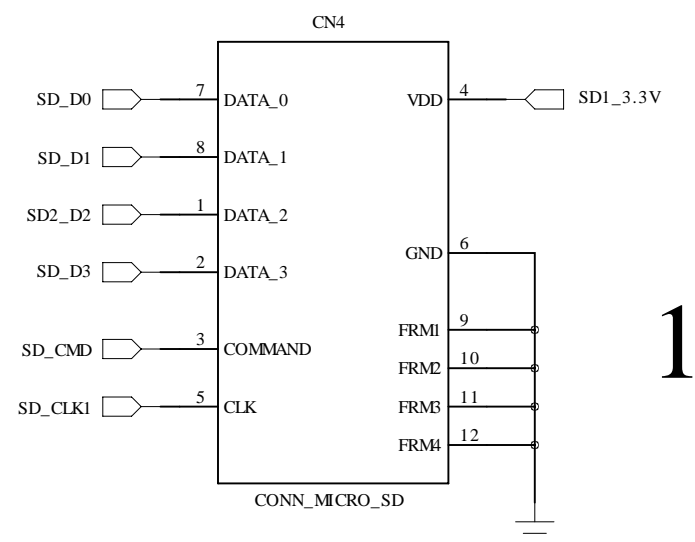
CPU



Micro SD Card Sockets

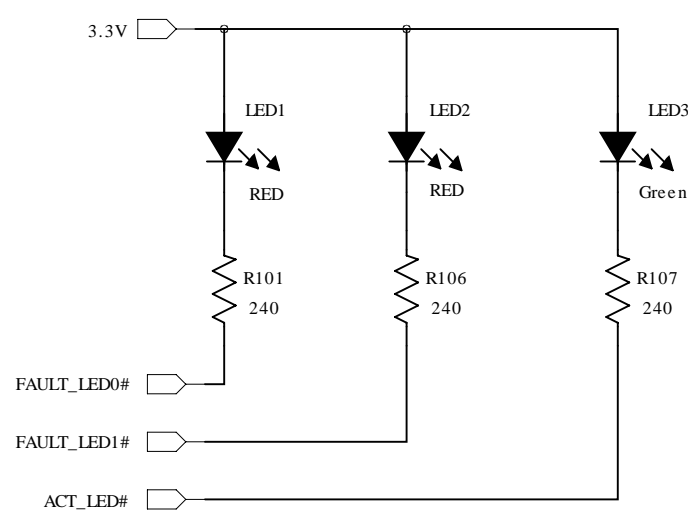


0

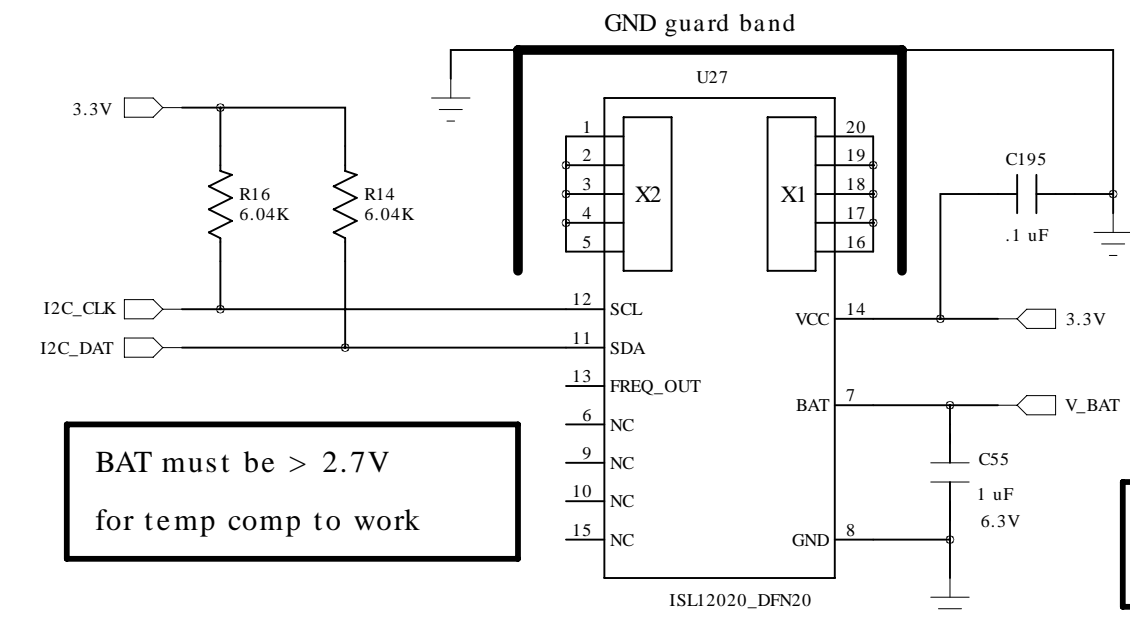


1

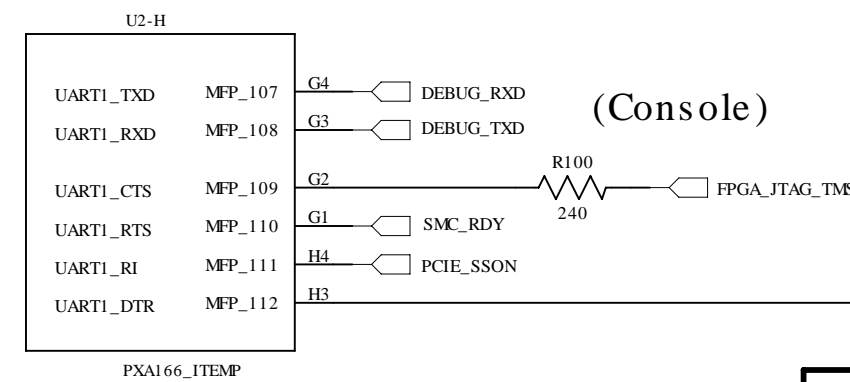
SD Card LEDs



RTC and Temp. Sensor

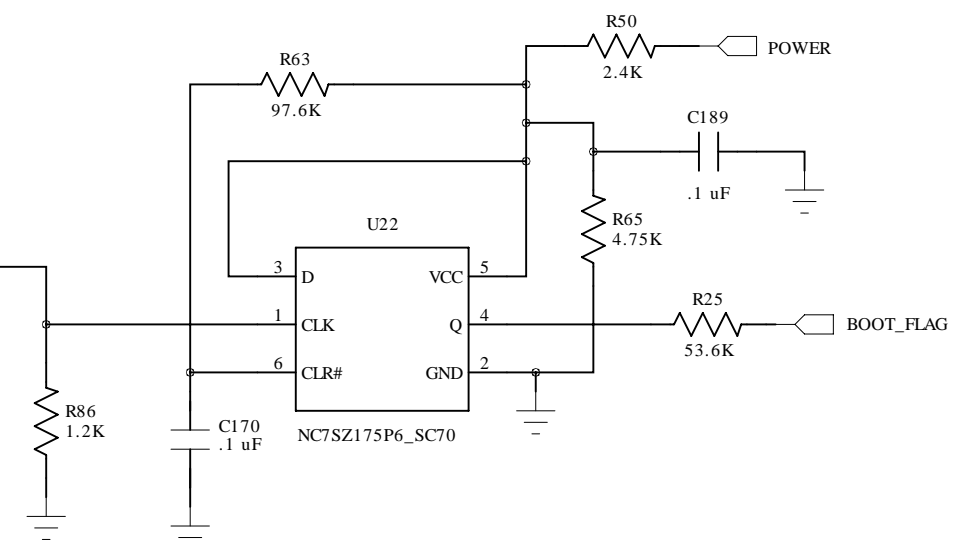


CPU Debug UART

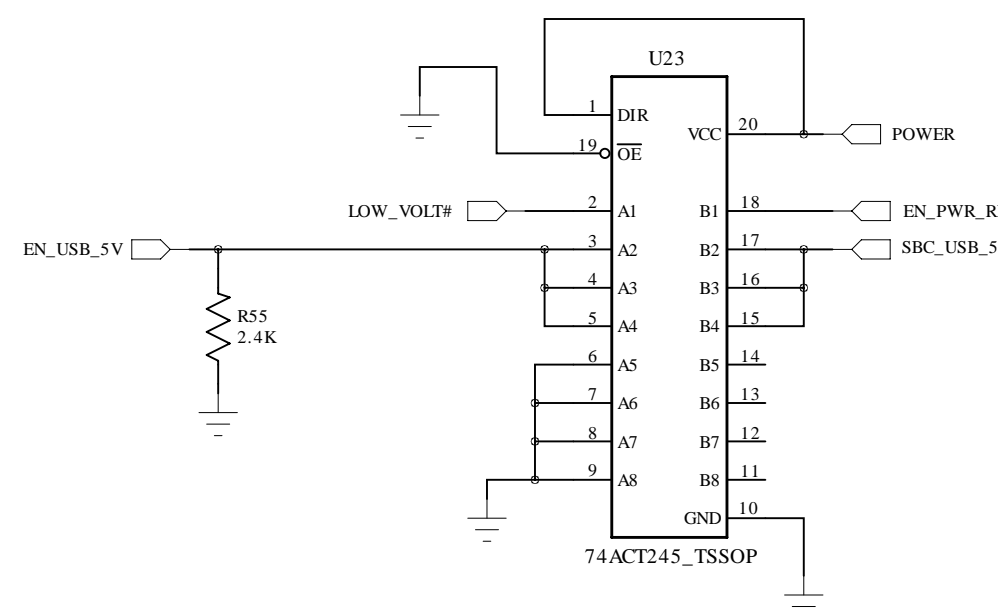


Keep normally at logic zero

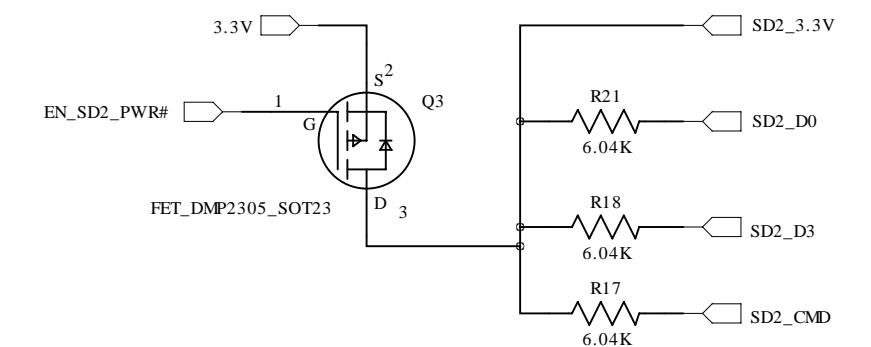
Reboot Flag



3.3V --> 5V Level Shifter

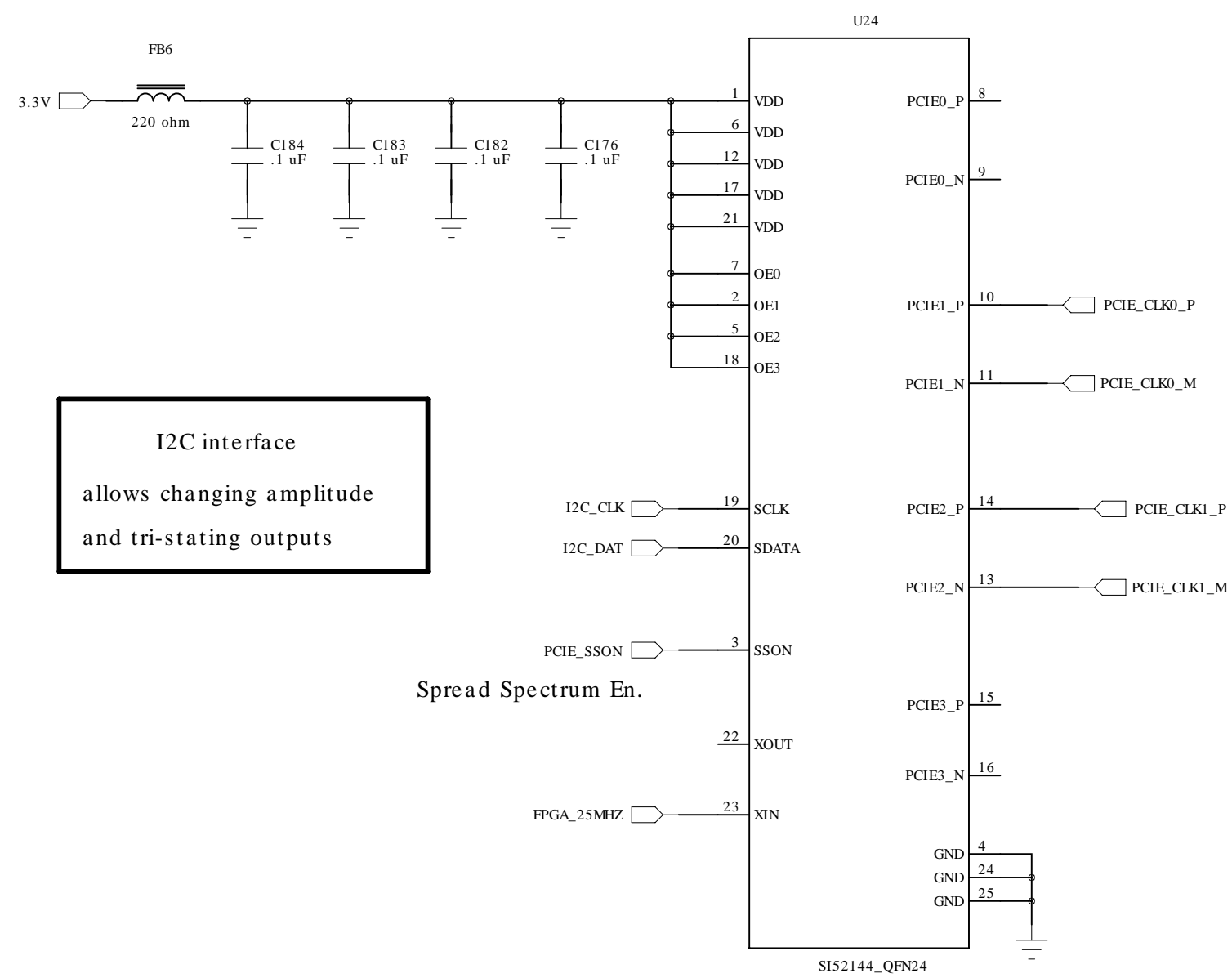


OFF BD. SD Card Power



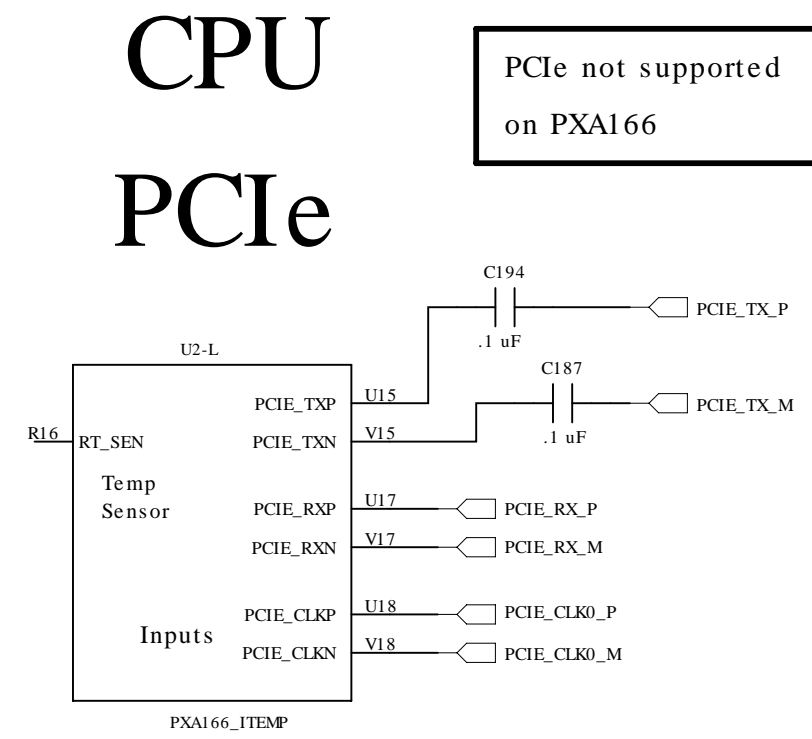
Technologic Systems	Date Jan. 3, 2013
Title: TS-4710 SD card, RTC, Temp.	
Rev: A	Designer
Sheet 8 of 10	

PCIe 100 MHz Clock Generator



I2C interface
allows changing amplitude
and tri-stating outputs

Spread Spectrum En.



Two 100-pin Off-board Connectors

"POWER" pins supply all power to the module
Apply 4.5V to 5.5V to these pins

Current drain is approximately 400 mA

EXT_RESET# is an Input
used to reboot the CPU

Do not drive active high
(use open drain)

⚠ All signals driving DIO on CN1 & CN2 must be powered by the 3.3V on CN2, or remain at 0V until the CN2 3.3V rail is > 3.0V

⚠ Pin 1 is the top left corner pin on the connector. All of the pins on the left are odd numbered. This may differ from the connector manufacturer's datasheet.

OFF_BD_RESET# is an Output
used to reset all peripherals

Must have 10 nF Capacitor
very near CN2 and GND
for all "quiet" signals
(between diff pairs)

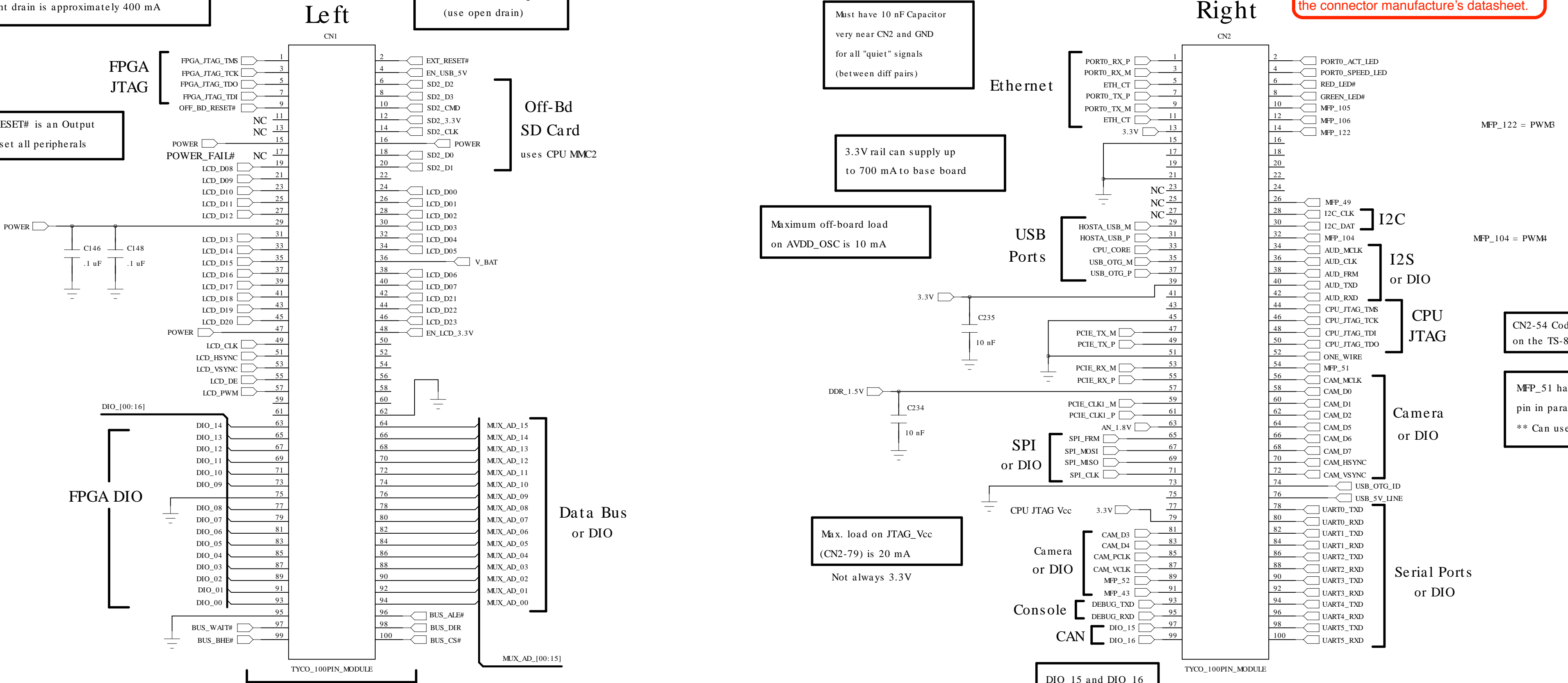
3.3V rail can supply up
to 700 mA to base board

Maximum off-board load
on AVDD_OSC is 10 mA

Max. load on JTAG_Vcc
(CN2-79) is 20 mA
Not always 3.3V

CN2-54 Codec CLK
on the TS-8390

MFP_51 has FPGA
pin in parallel
** Can use either



FPGA DIO

Data Bus
or DIO

Bus Control

If Bus is not needed, all Bus
signals can be changed to DIO

⚠ Any I/O routed to a user accessible
connector should have additional ESD
protection placed on the carrier board.

Devices connected to this bus must never
drive it when BUS_CS# is deasserted
(must be off within 30 nS of deassertion)

Devices must pull the BUS_WAIT# line low
if they need more than 150 nS strobe

The data bus can not have more than
30 pF of off-board capacitive loading
May need data buffer chip for heavy loads