PXA166 800 MHz - PXA168 1066 MHz

USB Ports

Board ID

SMC Bus

LCD

I2S

Control

Camera

USB Ports

Board ID

SMC Bus

LCD

I2S

Control

Camera
10/100 Ethernet 4-Port Switch

Defaults to MI PHY mode with 3.3V Levels

Auto MDIX is supported
Polarity Correction also supported

CPU
MAC

Ethernet MII

Defaults to MI PHY mode with 3.3V Levels

Auto MDIX is supported
Polarity Correction also supported

All Port 6 pins have PU or PD bias

Power up with no config

MAC

PWM 4

M II PHY

1.2V

10/100 Ethernet 4-Port Switch

CPU
MAC

Ethernet MII

Defaults to MI PHY mode with 3.3V Levels

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MAC

PWM 4

M II PHY

1.2V
# 1 3.3V Power Supply

- 3.3V Power Supply up to 2000 mA
- 2.5 MHz sw. freq.
- 22 uF minimum
- 50 uF max.

# 2 1.8V Regulator

- 1.8V Regulator
- 4.1V nominal
- 1.8V regulators

# 3 CPU Core Supply

- 1.0V or 1.12V
- 3.30V nominal
- 1.0V or 1.12V

# 4 DDR3 1.5V Reg.

- DDR3 1.5V Reg.
- 1000 MHz needs 1.12V
- 800 MHz needs 1.0V

---

**Title:** TS-4712 Power Supplies

**Date:** Jan. 2, 2013

**Rev:** A

**Designer:**

**Sheet:** 6 of 10
CPU Power

PXA168 PCIe rails must be connected to AN_1.8V

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PCIe 100 MHz
Clock Generator

PXA166 and PXA168 BOM Differences

R57 = 140 ohm for PXA168
R56 removed for PXA168
FB6, FB7 removed for PXA166
U24 removed for PXA166
U2 = PXA166 Commercial Temp
or = PXA168 Industrial Temp

PCIe not supported on PXA166
**Two 100-pin Off-board Connectors**

- **POWER** pins supply all power to the module.
  - Apply 4.5V to 5.5V to these pins.
  - Current drain is approximately 400 mA.

- OFF_BD_RESET# is an Output used to reset all peripherals.
  - Must have 10K ohm Capacitor very near CN2 and GND for all 'open' signals.

- EXT_RESET# is an Input used to reboot the CPU.
  - Do not drive active high (use open drain).

- Apply 4.5V to 5.5V to these pins.

- "POWER" pins supply power to the module.

- FPGA DIO

- SATA, USB, I2C, Camera

- Off-Bd SD Card
  - Connects to CPU MMC2

- Off-Bd JTAG

- Data Bus or DIO

- Left
  - BUS_BHE#
  - BUS_WAIT#
  - BUS_CS#
  - BUS_DIR
  - BUS_CI0 to BUS_CI31

- Right
  - BUS_CI0 to BUS_CI31
  - BUS_CI0

- Primary Ethernet
  - USB Ports
  - USB
  - 100-pin Off-board Connectors

- 3.3V can supply up to 700 mA to base board.

- Maximum off-board load on AN_1.8V is 10 mA.

- Minimum load on JTAG_Vcc (CN2-79) is 20 mA.
  - Not always 3.3V.

- Devices connected to this bus must never
  - Drive it when BUS_CSM is deasserted
  - (must be off within 30 nS of deassertion).

- Devices must pull the BUS_WA/PW low if
  - They need more than 150 nS strobe.

- The data bus cannot have more than
  - 30 pF of off-board capacitive loading.
  - May need data buffer chip for heavy loads.

---

**Notes**

- **Technologic Systems**
- **Date**: Jan. 2, 2013

**Title**: TS-4712 Off-board Connectors

**Rev**: A  **Designer**  **Sheet**: 10 of 10