10/100 Ethernet 4-Port Switch

CPU

MAC

Ethernet MII

Defaults to MI PHY mode with 3.3V Levels

All Port 6 pins have PU or PD bias

Pull-downs default P6 to port disabled mode

Auto MDIX is supported

Polarity Correction also supported

Requires Reset# asserted for 10 ms after power

Title: TS-4720 Ethernet Switch

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# 1 3.3V Power Supply

# 2 1.8V Regulator

# 3 CPU Core Supply

# 4 DDR3 1.5V Reg.
CPU Power

PXAl68 PCIe rails must be connected to AN_1.8V

CPU

CPU

PXA168 PCIE rails must be connected to AN_1.8V
PCIe 100 MHz
Clock Generator

CPU

Reboot Flag

PXA166 and PXA168 BOM Differences

R57 = 140 ohm for PXA168
R56 removed for PXA166
FB6, FB7 removed for PXA166
U2 = PXA166 Commercial Temp
or = PXA168 Industrial Temp
Two 100-pin Off-board Connectors

- **POWER** pins supply all power to the module. Apply 4.5V to 5.5V to these pins.
  - Current drain is approximately 600 mA.

- OFF_BD_RESET# is an Output used to reset all peripherals.
  - Must have 10 pf Capacitor very near CN2 and GND for all ‘open’ signals.

- FPGA_JTAG_TM is an Input used to reboot the CPU.
  - Do not drive active high (see open drain).

- FPGA_JTAG_TDI is an Input.

- BUS_WAIT# is an Input used to drive it when BUS_CS# is deasserted.

- BUS_BHE# is an Input used to drive it when BUS_CS# is deasserted.

- Devices connected to this bus must never drive it when BUS_CS# is deasserted.
  - (must be off within 30 ns of deassertion).

- Devices must pull the BUS_S/A# pin low if they need more than 150 ns strobe.

- The data bus cannot have more than 30 pf of off-board capacitive loading.
  - May need data buffer chip for heavy loads.

- Two 100-pin Off-board Connectors

- Bus Control
  - Off-Bd SD Card
    - FPGA DIO
    - FPGA JTAG
  - Data Bus or DIO
    - Bus Control
  - Left
    - Off-Bd SD Card
      - FPGA DIO
      - FPGA JTAG
    - Data Bus or DIO
  - Right
    - Primary Ethernet
    - USB Ports
    - I2C
    - I2S or DIO
    - Camera or DIO
    - Serial Ports or DIO

- Maximum off-board load on AN_1.8V is 10 mA.
  - Minimum off-board load on AN_1.8V is 10 mA.

- Must have 10 pf Capacitor very near CN2 and GND for all ‘open’ signals.
  - (between off pins).

- Maximum off-board load on JTAG_Vcc is 20 mA.
  - Maximum load on JTAG_Vcc is 20 mA.

- Not always 3.3V.

- May need data buffer chip for heavy loads.

- Two 100-pin Off-board Connectors

- Technologic Systems
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  - Title: TS-4720 Off-board Connectors
  - Rev: A
  - Designer
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