LAN8710 can power sequence in any order

10/100 Ethernet Port

CPU

MAC

PHY address = 0

LED high voltage = VDD_2A = 3.3V

PHY address and modes latched on rising edge of Reset#

For MX315 in MII mode before deasserting Reset#

1.2V Core

Internal 1.2V Reg can be turned off by keeping LED high

Using Sw 1.2V Reg saves 13 mA @ 5V
Total chip power 140mA = 100 mw

Must have no aggressor signals near 12.1K resistor

Try short as possible

In 1.2mA

12.1K

6.3V

CPU

4

10/100 Ethernet PHY

LAN8710i

10/100 Ethernet Port

CPU

MAC

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LED high voltage = VDD_2A = 3.3V

PHY address and modes latched on rising edge of Reset#

For MX315 in MII mode before deasserting Reset#

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CPU

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10/100 Ethernet PHY

LAN8710i

10/100 Ethernet Port

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Try short as possible

In 1.2mA

6.3V
Interface to CPU

Power up

CPU reload bit stream

Bit stream should initialize
EN_AVDD_OTG# deasserted (high)
After FPGA_RESET# deasserted, it should assert
EN_AVDD_OTG#
Then wait 10 ms, and write a "1" into the CPU RESET Latch

FPGA_RESET# will still be asserted
after FPGA is configured
and can be used as a FPGA reset

CPU can also drive FPGA_RESET#
low during a "soft" FPGA update

This will clear Boot Flag

“Warm Reboot” occurs
by clearing Reset Latch
This will reload the FPGA

This will not clear Boot Flag

25K equivalent LUTs
(15K 6-input LUTs)
177 DIO
30K Flip-flops
52 [2K x 9] Block RAM
2 PLLs + 4 DCMs
38 18x18 Multipliers

Each MUlt. has an adder and accumulator

TeChnologic Systems
Date June 11, 2013
Title: TS-4740 Xilinx FPGA
Rev: A  Designer  Sheet 5 of 13
Xilinx LX25T_324 FPGA

Gigabit Transceivers

FPGA_INIT# can be used to delay configuration
Also indicates load error

Power and Special Functions

10_swapen_0 controls DIO during configuration. Low = PU enabled
High = All DIO are floating

FPGA Reload

Page 162 GTP User Guide

Page 168-169

RF_CLK inputs have internal 100 ohm term.
must be cap coupled

Page 168-169

8MB SPI Flash

64 bytes of GTP
FPGA Core 1.2V

Internal 3 ms delay

CPU
Debug UART
(Except)
Reboot Flag

Keep normally at logic zero
CPU Power

PXA168 PCIe rails must be connected to AN_1.8V

CPU

T17 should be connected to VDD_Core Voltage for normal operation

Jan 4 email from Eliza near CN2

TS-4740 CPU Power and Bypass caps
Micro SD Card Socket

RTC and Temp. Sensor

Temp must be > 2.7V for temp comp to work

eMMC 4GB

SD Card LEDs

BAT must be > 2.7V for temp comp to work

Temp takes 68 uA for 22 ms, once every minute
PCIe 100 MHz Clock Generator

I2C interface allows changing amplitude and tri-state outputs

Phase does not matter

EEPROM 1 Kbyte

I2C address is same as RTC!
Two 100-pin Off-board Connectors

**POWER** pins supply all power to the module
Apply 4.5V to 5.5V to these pins
Current drain is approximately 600 mA

EXT_RESET# is an Input
used to reset the CPU
Do not drive active high
(except open drain)

OFF_BD_RESET# is an Output
used to reset all peripherals

** Must have off-capacitor very near CN2 and GND
for all "quiet" signals
(between diff pairs)

FPGA_JTAG_TDI
FPGA_JTAG_TDO
FPGA_JTAG_TCK

Bus Control

If Bus is not needed, all Bus signals can be changed to DIO

Devices connected to this bus must never drive it when BUS.Command is deasserted
(must be off within 50 nS of deassertion)

Device must pull the BUS_Reset pin low
if they need more than 150 uA strobe

FPGA DIO

DIO_00
DIO_01
DIO_02
DIO_03
DIO_04
DIO_05
DIO_07
DIO_08
DIO_13
DIO_14

Data Bus or DIO

FPGA

DIO_15
DIO_16

V_BAT

USB Ports

USB_5V_LINE

Gigabit Ethernet

MFP_104 or PWM

Camera or DIO

CAM_M_CLK
CAM_P_CLK
CAM_D0
CAM_D1
CAM_D2
CAM_D3
CAM_HS
CAM_V

SPI or DIO

I2C

I2S

Camera

Console

Serial Ports or DIO

EXT_RESET#

CPU_JTAG_VCC

AUD_TXD
AUD_FRM
AUD_CLK
AUD_M_CLK

CPU_JTAG_VCC

UART3_TXD
UART2_TXD
UART1_RXD
UART0_RXD

CPU_JTAG_VCC

UART5_RXD
UART5_TXD
UART4_RXD
UART4_TXD

CPU_JTAG_VCC

FE_CT
FE_RX_P
FE_RX_M
FE_TX_M

CPU_JTAG_VCC

CPU_JTAG_VCC

GIG_SPEED_LED
GIG_ACT_LED

MFP_104 = PWM 4

MFP_121 = PWM 0

** Cannot use either

** Can use either

Title: TS-4740 Off-board Connectors
Rev: A  Designer  Sheet 13 of 13

Technologic Systems  Date: June 11, 2013