DDR3 RAM
Termination
Power Supply

Termination
Resistors

Technologic Systems
Title: TS-4740 DDR3
Date June 11, 2013
Rev: A
Designer
Sheet 3 of 13
10/100 Ethernet Port

CPU

MAC

LAN8710i

Must have no aggressor signals near 12.1K resistor.
Keep short as possible.

PHY address = 0

PHY address and modes latched
on rising edge of Reset#.

LAN8710i can power
sequence in any order

LED1 = Activity/Link

LED2 = Speed 100 Mbit

PHY address = 0

MDIO bus can not be
used until 100 uS after
Reset# is deasserted.

MXCLK max is 2.5 MHz

MDC

MDIO

PHY max is 2.5 MHz

Initial 1.2V Reg

can be turned off
by keeping LED high.

Use 1.2V Reg.

set at 13 mA @ 3.3V

Total chip power:
140mW ~ 100 mW

LPC8710i

CPU

TX_EN

TX_CK

TXD3

TXD2

TXD1

TXD0

RX_CK

RXD3

RXD2

RX_DV

RXD1

RXD0

RX_ER

PHY address = 0

PHY address and modes latched
on rising edge of Reset#.

LAN8710i can power
sequence in any order

LED1 = Activity/Link

LED2 = Speed 100 Mbit

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LAN8710i can power
sequence in any order

LED1 = Activity/Link

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PHY address = 0

PHY address and modes latched
on rising edge of Reset#.
Interface to CPU

"Warm Reboot" occurs by clearing Reset Latch
This will reload the FPGA
This will not clear Boot Flag

Power up
FPGA_RESET# will still be asserted after FPGA is configured and can be used as a FPGA reset

CPU reload bit stream
CPU can also drive FPGA_RESET# low during a "soft" FPGA update

Bit stream should initialize EN_AVDD_OTG# deasserted (high)
After FPGA_RESET# deasserted, it should assert EN_AVDD_OTG# Then wait 10 ms, and write a "1" into the CPU RESET Latch

Xilinx LX25T_324 FPGA

25K equivalent LUTs
(15K 6-input LUTs)

177 DIO

30K Flip-flops

52 [2K x 9] Block RAM

2 PLLs + 4 DCMs

38 18x18 Multipliers

Each Mux has an adder and accumulator

CPU Reset Latch

"Warm Reboot" occurs by clearing Reset Latch
This will reload the FPGA
This will not clear Boot Flag

<table>
<thead>
<tr>
<th>Technologic Systems</th>
<th>Date</th>
<th>June 11, 2013</th>
</tr>
</thead>
<tbody>
<tr>
<td>Title: Xilinx FPGA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rev: A</td>
<td>Designer</td>
<td></td>
</tr>
<tr>
<td>Sheet 5 of 13</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Xilinx LX25T_324 FPGA

Gigabit Transceivers

FPGA_INIT# can be used to delay configuration
Also indicates load error

IO_SWAPEN_0 controls DIO during configuration. Low = PU enabled
High = All DIO are floating

Power and Special Functions

FPGA Reload

8MB SPI Flash

Page 162 GTP User Guide
Page 164-169
REF_CLK inputs have internal 100 ohm term.
must be cap coupled

All NC on LX25T

REF_CLK Input s have internal 100 ohm
term.
must be cap coupled

Giga bit
Xilinx LX25T_324 FPGA

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Xilinx LX25T_324 FPGA

Power and Special Functions

FPGA Reload

8MB SPI Flash
3.3V Power Supply

Power Supplies

1.8V Regulator

Power Sequencer

CPU Core Supply

Internal 3 ms delay
FPGA Core 1.2V

CPU
Debug UART

Reboot Flag

Keep normally at logic zero

Internal 3 ms delay

5V = 1.2V + 2.5% = 1.23V typ.

FPGA Core 1.2V
CPU Power

PXA168 PCIe rails must be connected to AN_1.8V.

CPU CORE

3.3V

DDR_1.5V

AVDD_OTG

AN_1.8V

SBC_USB_5V

CPU

CPU CORE

3.3V

DDR_1.5V

AVDD_OTG

AN_1.8V

SBC_USB_5V

Technologic Systems

Date: June 11, 2013

Title: TS-4740 CPU Power and Bypass caps

Rev: A  Designer  Sheet 9 of 13
Micro SD Card Socket

RTC and Temp. Sensor

eMMC 4GB

SD Card LEDs
PCIe 100 MHz
Clock Generator

12C interface allows changing amplitude and tri-stating outputs

Phase does not matter

Pins 7 and 8 have 100K PD on SI52142

EEPROM 1 Kbyte

I2C address is same as RTC!

CPU PCIe

FPGA GND

PCIe not supported on PXA166
Gigabit Ethernet Controller

MDRX supported in 10/100 modes

Technologic Systems
Title: TS-4740 Gigabit Ethernet Controller
Rev. A
Date June 11, 2013
Designer
Sheet 12 of 13
Two 100-pin Off-board Connectors

- "POWER" pins supply all power to the module. Apply 4.5V to 5.5V to these pins.
- "POWER" pins supply all power to the module.
- Power drain is approximately 600 mA.
- "POWER" pins supply all power to the module. Apply 4.5V to 5.5V to these pins.

- FPGA DIO
  - DIO_00
  - DIO_05
  - DIO_07
  - DIO_08
  - DIO_09
  - DIO_10
  - DIO_11
  - DIO_12
  - DIO_13

- JTAG
- FPGA_JTAG_TM
- BUS_WAIT#
- LCD_VSYNC
- BUS_BHE#
- BUS_CS#
- LCD_D20
- LCD_D19
- LCD_D18
- LCD_D16
- LCD_D15
- LCD_D12
- LCD_D10
- LCD_D09
- LCD_PWM
- LCD_CLK
- DIO_19
- LCD_DE

- Two 100-pin Off-board Connectors
- Bus Control
- Left
- Right

- Bus is not needed, all bus signals can be changed to DIO.
- Devices connected to this bus must never drive it when BUS_CCM is deasserted (must be off within 30 ns of deassertion).

- Devices must pull the BUS_W-AW low if they use more than 150 ns strobe.

- Must have 10Ω capacitors very near CN2 and GND for all "active" signals (between off points).

- Must have 10Ω capacitors very near CN2 and GND for all "active" signals (between off points).

- Maximum off-board load on ANS_1.8V is 10 mA.

- Pin 1 is the top left corner pin on the connector. All of the pins on the left are odd numbered. This may differ from the connector manufacturer’s datasheet.

- Title: TS-4740 Off-board Connectors
- Date: June 11, 2013
- Designer: A
- Sheet: 13 of 13