RXCLK must be biased low to enable internal 1.8V reg.

LAN8710i can power sequence in any order, except when using external 1.8V Core power.

Resistor PD on pin 18 is not required per data sheet. But Jesse could not get it to work until we added it.
The document appears to be a technical schematic diagram of a power management integrated circuit (PMIC). The schematic shows various components and connections, likely related to power distribution and management within an electronic device.

Key points from the schematic:
- The diagram includes labels for various voltages and currents, such as 3.3V Power Supply, 3.3V, and 1.8V DDR.
- There are connections and power sequence details, including power up to 1500 mA.
- Components like M11VGEN1 and M10VGEN1DRV are shown.
- There are references to coil values (2.2UH) and capacitor values (6.3V, 10 uF).
- The schematic includes various ICs and their associated components, such as TS-4800 PMIC, ISL8009A, and NSS12100X.

The text on the page includes notes about voltage levels and current requirements, such as:
- Voltage BP must rise above 3.2V to operate properly.
- Design fault: BP should not exceed 3.2V.
- Valid BP is 3.0 to 4.65V.
- Power sequence details for various voltages.

The diagram is complex and detailed, with a focus on power management and sequence, making it essential for understanding the power flow and operation of the device.
Title: Design Sheet of CPU Core

Peripheral Core

3.3V Caps

C132 C133 C134 C135 C136 C137 C138 C139 C140 C141 C142 C143 C144 C145 C146 C147 C148 C149 C150 C151 C152 C153 C154 C155 C156 C157 C158 C159

CPU Core

C117 C118 C119 C120 C121 C122 C123 C124 C125 C126 C127 C128 C129 C130 C131 C132 C133 C134 C135 C136 C137 C138 C139 C140 C141 C142 C143 C144 C145 C146 C147 C148 C149 C150 C151

RTC

Y2 XTAL_SM T_8X3

720-1005-2-ND 12.5 pF X tantal

Maxim has RTC with same pin-out

12 pF RTC

TS-4800 Temp, RTC, Caps, Boot Strap

Boot Strap Resistor

DAT08 = Boot Source
DAT13 and DAT14 = BT_MEM_CTL
DAT15 = BT_BUS_WIDTH
DAT20 and DAT21 = Boot Memory Type

Boot Strap Bias Resistors

use USB_OTG
Internal PHY
Don’t use EEPROM DCD
Boot Source
Boot @ 400 Mhz
SLC NAND
NAND
Page size
MUXed Data
Bias for Boot
Boot CPU at 400 Mhz

Technologic Systems

July 2, 2010

Title: TS-4800 Temp, RTC, Caps, Boot Strap

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