USB PHY

Micro SD Card Socket
FPGA with 5000 LUTs

FPGA 1.2V Reg.

LDO

1.2V

Measurments:

<table>
<thead>
<tr>
<th>Component</th>
<th>Measurement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage</td>
<td>1.2V</td>
</tr>
<tr>
<td>Stability</td>
<td>±5%</td>
</tr>
</tbody>
</table>

FPGA 0 has 20 DIO
Bank 1 has 6 DIO
Bank 2 has 18 DIO
Bank 3 has 4 DIO
Bank 4 has 8 DIO
Bank 5 has 18 DIO
Bank 6 has 8 DIO
Bank 7 has 18 DIO

FPGA pins can be swapped but only pins within each Power Rail

Set CONFIG_MODE to NONE
This allows all pins to be used

1 uF
18.2K
R99

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XP2-5 has:

- 50 LUTs
- 12 18x18 Multipliers
- 100 I/O with 166 pin package

- "reset on" = about 1.5 ms
- max PLL lock = 10 MHz

rstup and pull-down resistors
are 6 to 30k ohms

PMIC_STBY_REQ, PMIC_ON_REQ, and CPU_33Mhz have 3.2V levels

FPGA must be designed for that

Page 57 of Data Sheet (Bit Sockering)

Power Supplies can be sequenced in any order but must be monotonic.

All I/O lines are tri-stated during power cycling

Technologic Systems

July 2, 2010

Title: TS-4800 FPGA

Rev: Designer Sheet 4 of 9
RXCLK must be biased low to enable internal 1.8V reg.

Resistor PD on pin 18 is not required per data sheet. But Jesse could not get it to work until we added it.

PHy address = 0

PHY address and mode is locked on rising edge of Reset#.

Put MX515 in MII mode before deasserting Reset#.

LED1 = Activity/Link

LED2 = Speed 100 Mbit

LAN8710 can power sequence in any order, except when using external 1.8V Core power.
### Boot Strap Resisters

- **DAT_08** = Boot Source
- **DAT13 and DAT14** = BT_MEM_CTL
- **DAT15 = BT_BUS_WIDTH**
- **DAT20 and DAT31** = Boot Memory Type

- **24 MHz Osc**
- Low-power Boot mode disabled
- **UART1 used for Serial download**
- **BT_HPN_EN**
- **TBD3**

#### Temp Sensor

- 2.775V_BOOT
- 1.8V_DDR
- VCC
- 1.2V_DIG1
- VDD_GP
- 1.2uF
- C134
- 1.8V_DDR
- C152
- C155
- C156
- C157
- C159
- C165
- C168
- C169
- C170
- C198
- C86
- C87
- C83
- C90
- C95
- C96
- C97
- C99

### RTC

- 3.3V Caps
- 2.775V_BOOT
- 1.8V_DDR
- VCC
- 1.2V_DIG1
- VDD_GP
- 1.2uF
- C134
- 1.8V_DDR
- C152
- C155
- C156
- C157
- C159
- C165
- C168
- C169
- C170
- C198
- C86
- C87
- C83
- C90
- C95
- C96
- C97
- C99

### Resisters

- 6.04K
- R31
- Y2
- R32
- R60

### Rev: Design Sheet of Technologic Systems

**Title:** TS-4800 Temp, RTC, Caps, Boot Strap

**Date:** July 2, 2010

**Designer:**

**Sheet:** 7 of 9
Two 100-pin Off-board Connectors

FPGA JTAG

OFF_BD_RESET# is an Output used to reset all peripherals.

FPGA

POWER

OFF_BD_RESET# is an Output used to reset all peripherals.

SD Card

FPGA DIO

Bus Control

Boot Strap

Mode 2

SD Card

USB OTG D+

USB OTG D-

SPI_MOSI

SPI_CS#

2.775V_BOOT

1.8V_DDR

ETH_RX+

ETH_TX+

NC

HOSTA_USB_P

HOSTA_USB_M

USB_OTG_ID

CPU_JTAG_TCK

ONE_WIRE

AUD_TXD

AUD_FRM

CPU JTAG TDI

DISP_DAT15

DISP_DAT09

DISP_VSYNC

BUS_WAIT#

DIO_00

DIO_02

DIO_03

DIO_05

DIO_13

DIO_04

DIO_09

CONNECTION 1.5K OHM RESISTOR

OFF_BD_RESET# TO SET LOW

EXT_RESET# IS AN INPUT USED TO REBOOT THE CPU

DO NOT DRIVE ACTIVE HIGH (NEGATIVE EDGE)

All signals driving DIO on CN1 & CN2 must be powered by the 3.3V on CN2, or remain at 0V until the CN2 3.3V rail is > 3.0V

Maximum off-board load

on 2.775V, 1.8V, 1.2V

is 10 mA each

Maximum off-board load on TS_1.2V is 500 mA

USB Ports

Ethernet

Data Bus

Any I/O routed to a user accessible connector should have additional ESD protection placed on the connector board.

Device must pull the BUS_WAFW line low if they need more than 150 nA strobes

The data bus can not have more than

50 pF off-board capacitive loading

May need data buffer chip for heavy loads

Pin 1 is the top left corner pin on the connector. All of the pins on the left are odd numbered. This may differ from the connector manufacturer’s datasheet.