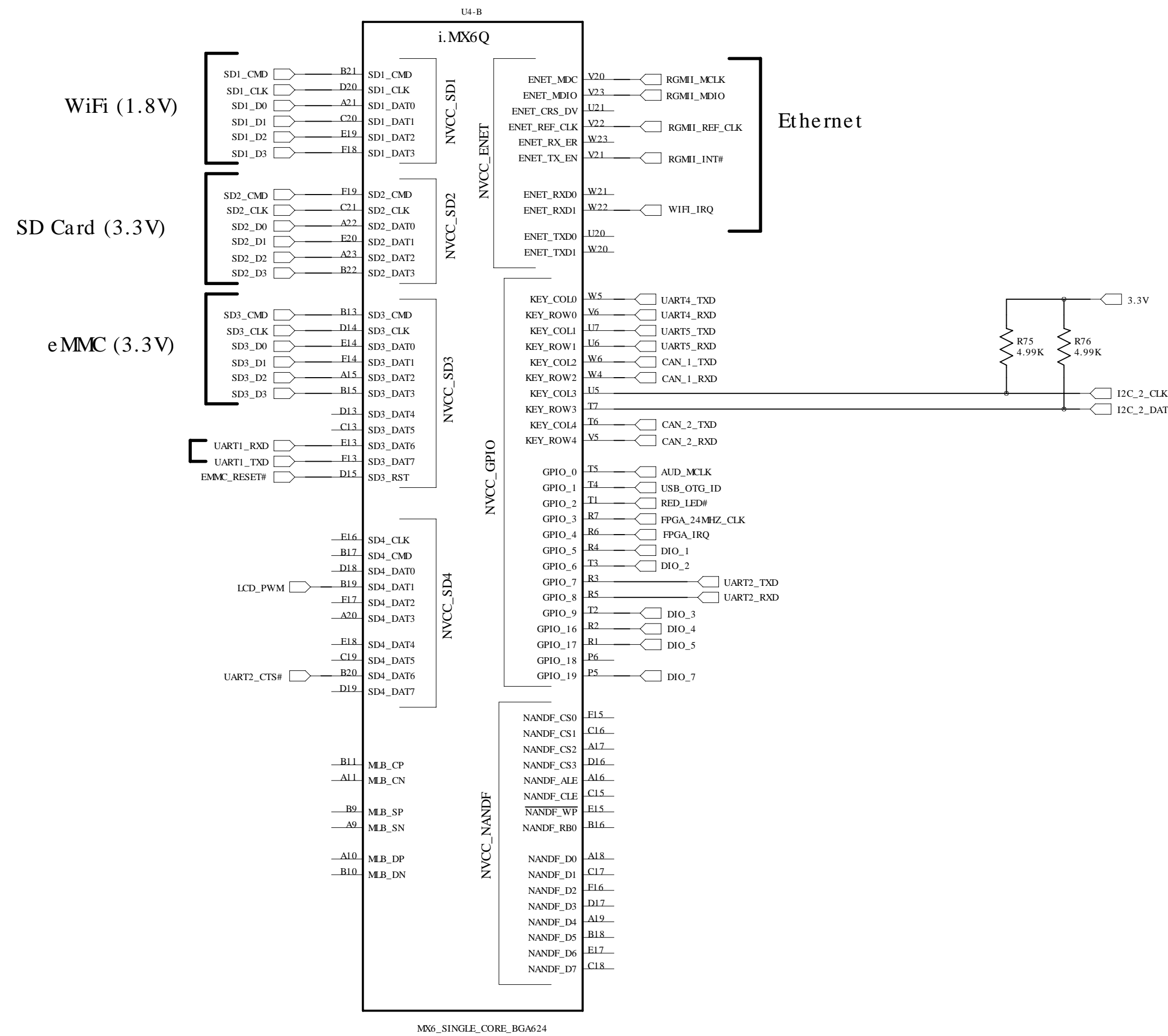
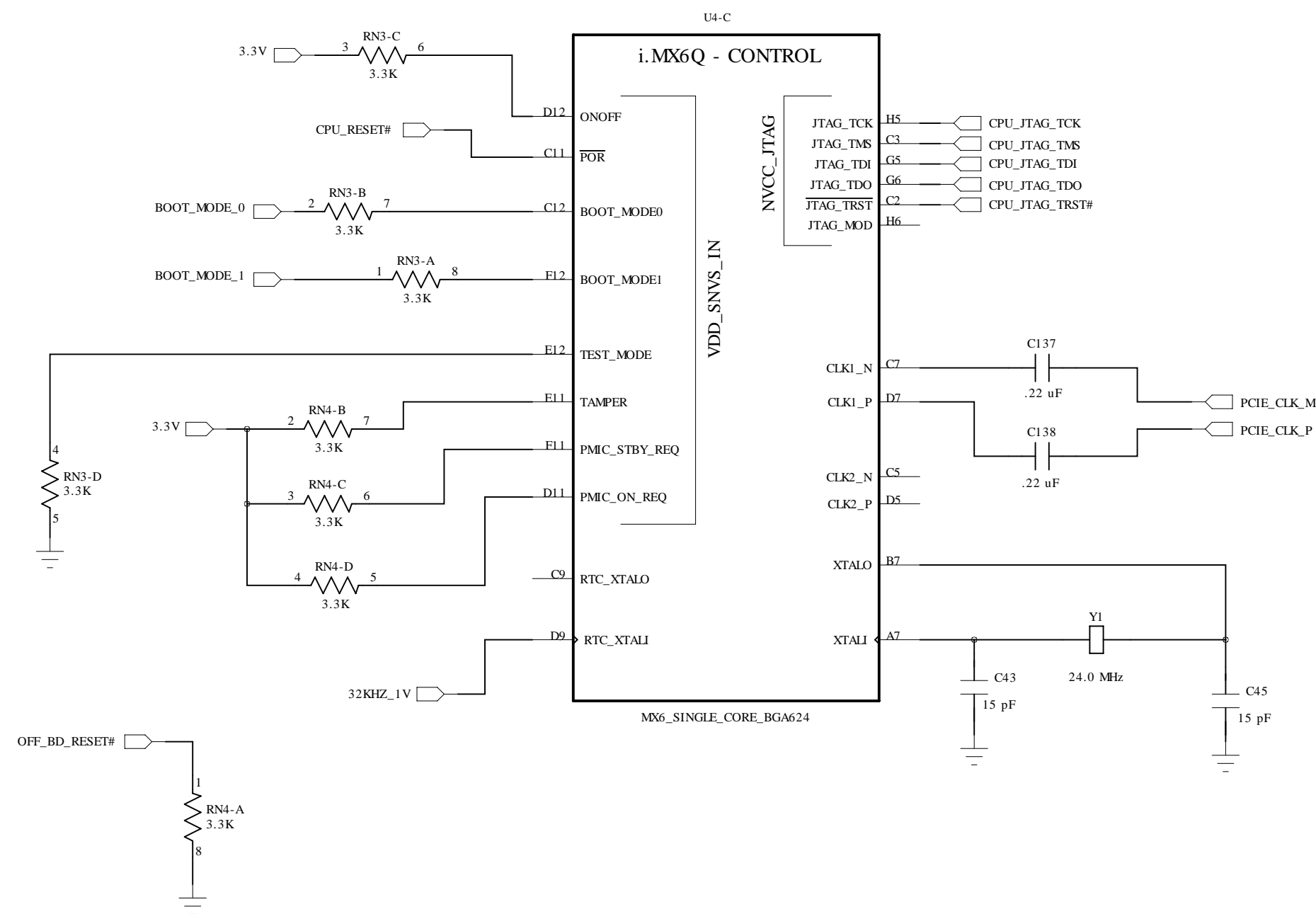


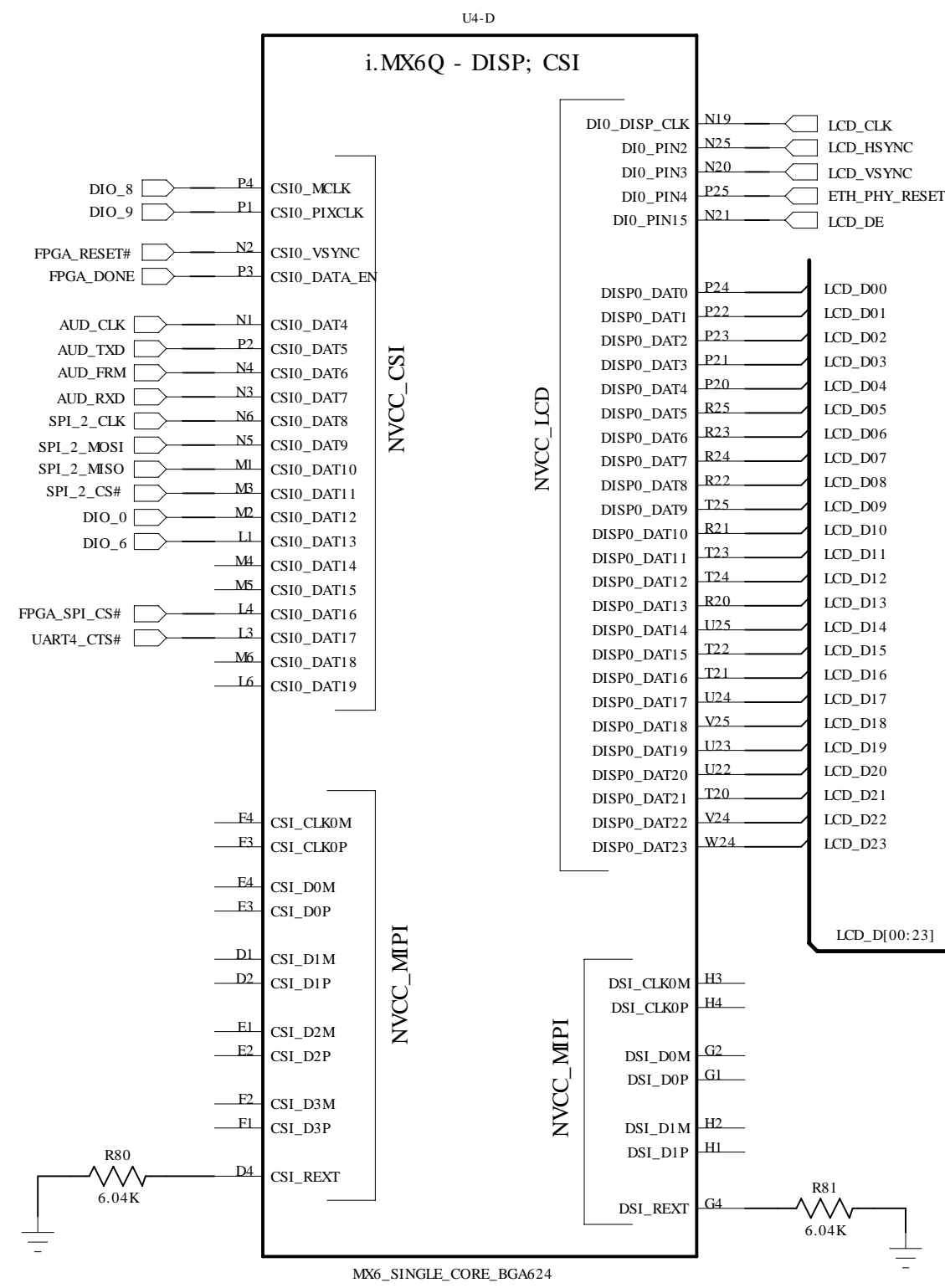
# SD, GPIO, NAND



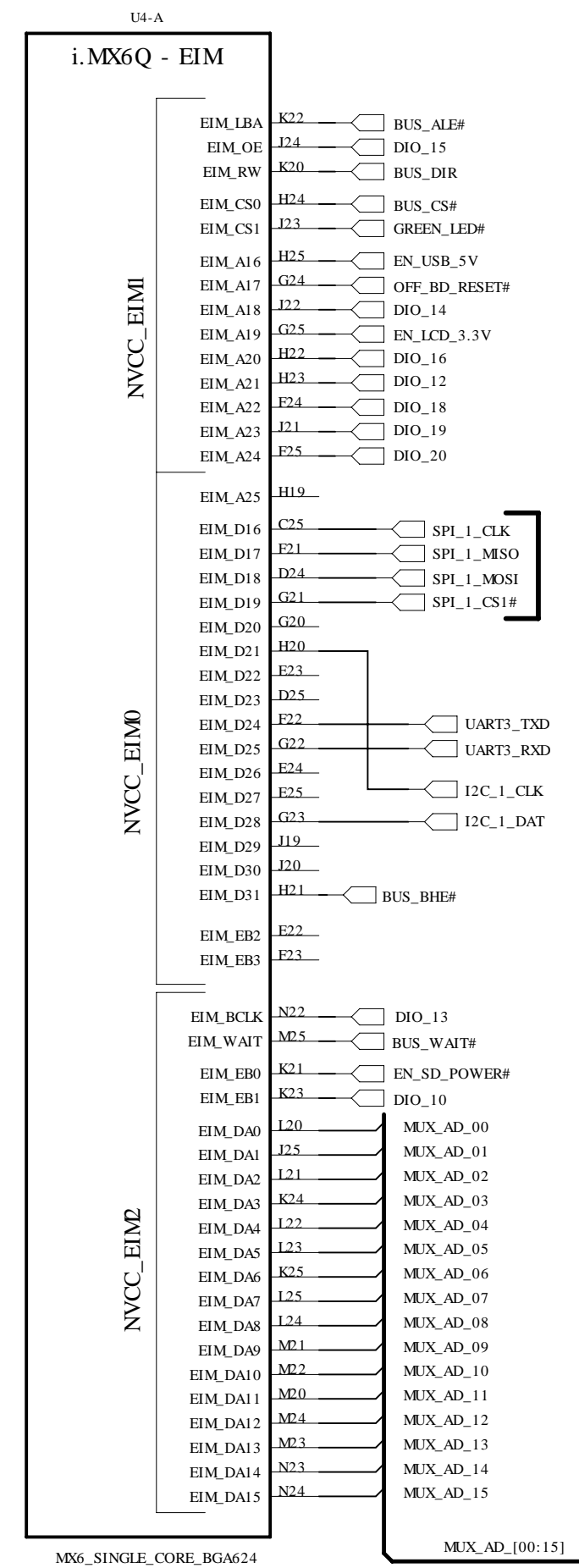
# Control



# LCD

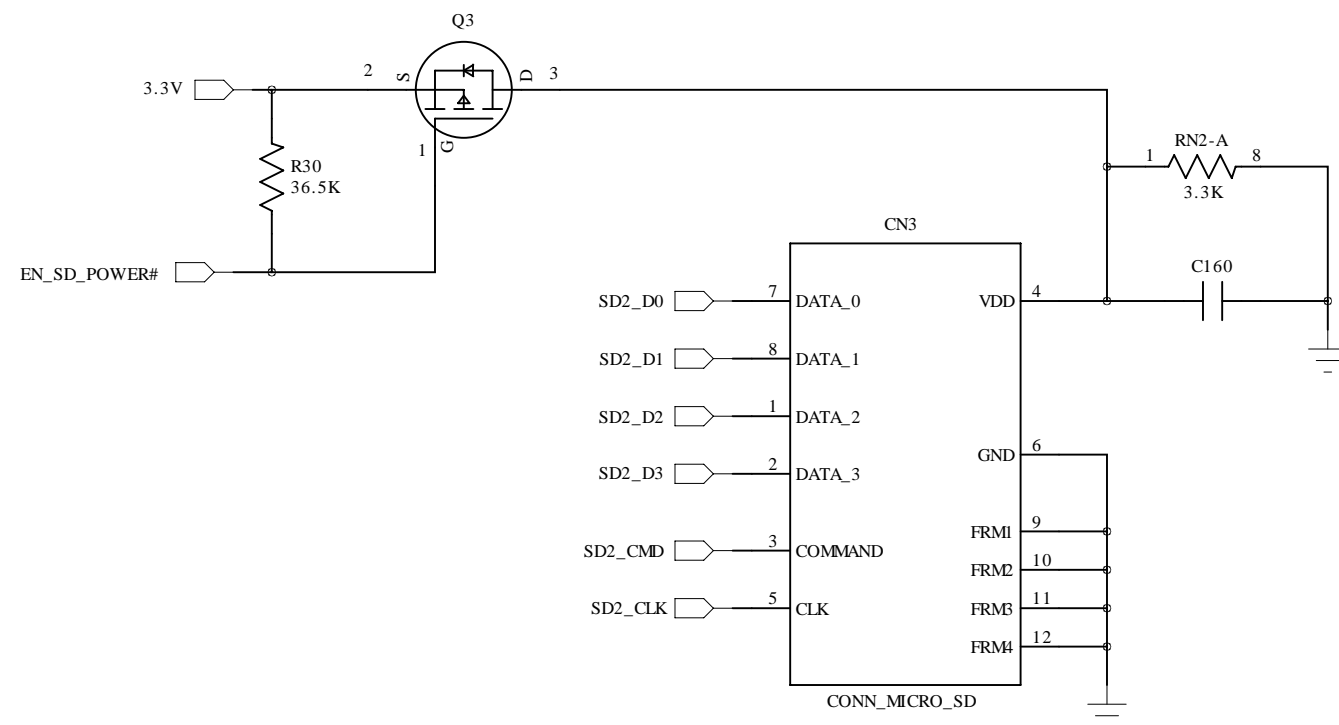


# EIM

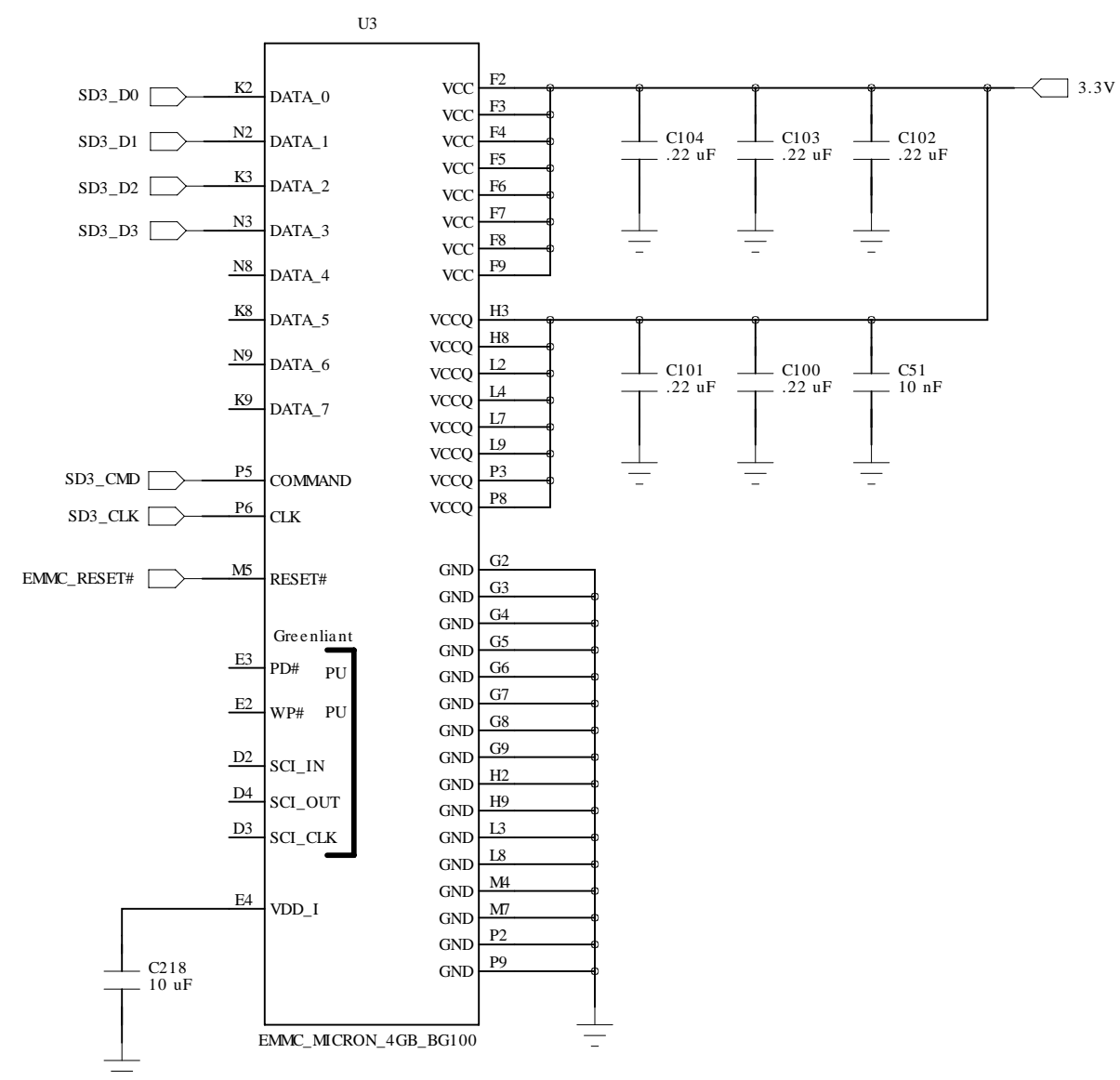


SPI BOOT

# Micro SD Card Socket

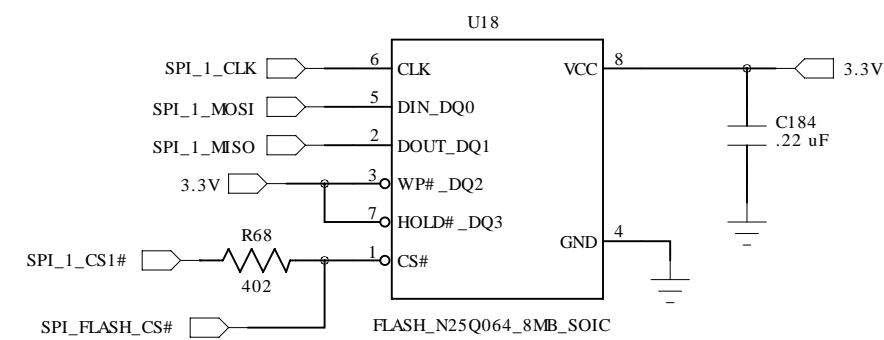


# eMMC 4GB



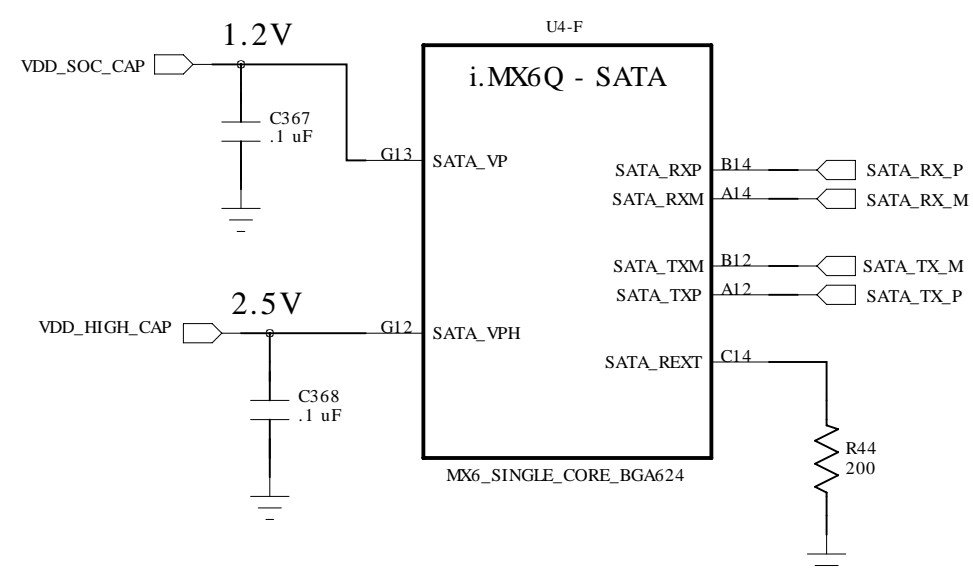
Technologic Systems	Date May 21, 2014
Title: TS-4900 SD card, eMMC	
Rev: A	Designer
Sheet 4 of 7	

# SPI Boot Flash

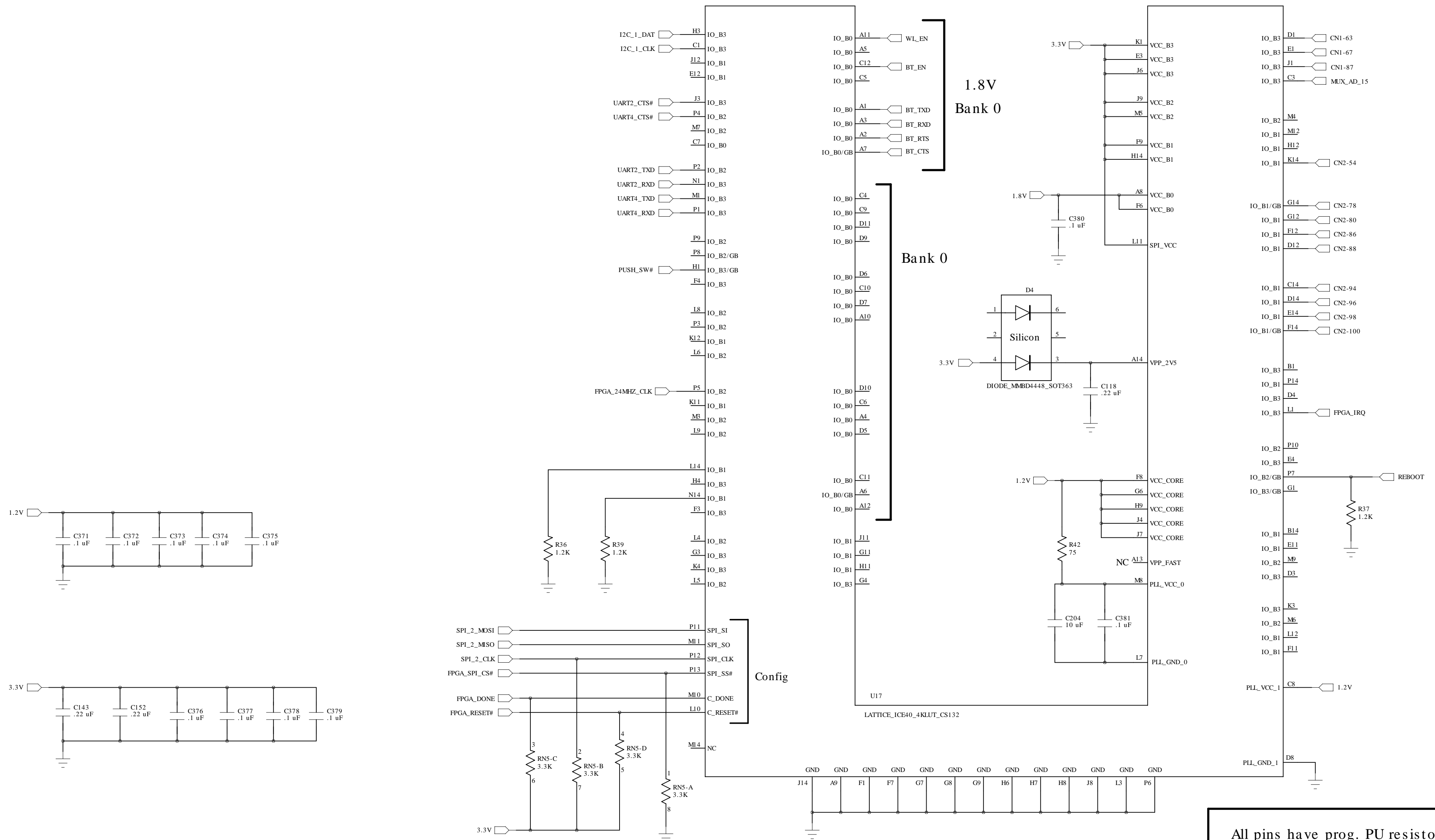


64 bytes of OTP

# SATA



# iCE40 FPGA



All pins have prog. PU resistor  
 Schmitt Trig. on all Inputs  
 10 MHz min clock for PLL  
 No Internal clock

# Two 100-pin Off-board Connectors

"5V" pins supply all power to the module  
Apply 4.5V to 5.5V to these pins

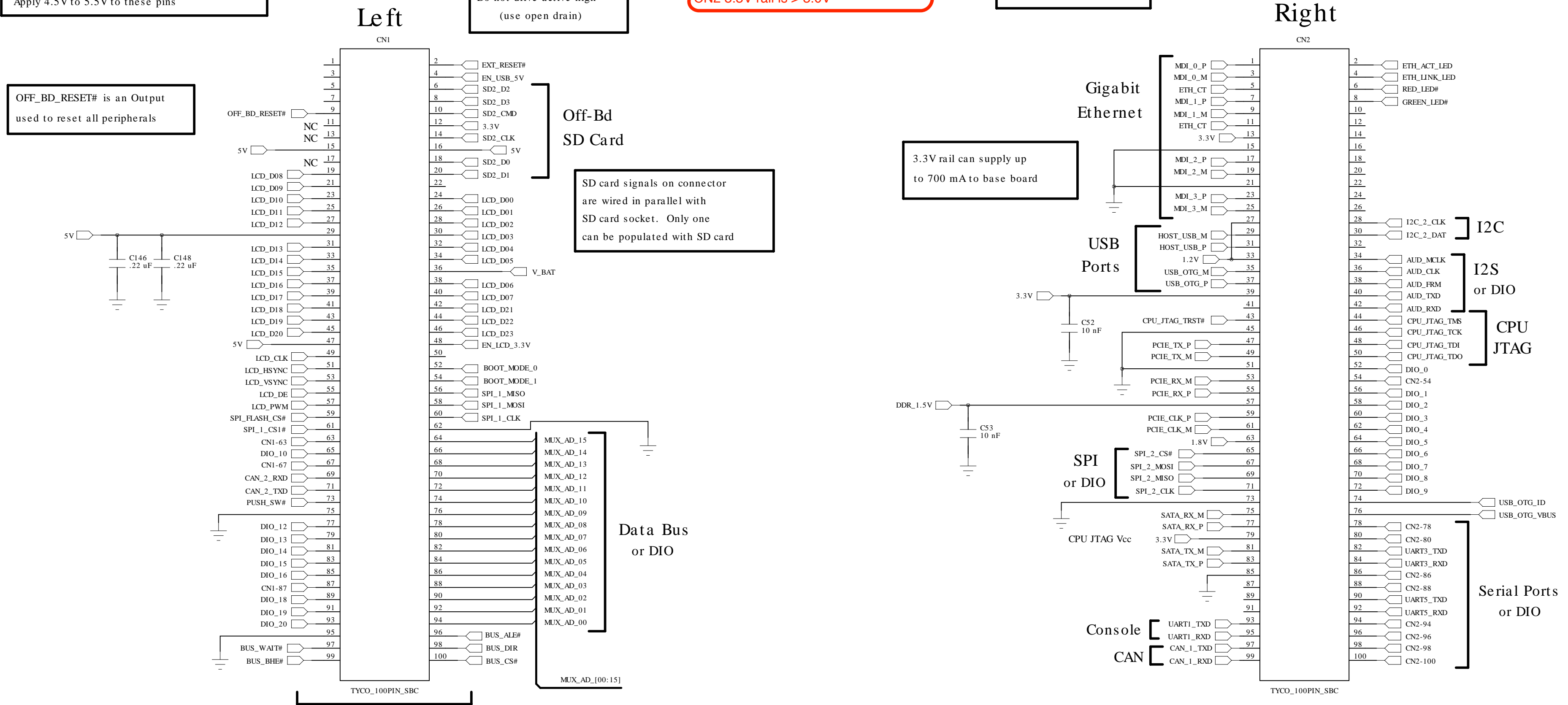
OFF\_BD\_RESET# is an Output  
used to reset all peripherals

EXT\_RESET# is an Input  
used to reboot the CPU  
  
Do not drive active high  
(use open drain)

⚠ All signals driving DIO on CN1 & CN2 must be powered by the 3.3V on CN2, or remain at 0V until the CN2 3.3V rail is > 3.0V

Must have 10 nF Capacitor  
very near CN2 and GND  
for all "quiet" signals  
(between diff pairs)

3.3V rail can supply up  
to 700 mA to base board



Off-Bd SD Card  
  
SD card signals on connector  
are wired in parallel with  
SD card socket. Only one  
can be populated with SD card

Data Bus  
or DIO

Bus Control

CN1-Pin 67 = UART0 TXEN

If Bus is not needed, all Bus  
signals can be changed to DIO

Devices connected to this bus must never  
drive it when BUS\_CS# is deasserted  
(must be off within 30 nS of deassertion)

Devices must pull the BUS\_WAIT# line low  
if they need more than 150 nS strobe

The data bus can not have more than  
30 pF of off-board capacitive loading  
May need data buffer chip for heavy loads

CN2-54 Codec CLK  
on the TS-8390

