Rev. A --> Rev. C Changes

Moved parts and copper away from mounting holes
Par interface pins were swapped

Biased BOOT_MODE_1 high
   and BOOT_MODE_0 low

5 LVDS diff pairs connected to CN2
CN2 pins 56, 58 and 60 go to different CPU DIO
Audio MCLK changed to CN2-54
CPU JTAG signals no longer connected to CN2
   CPU JTAG signals go to Test Points

Possible Heat Sinks for CPU

CTS # APF19-19-13CB/A01
CTS # APF19-19-10CB/A01
CTS # APF19-19-06CB/A01
RAM Data bits 32-63

Not populated for Single Core CPU
Control

This 100 MHz PCIe clock is OK for Rev 1.0 PCIe
But not for Rev 2.0

Errata - slow start up - 2ms

LVDS

HDMI
Micro SD Card Socket

eMMC 4GB

RTC and Temp. Sensor

BAT must be > 2.7V for temp comp to work
WiFi Radio

VBAT must power up first

SPI Boot Flash

64 bytes of OTP

SATA