TS-4900 Rev.C Schematic

Pages 0, 5, 10 and 11 not included

Rev.A --> Rev.C Changes

Moved parts and copper away from mounting holes

Par interface pins were swapped
U4.K23 and U4.H21 = CN1 pins 65 and 99

Biased BOOT_MODE_1 high
and BOOT_MODE_0 low

5 LVDS diff pairs connected to CN2

CN2 pins 56, 58 and 60 go to different CPU DIO

Audio MCLK changed to CN2-54

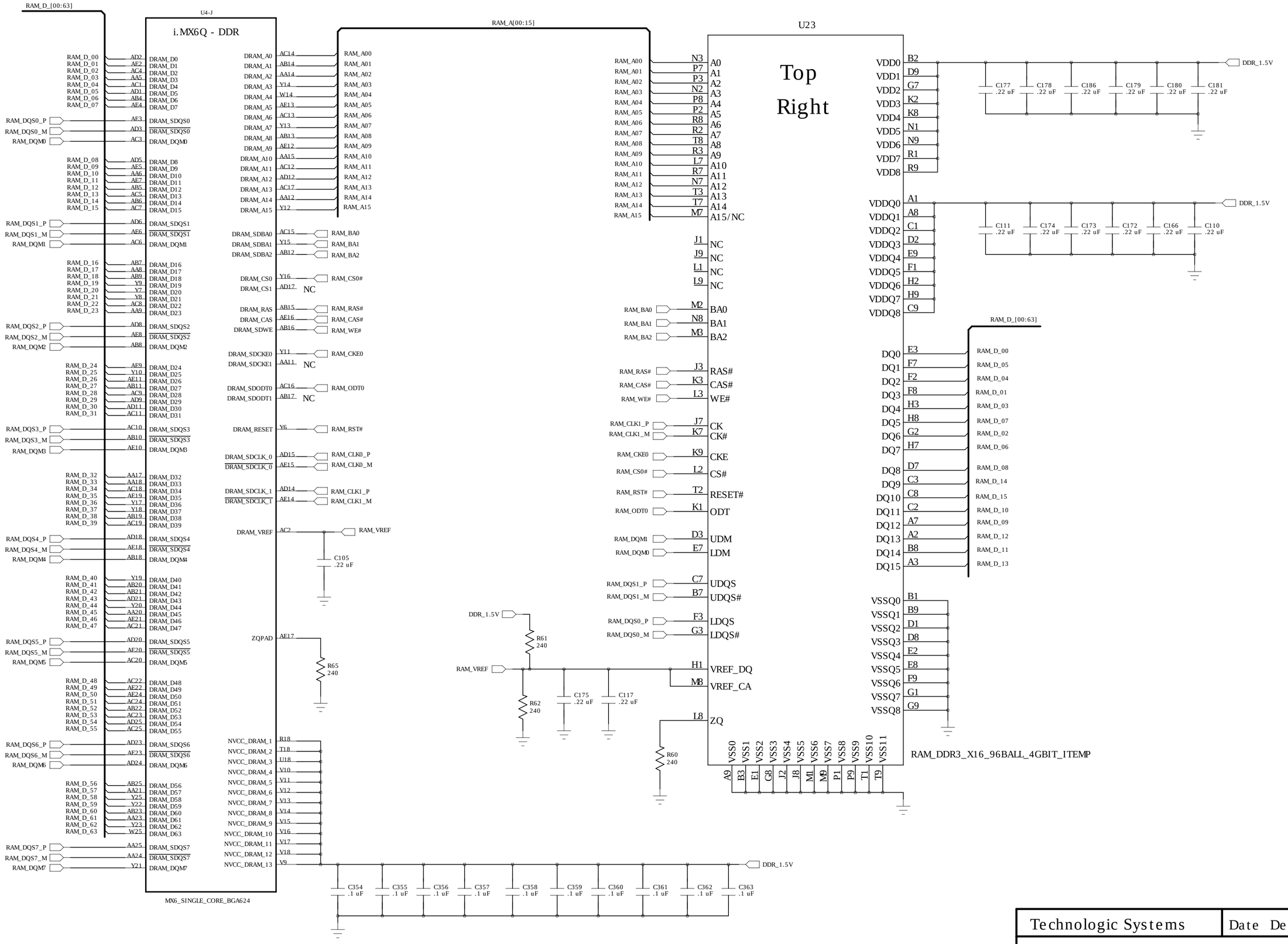
CPU JTAG signals no longer connected to CN2
CPU JTAG signals go to Test Points

Possible Heat Sinks for CPU

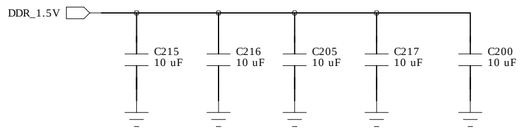
CTS # APF19-19-13CB/A01
CTS # APF19-19-10CB/A01
CTS # APF19-19-06CB/A01

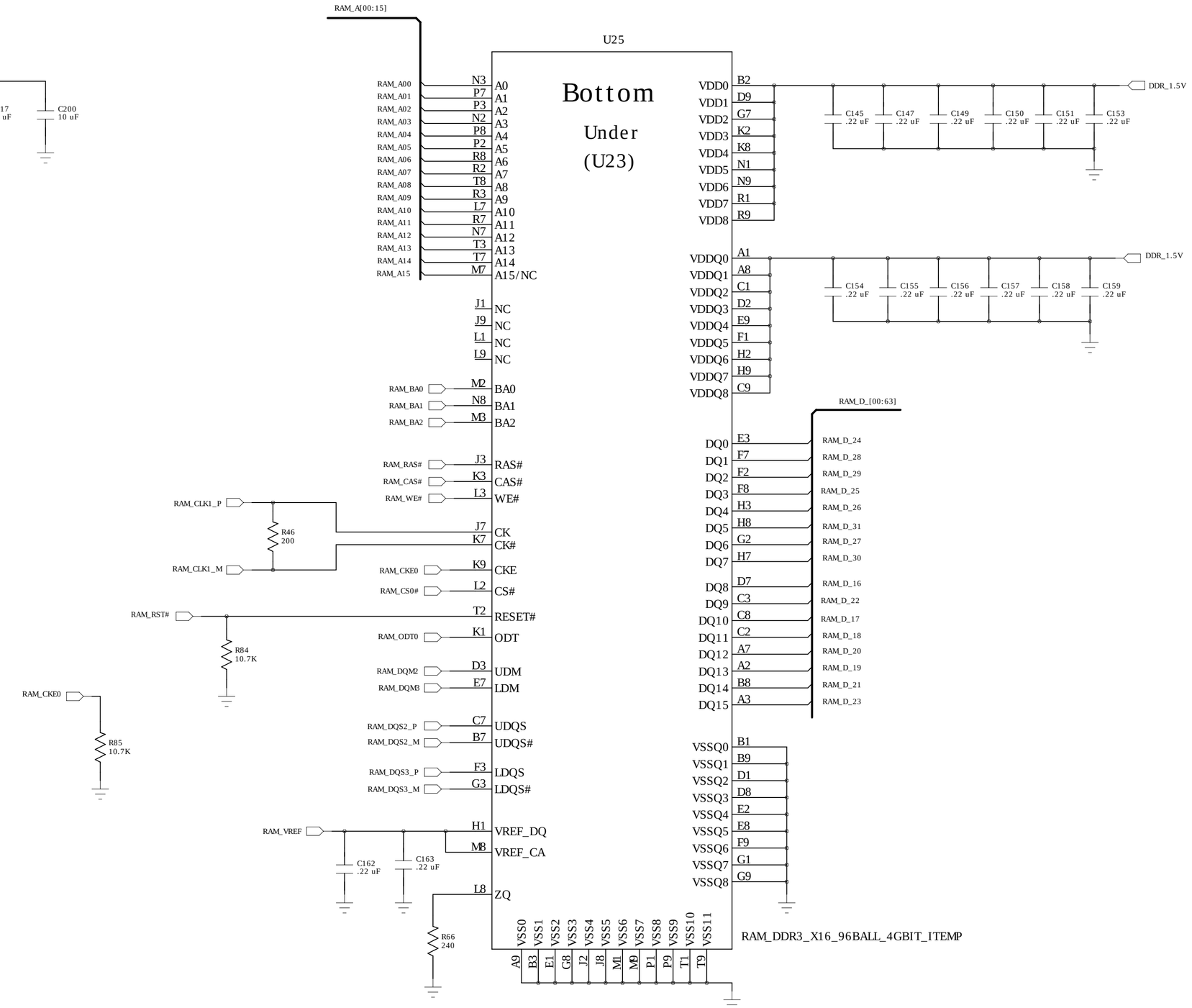
Technologic Systems	Date Dec. 5, 2014	
Title: TS-4900 MX6 SBC		
Rev: C	Designer	Sheet 1 of 15

512 MB per RAM Chip



Technologic Systems	Date Dec. 5, 2014	
Title: TS-4900 DDR3 RAM		
Rev: C	Designer	Sheet 2 of 15

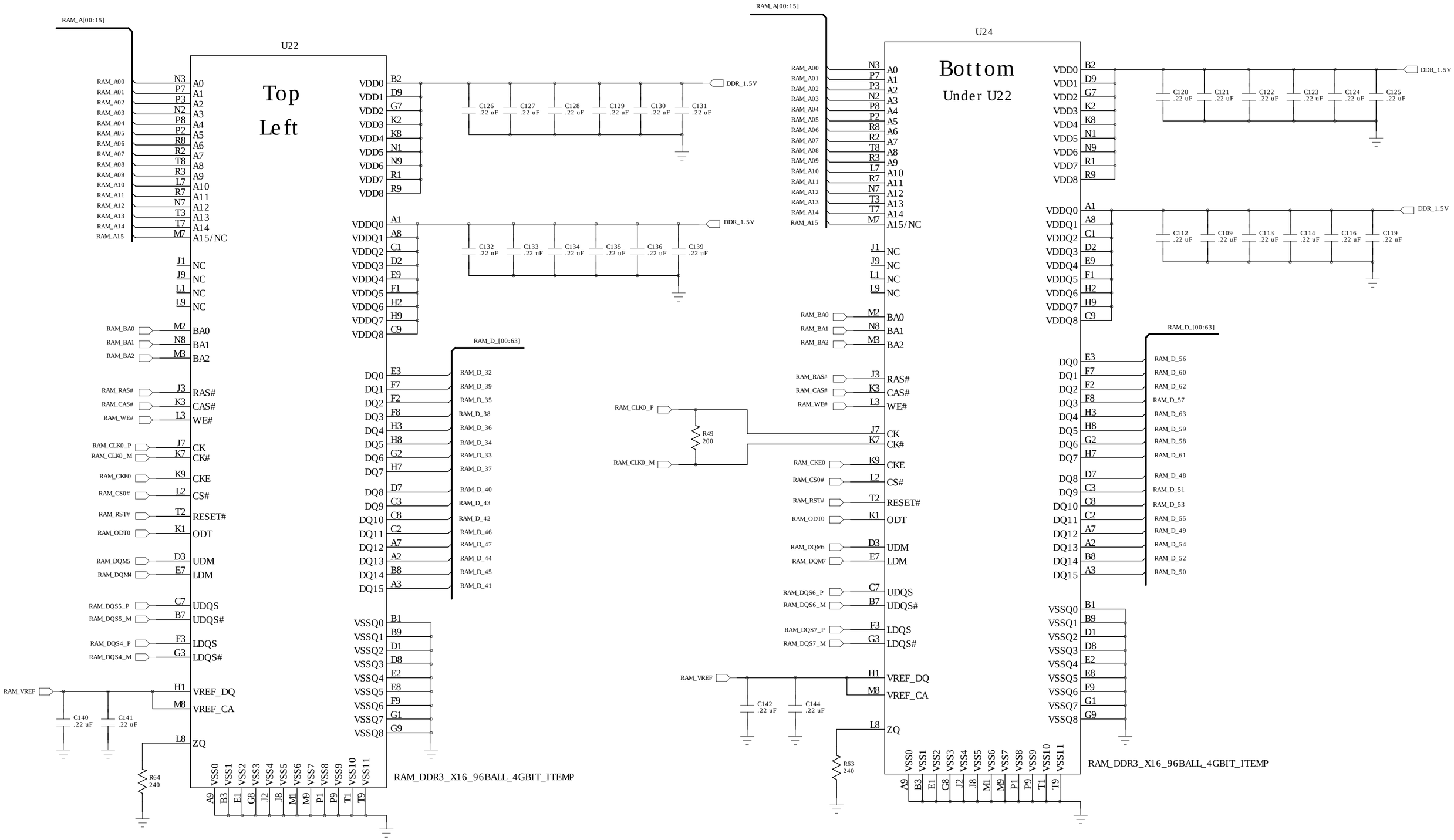




Technologic Systems	Date Dec. 5, 2014	
Title: TS-4900 DDR3 RAM		
Rev: C	Designer	Sheet 3 of 15

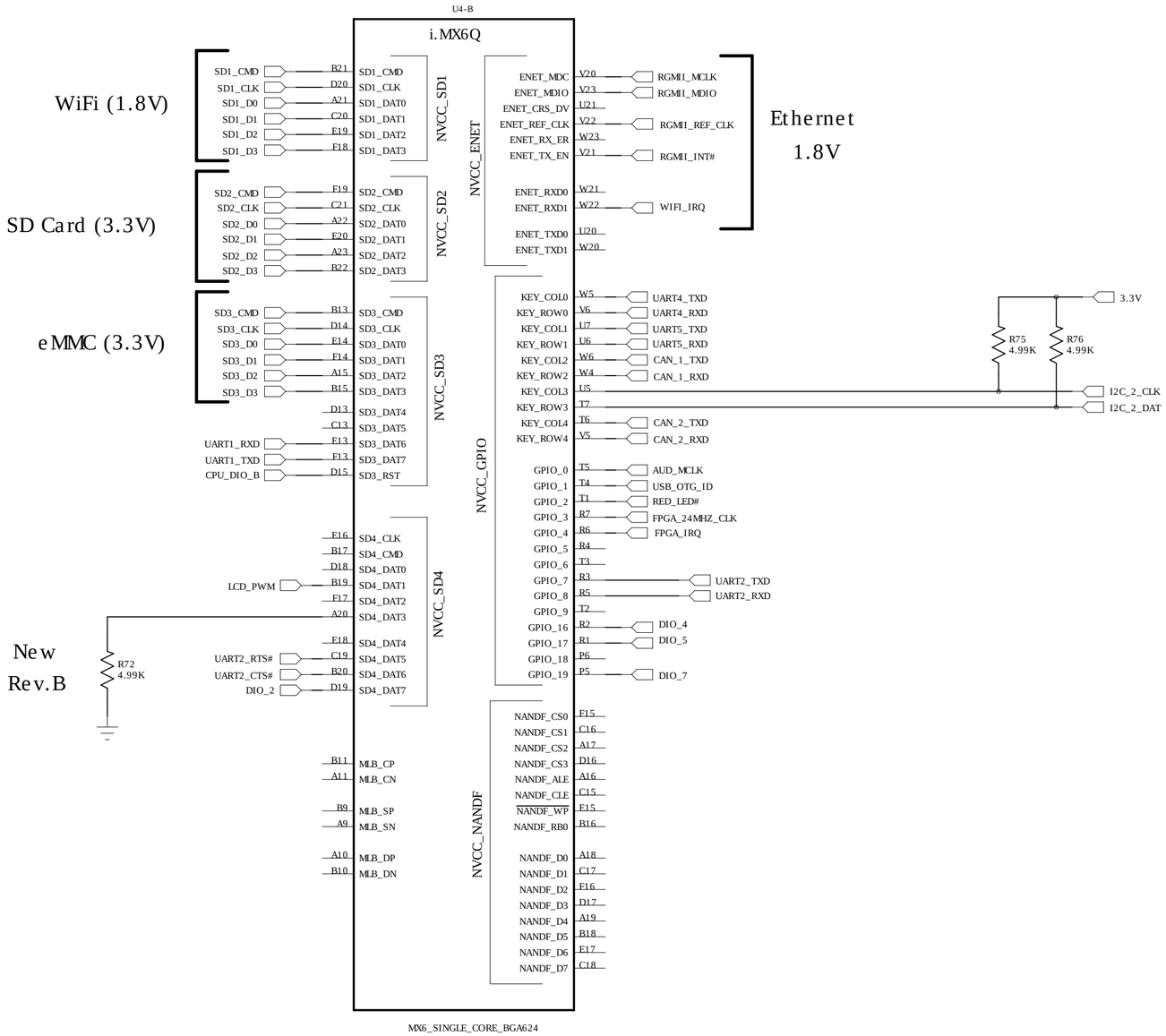
RAM Data bits 32-63

Not populated for Single Core CPU

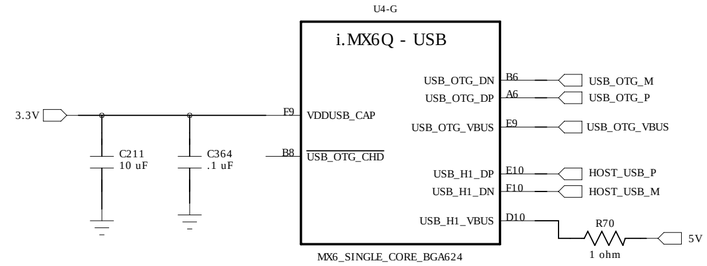


Technologic Systems		Date Dec. 5, 2014
Title: TS-4900 DDR3 RAM		
Rev: C	Designer	Sheet 4 of 15

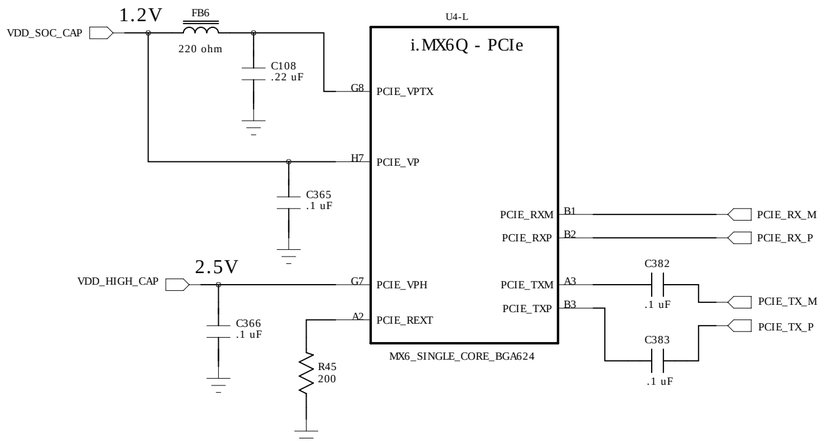
SD, GPIO, NAND



USB



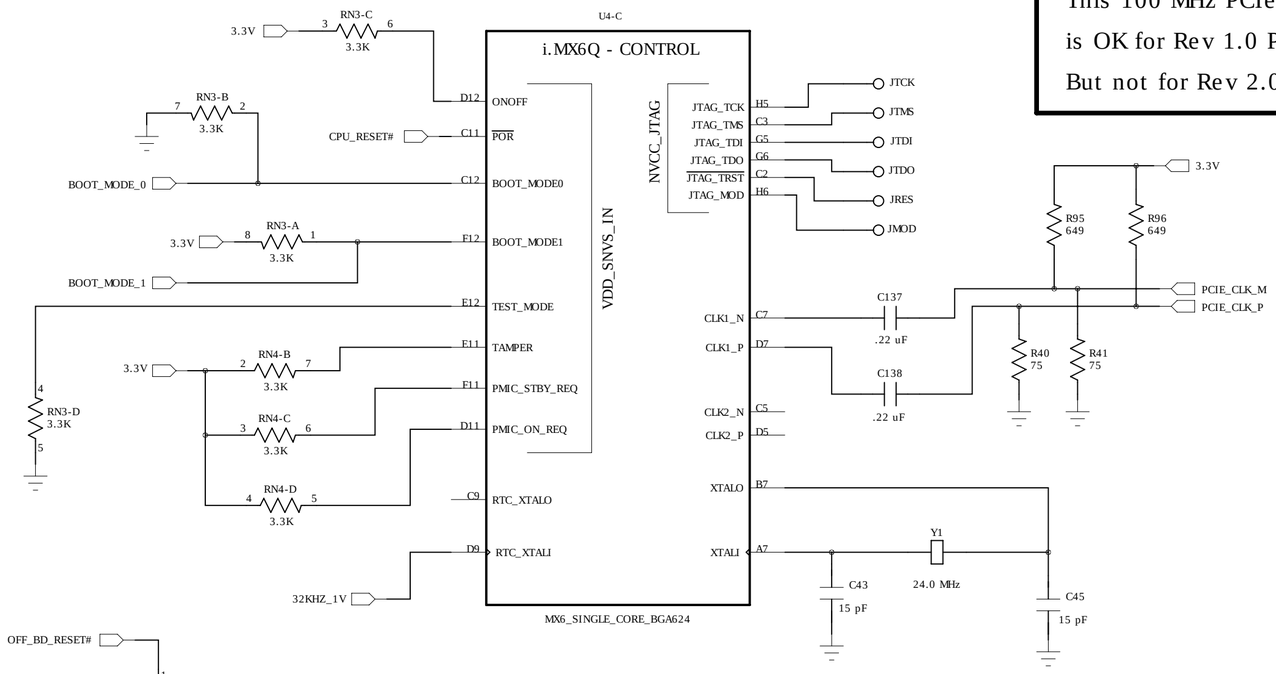
PCIe



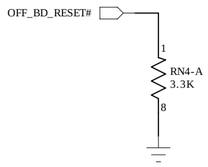
Technologic Systems	Date Dec. 5, 2014	
Title: TS-4900 MX6 SBC		
Rev: C	Designer	Sheet 6 of 15

Control

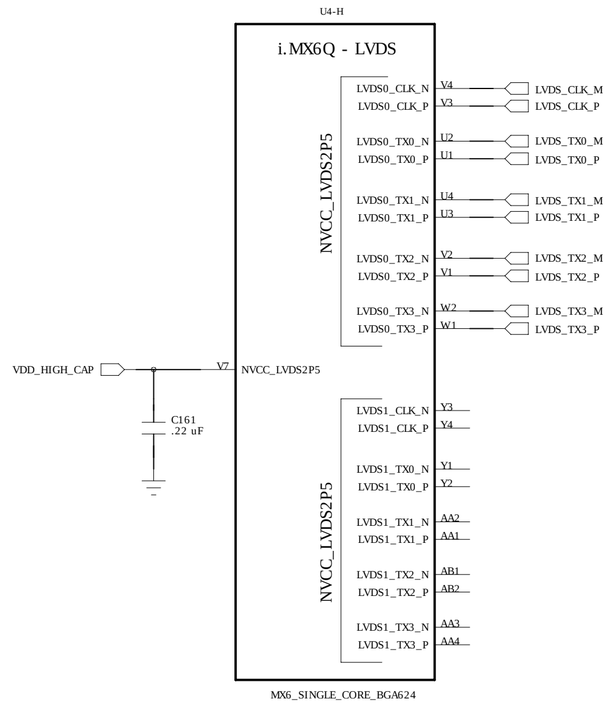
This 100 MHz PCIe clock
is OK for Rev 1.0 PCIe
But not for Rev 2.0



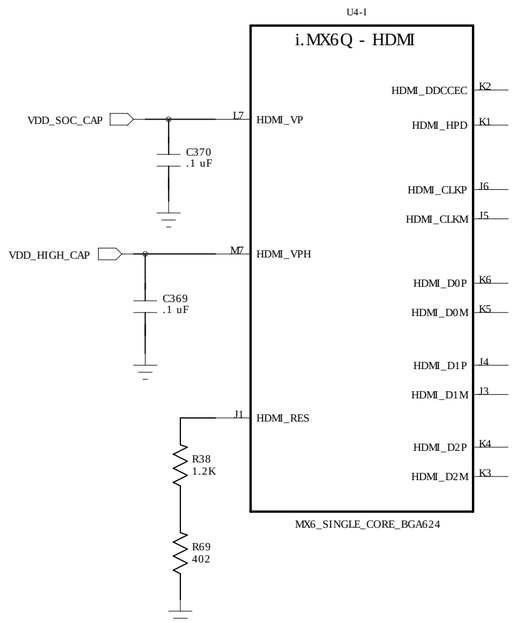
Errata - slow start up - 2ms



LVDS

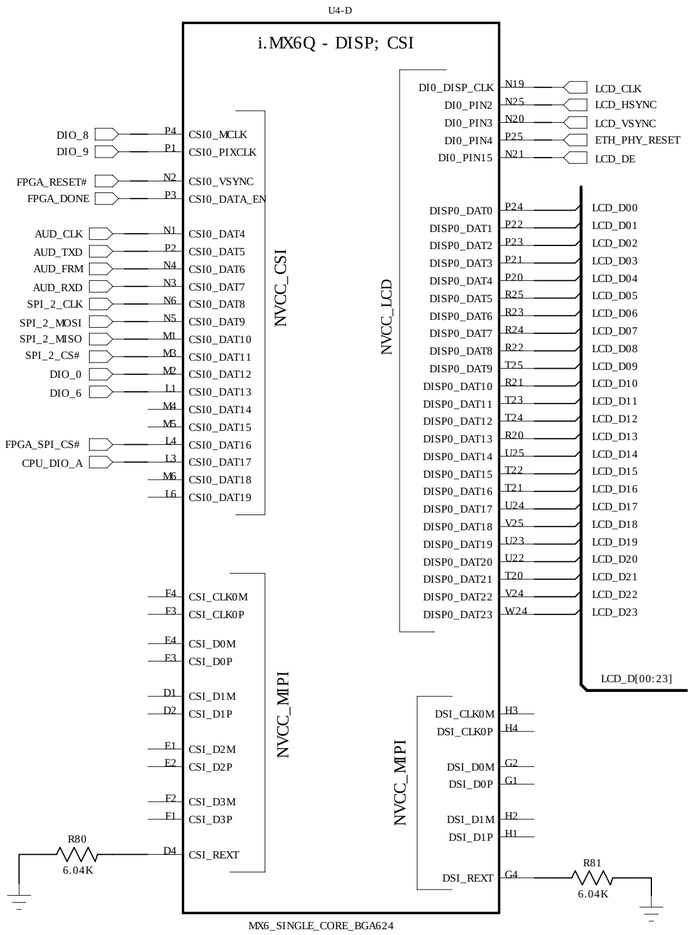


HDMI

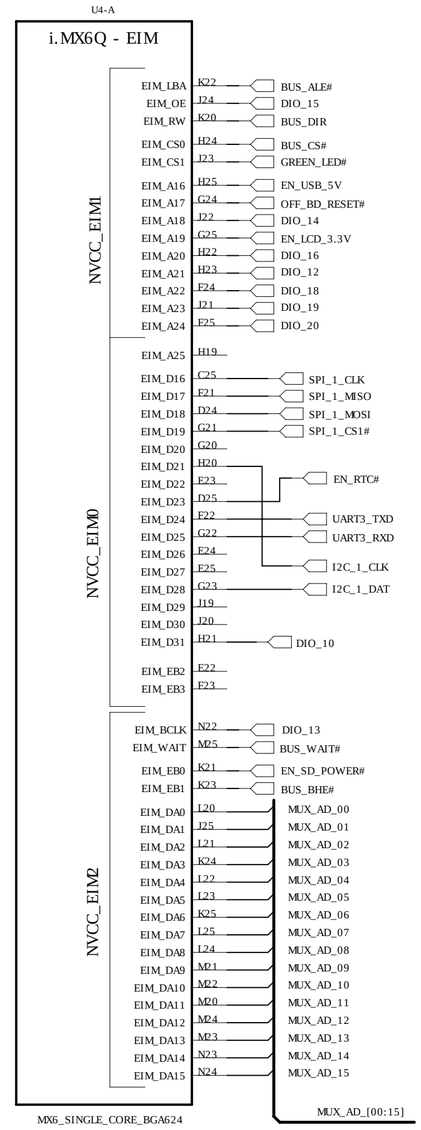


Technologic Systems		Date Dec. 5, 2014
Title: TS-4900		
Rev: C	Designer	Sheet 7 of 15

LCD

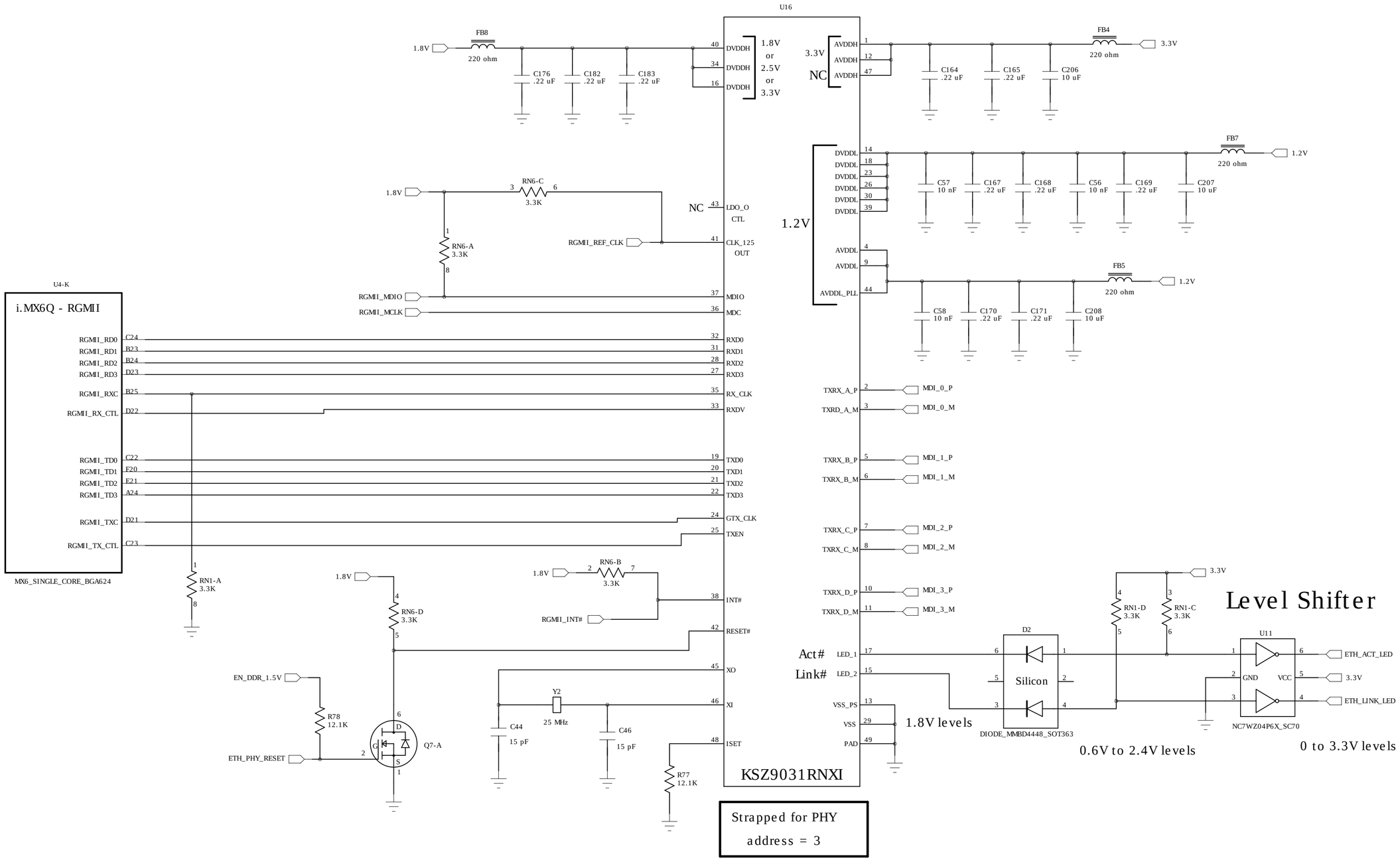


EIM



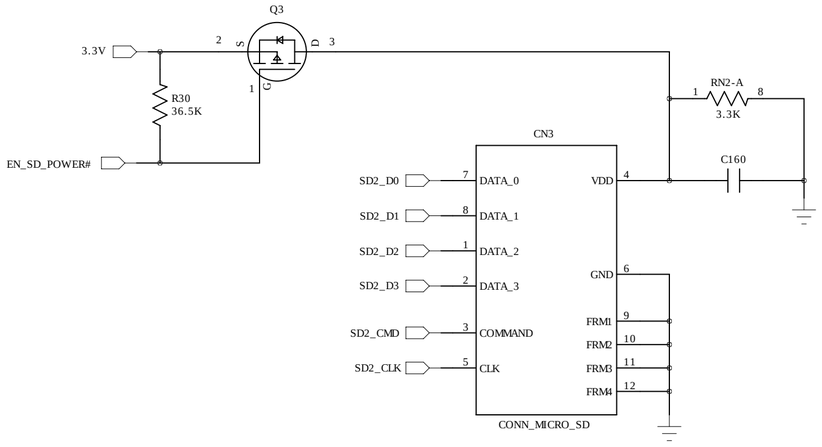
Technologic Systems	Date Dec. 5, 2014	
Title: TS-4900 LCD signals		
Rev: C	Designer	Sheet 8 of 15

10/100/1000 Ethernet PHY

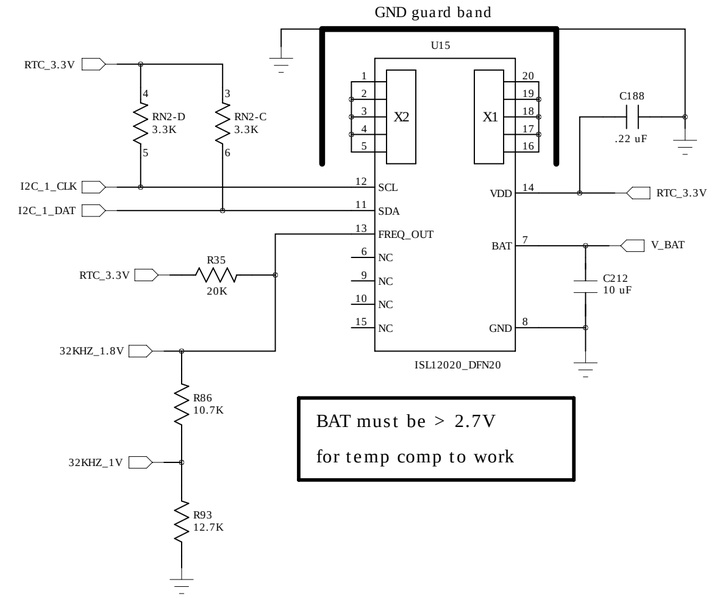


Technologic Systems	Date Dec. 5, 2014	
Title: TS-4900 Gigabit Ethernet PHY		
Rev: C	Designer RLM	Sheet 9 of 15

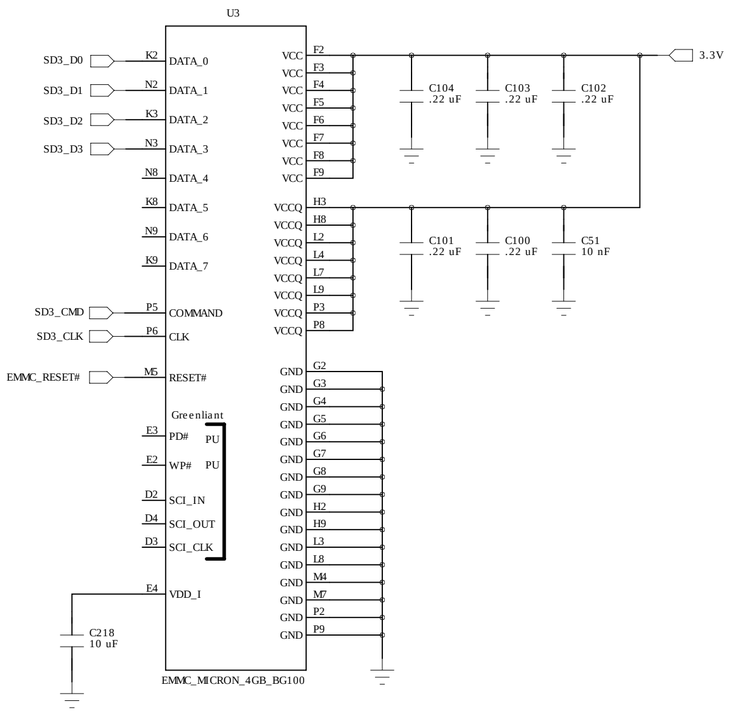
Micro SD Card Socket



RTC and Temp. Sensor



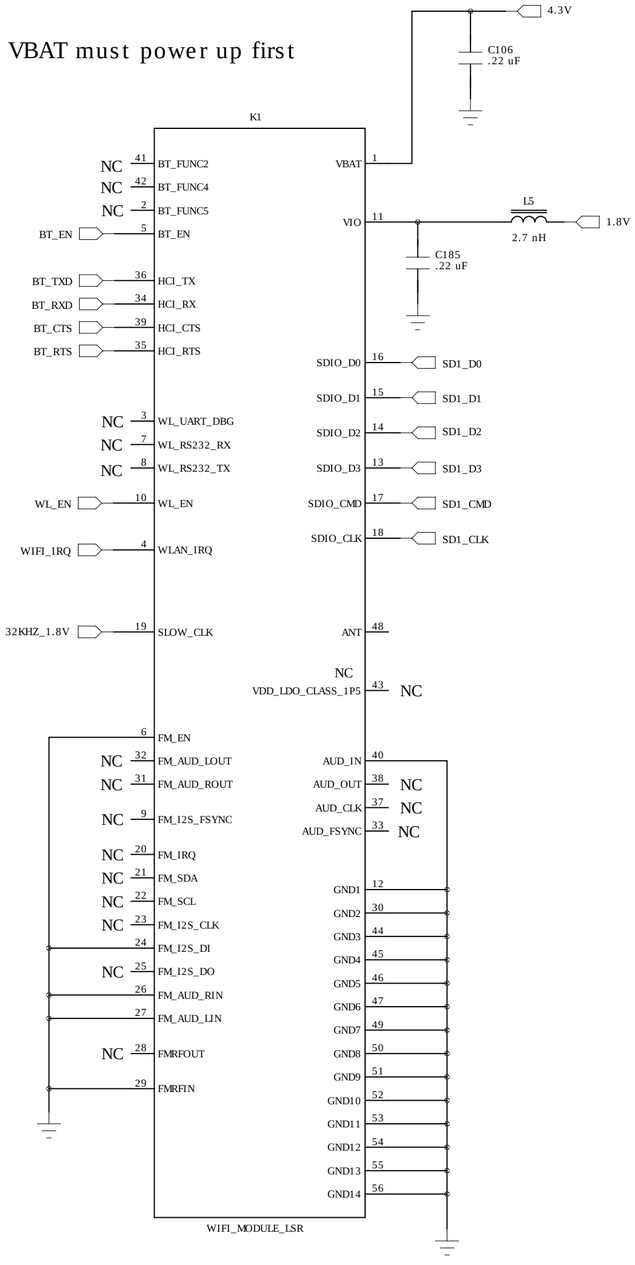
eMMC 4GB



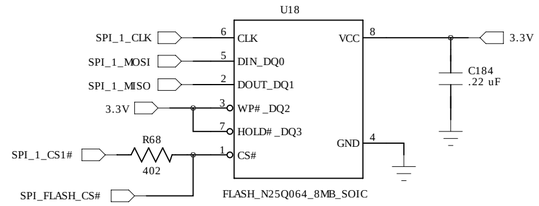
Technologic Systems	Date Dec. 5, 2014	
Title: TS-4900 SD card, RTC, Temp.		
Rev: C	Designer	Sheet 12 of 15

WiFi Radio

VBAT must power up first

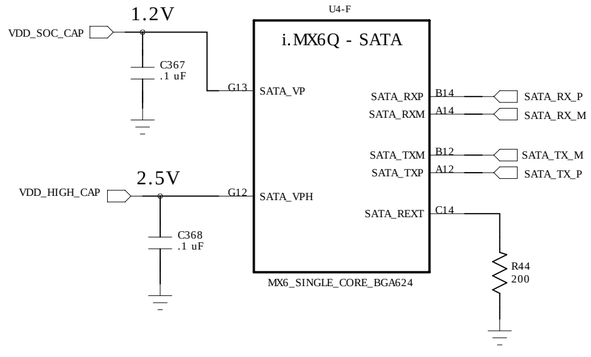


SPI Boot Flash



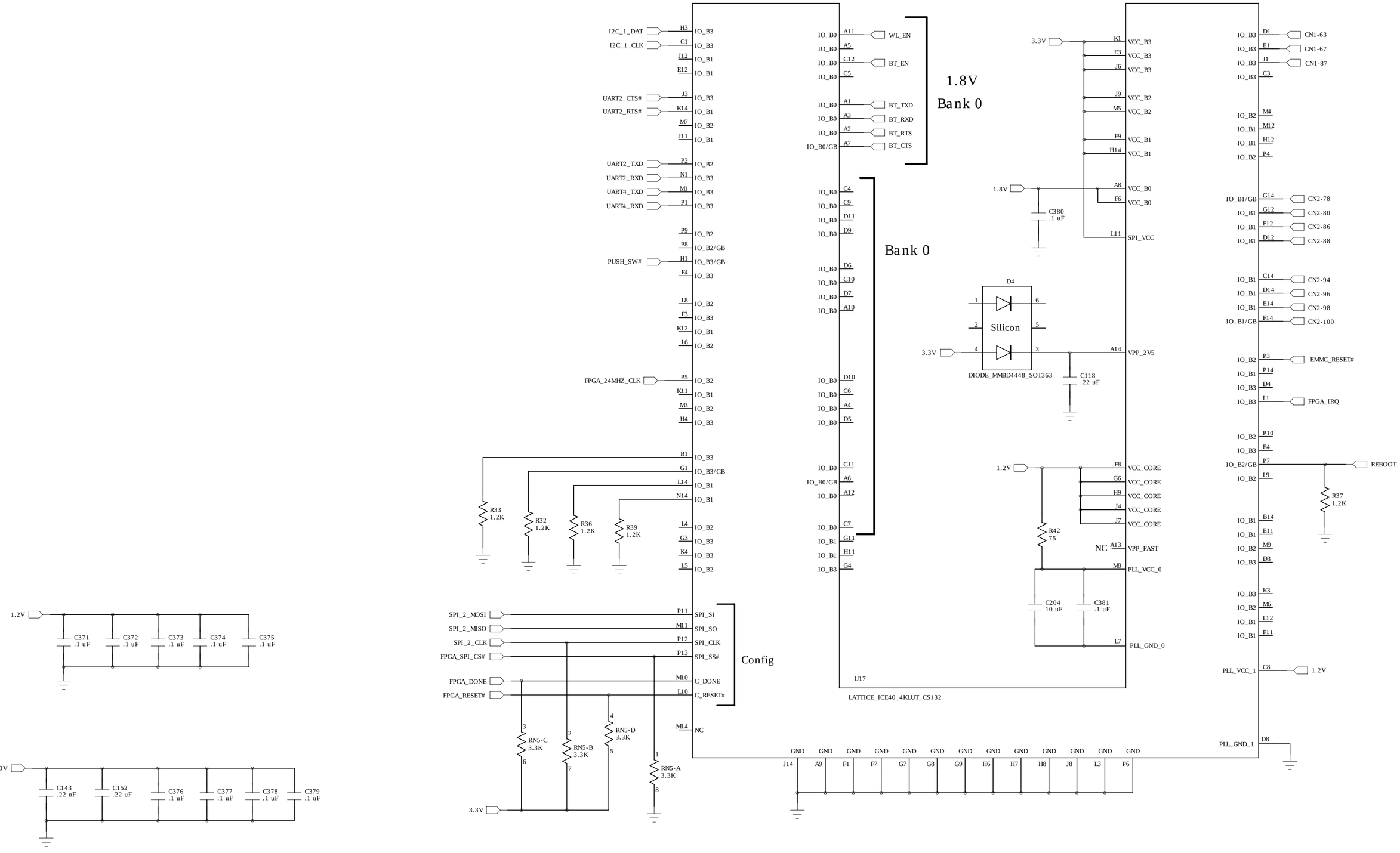
64 bytes of OTP

SATA



Technologic Systems	Date Dec. 5, 2014	
Title: TS-4900 WiFi		
Rev: C	Designer	Sheet 13 of 15

iCE40 FPGA



Technologic Systems	Date Dec. 5, 2014	
Title: TS-4900 iCE40 FPGA		
Rev: C	Designer	Sheet 14 of 15

Two 100-pin Off-board Connectors

"5V" pins supply all power to the module
Apply 4.5V to 5.5V to these pins

OFF_BD_RESET# is an Output
used to reset all peripherals

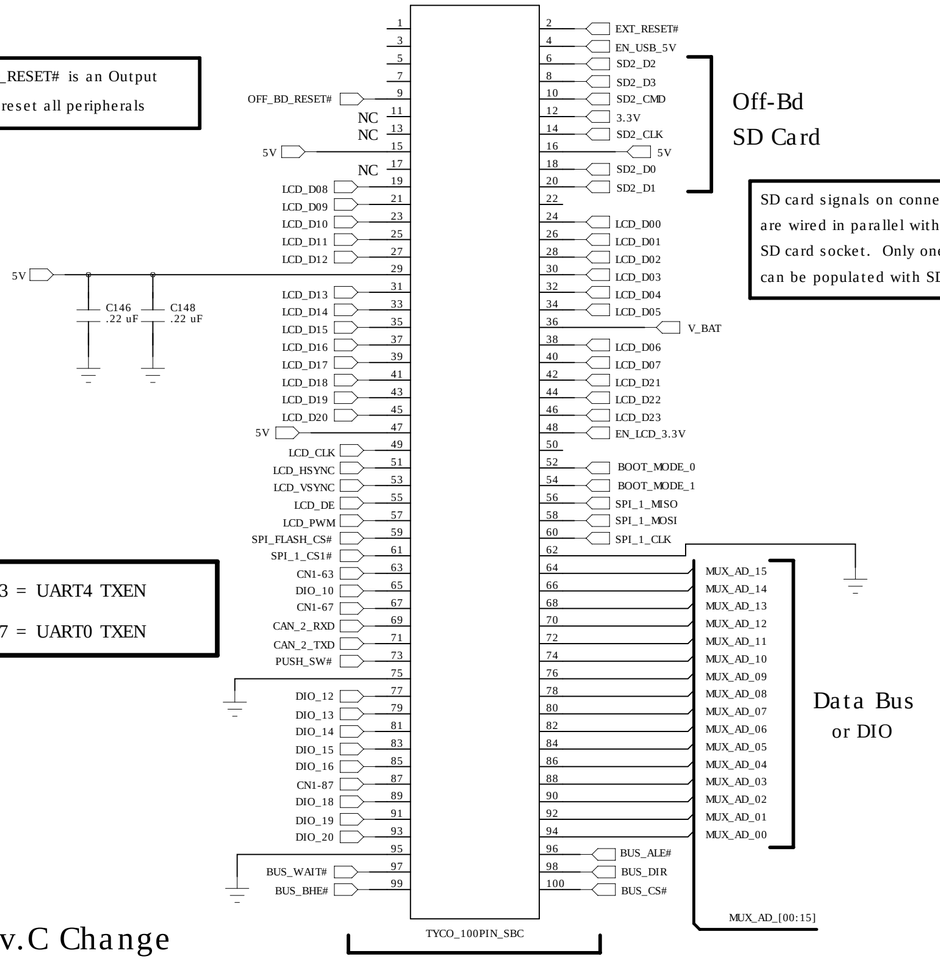
EXT_RESET# is an Input
used to reboot the CPU

Do not drive active high
(use open drain)

⚠ All signals driving DIO on CN1 & CN2 must be powered by the 3.3V on CN2, or remain at 0V until the CN2 3.3V rail is > 3.0V

Left

CN1



Off-Bd
SD Card

SD card signals on connector
are wired in parallel with
SD card socket. Only one
can be populated with SD card

Data Bus
or DIO

Bus Control

CN1-Pin 63 = UART4 TXEN

CN1-Pin 67 = UART0 TXEN

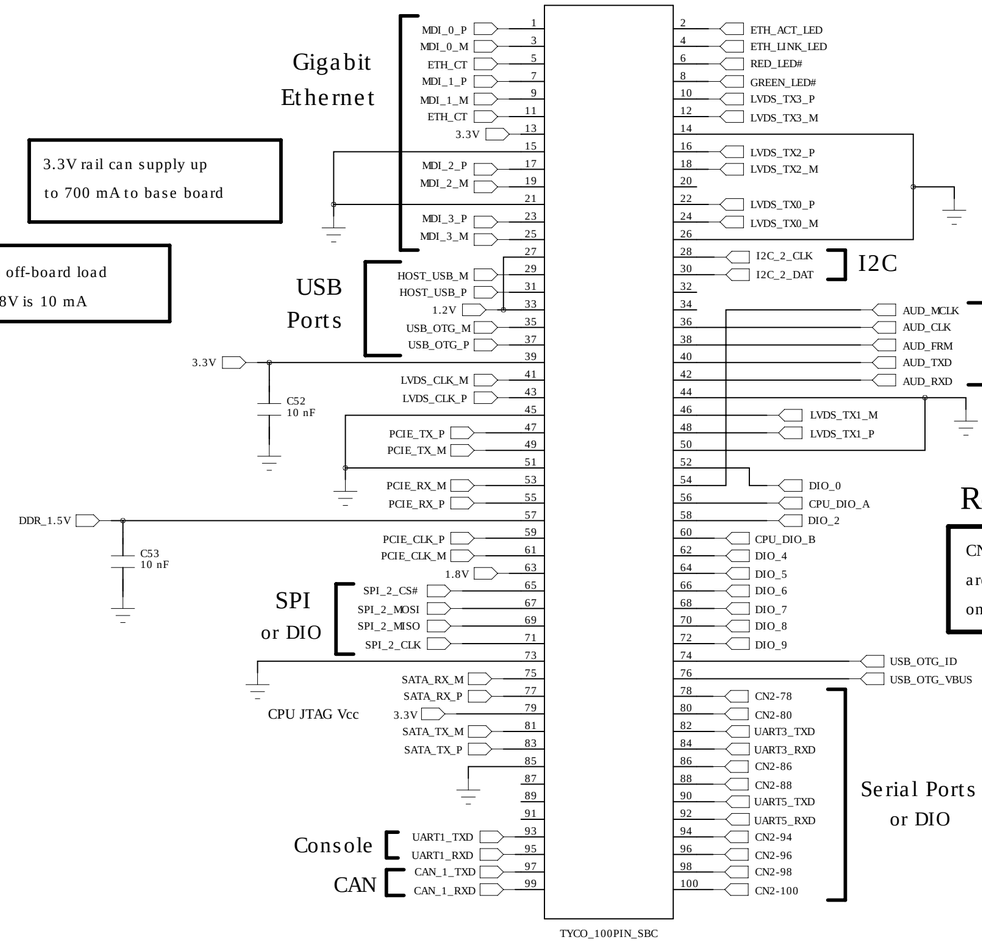
Rev.C Change

CN1-65 (DIO_10) and CN1-99
were swapped on CPU

If Bus is not needed, all Bus
signals can be changed to DIO

Right

CN2



Gigabit
Ethernet

3.3V rail can supply up
to 700 mA to base board

Maximum off-board load
on AN_1.8V is 10 mA

USB
Ports

I2C

I2S
or DIO

SPI
or DIO

CPU JTAG Vcc

Console

CAN

Serial Ports
or DIO

Rev.C Change

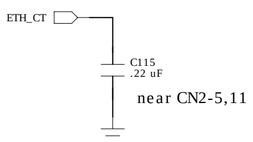
CN2 pins 56, 58, and 60
are different iMX6 balls
on Rev.C than on Rev.A

LVDS pairs are
length matched

PCIe Diff Pairs have
been Polarity swapped

SATA can NOT have
polarity swapped

SATA and PCIe Diff pairs do
NOT have to be length matched



Technologic Systems		Date Dec. 5, 2014
Title: TS-4900 Off-board Connectors		
Rev: C	Designer	Sheet 15 of 15