**TS-4900 iMX6 SBC**

### Options

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Option 2</td>
<td>TS-4900-1024-S10S-C Single core, 1 GHz, no WiFi, no RTC, no eMMC, 1GByte RAM, (0 to 70)</td>
</tr>
<tr>
<td>Option 3</td>
<td>TS-4900-1024-4096F-S8S-RTC-I Single core, 800 MHz, no WiFi, 1 GByte RAM (~0 to 85)</td>
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<tr>
<td>Option 4</td>
<td>TS-4900-1024-4096F-S8S-RTC-WIFI-I Single core, 800 MHz, with WiFi, 1 GByte RAM (~0 to 85)</td>
</tr>
<tr>
<td>Option 5</td>
<td>TS-4900-2048-4096F-Q10S-RTC-E Quad core, 1 GHz, no WiFi, 2GByte RAM, (Temp -20 to 85)</td>
</tr>
<tr>
<td>Option 6</td>
<td>TS-4900-2048-4096F-Q10S-RTC-WIFI-E Quad core, 1 GHz, with WiFi, 2GByte RAM, (Temp -20 to 85)</td>
</tr>
</tbody>
</table>

### Rev.A --> Rev.C Changes

- Moved parts and copper away from mounting holes
- Pin interface pins were swapped
- Biased BOOT_MODE_1 high
  - and BOOT_MODE_0 low
- 5 LVDS diff pairs connected to CN2
- CN2 pins 56, 58 and 60 go to different CPU DIO
- Audio MCLK changed to CN2-54
- CPU JTAG signals no longer connected to CN2
- CPU JTAG signals go to Test Points

### Rev.D changes:

- Allow external PCIe 100 MHz CLK
- No layout change needed - BOM change
- Added 4mm keep out around iMX6 top layer for new heat sink
- Changed to 153-ball eMMC
- Added EIM Byte strobe to CN1 pin 22
  - FPGA ball "P4" controls SD power
- Allow FPGA to be 1-time programmed
  - For Windows CE applications
  - Requires PU on FPGA_SPI_CS#
  - Also connect to CN2 pin 34
- Ball "L6" on CPU is GND, to indicate Rev.D
- JTAG ball "H6" is GND
- CN1 pin 12 is wrong, but can't change it

Web Schematic: Some proprietary information has been withheld.
RAM Data bits 32-63
Not populated for Single Core CPU
Control

This 100 MHz PCIe clock is OK for Rev 1.0 PCIe
But not for Rev 2.0

Errata - slow start up - 2ms
Micro SD Card Socket

RTC and Temp. Sensor

eMMC 4GB

BAT must be > 2.7V for temp comp to work

EN_RTC# has weak PU on CPU DIO
At system power up, FET is off
Two 100-pin Off-board Connectors

- CN1-63 = UART4 TXEN
- CN1-67 = UART0 TXEN

- CN1-Pin 65 (DIO_10) and CN1-99 were swapped on CPU

- EXT_RESET# is an Input used to reset all peripherals

- OFF_BD_RESET# is an Output used to reset all peripherals

- Sata and PCIe Diff pairs do NOT have to be length matched

- Any I/O routed to a user accessible connector should have additional ESD protection placed on the carrier board.

- MUX_AD_01 to MUX_AD_15

- SD Card can be populated with SD card socket. Only one is wired in parallel with SD card socket. Only one can be populated with SD card.

- 1.8V DDR_1.5V 3.3V rail can supply up to 700 mA to base board

- Maximum off-board load on AN_1.8V is 10 mA

- 3.3V rail can supply up to 700 mA to base board

- LVDS pairs are length matched

- SATA can NOT have polarity swapped

- PCIe Diff Pairs have been Polarity swapped

- Serial Ports or DIO

- USB Ports

- Gigabit Ethernet

- Two 100-pin Off-board Connectors