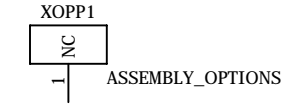


TS-4900 iMX6 SBC

Options



Option 2	TS-4900-1024-S10S-C	Single core, 1 GHz, no WiFi, no RTC, no eMMC, 1GByte RAM, (0 to 70)
Option 3	TS-4900-1024-4096F-S8S-RTC-I	Single core, 800 MHz, no WiFi, 1 GByte RAM (-40 to 85)
Option 4	TS-4900-1024-4096F-S8S-RTC-WIFI-I	Single core, 800 MHz, with WiFi, 1 GByte RAM (-40 to 85)
Option 5	TS-4900-2048-4096F-Q10S-RTC-E	Quad core, 1 GHz, no WiFi, 2GByte RAM, (Temp -20 to 85)
Option 6	TS-4900-2048-4096F-Q10S-RTC-WIFI-E	Quad core, 1 GHz, with WiFi, 2GByte RAM, (Temp -20 to 85)

Rev.A --> Rev.C Changes

Moved parts and copper away from mounting holes

Par interface pins were swapped
U4.K23 and U4.H21 = CN1 pins 65 and 99

Biased BOOT_MODE_1 high
and BOOT_MODE_0 low

5 LVDS diff pairs connected to CN2

CN2 pins 56, 58 and 60 go to different CPU DIO

Audio MCLK changed to CN2-54

CPU JTAG signals no longer connected to CN2
CPU JTAG signals go to Test Points

Rev.D changes:

Allow external PCIe 100 MHz CLK
No layout change needed - BOM change

Added 4mm keep out around iMX6
top layer for new heat sink

Changed to 153-ball eMMC

Added EIM Byte strobe to CN1 pin 22
FPGA ball "P4" controls SD power

Allow FPGA to be 1-time programmed
For Windows CE applications
Requires PU on FPGA_SPI_CS#
Also connect to CN2 pin 34

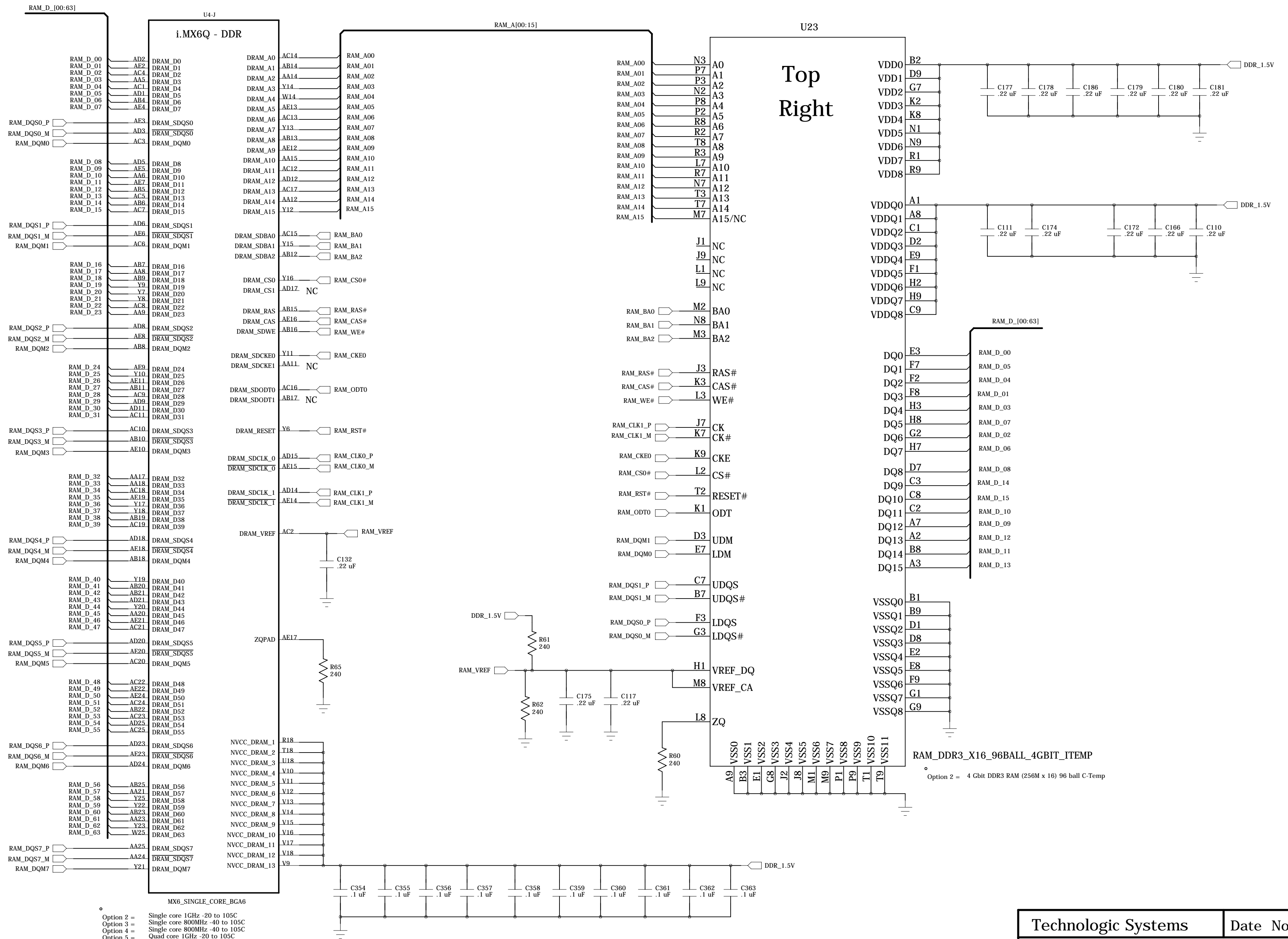
Ball "L6" on CPU is GND, to indicate Rev.D

JTAG ball "H6" is GND

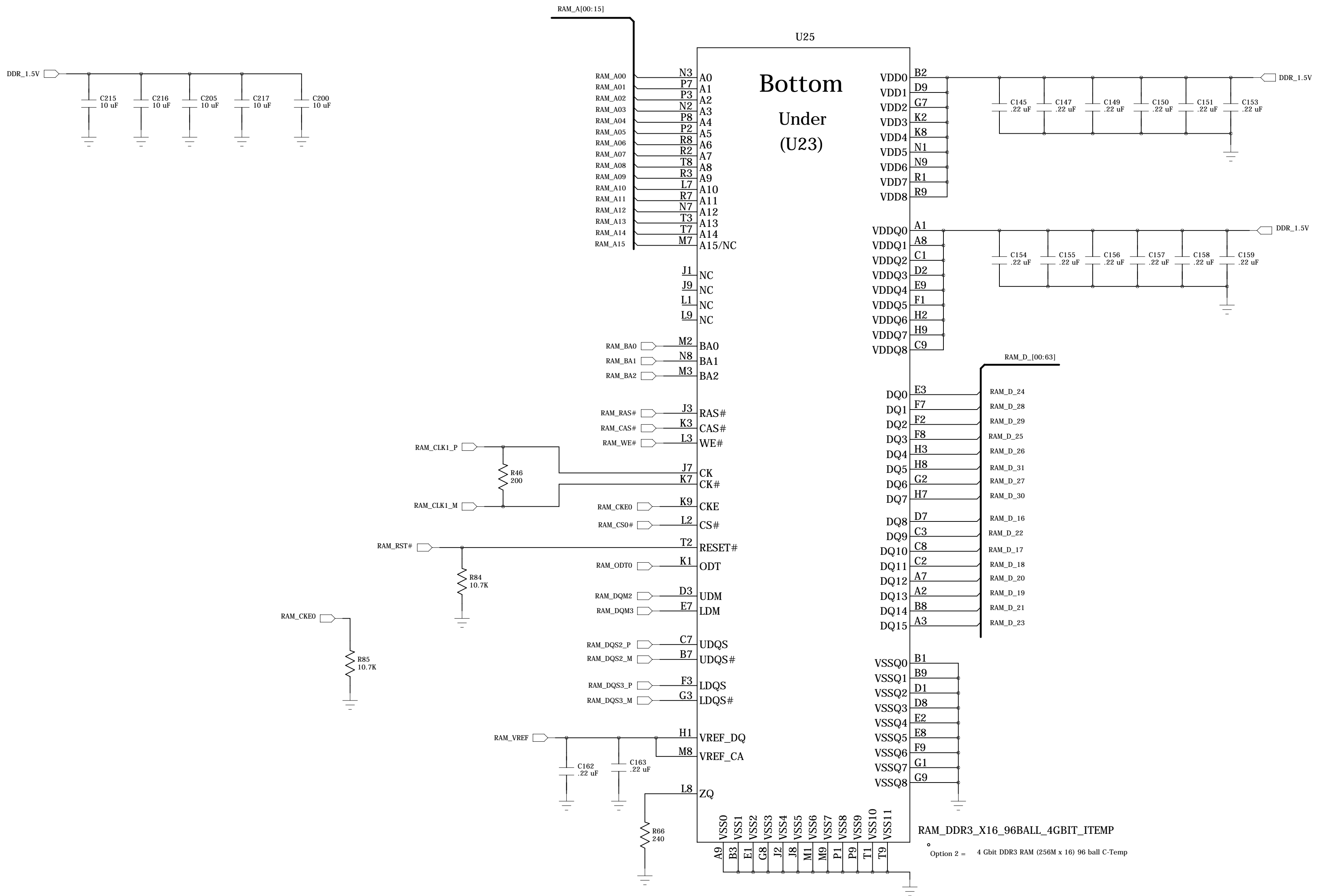
CN1 pin 12 is wrong, but can't change it

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512 MB per RAM Chip

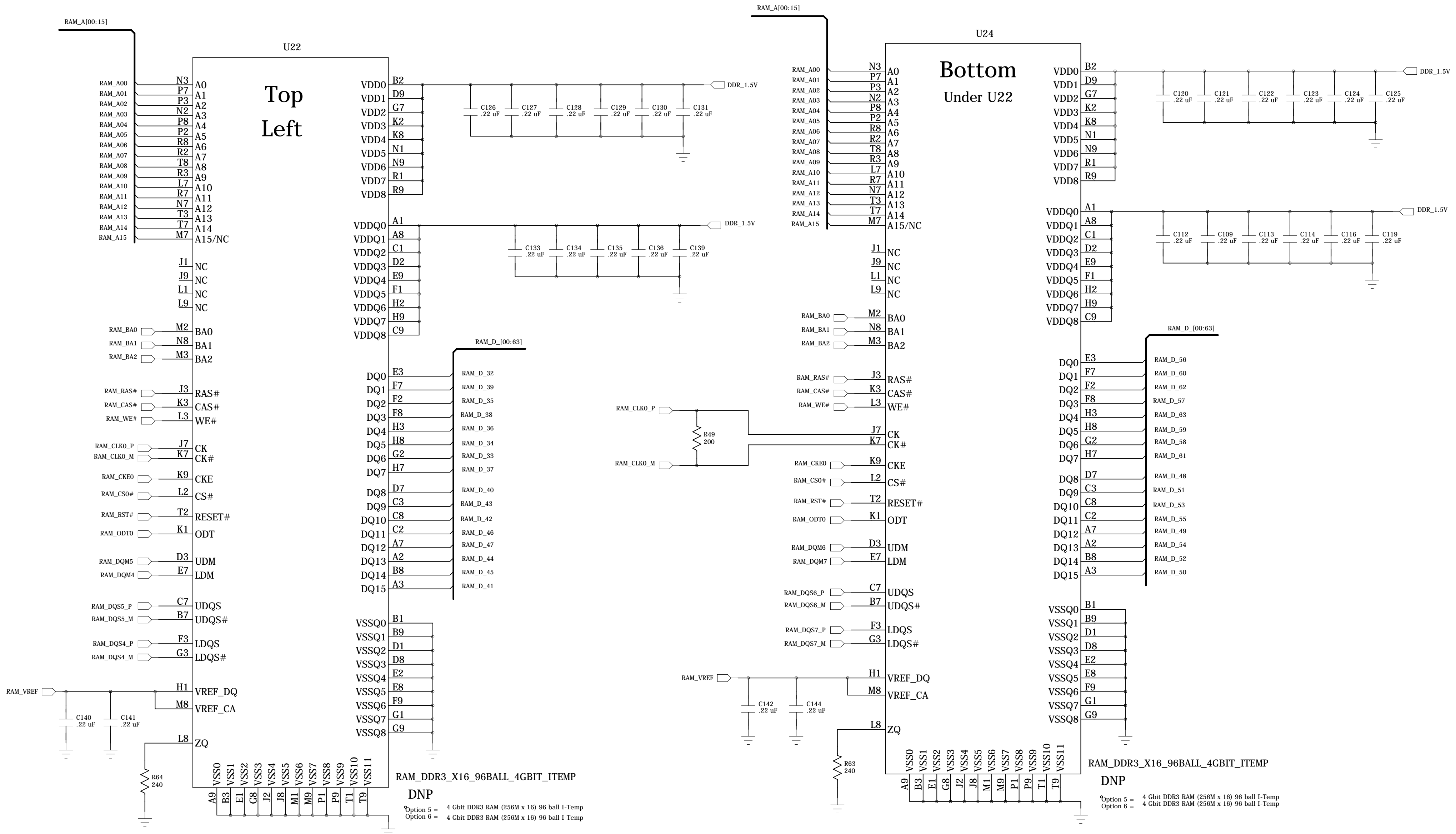


- MX6_SINGLE_CORE_BGA6
- Option 2 = Single core 1GHz -20 to 105C
 - Option 3 = Single core 800MHz -40 to 105C
 - Option 4 = Single core 800MHz -40 to 105C
 - Option 5 = Quad core 1GHz -20 to 105C
 - Option 6 = Quad core 1GHz -20 to 105C

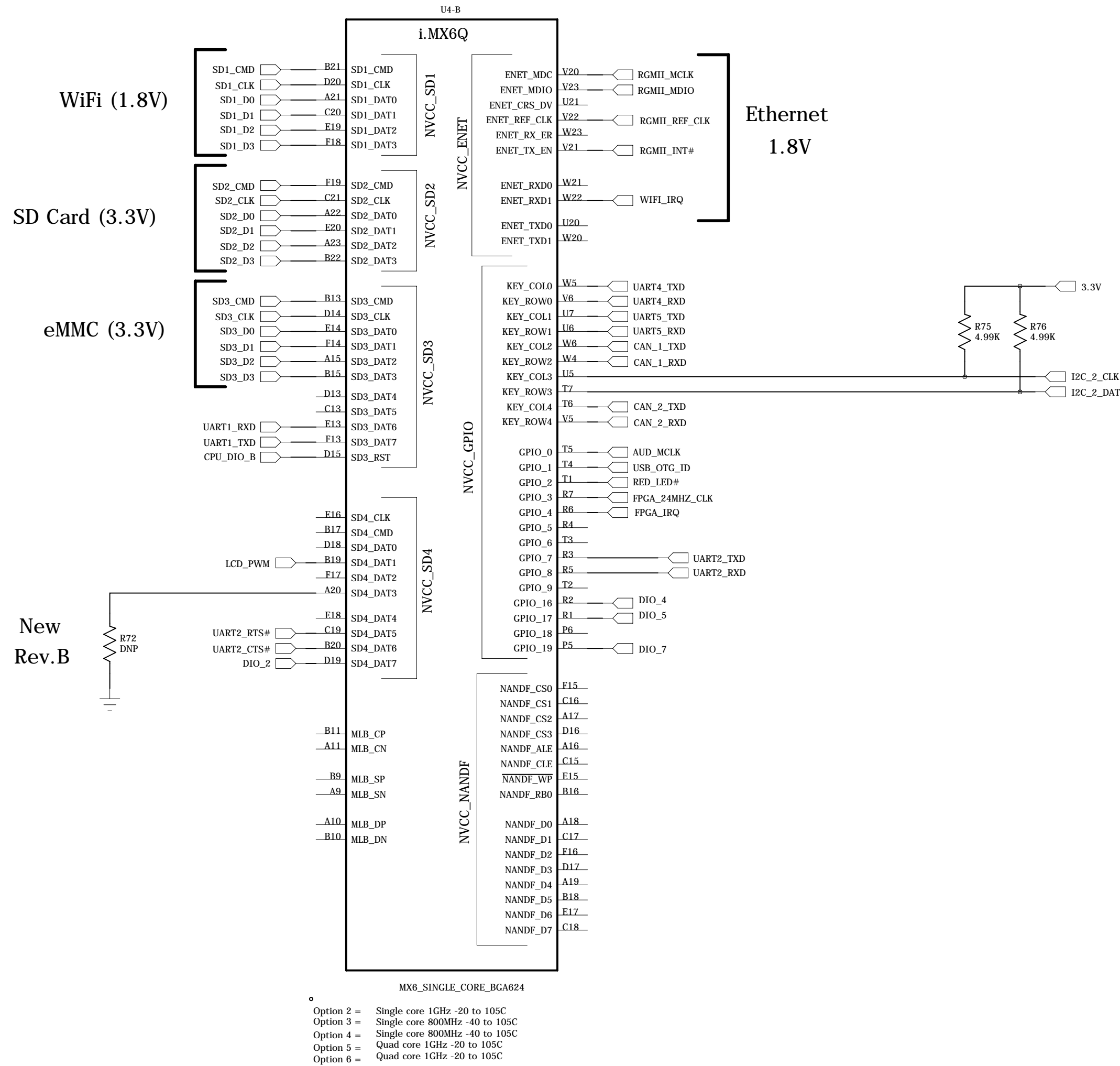


RAM Data bits 32-63

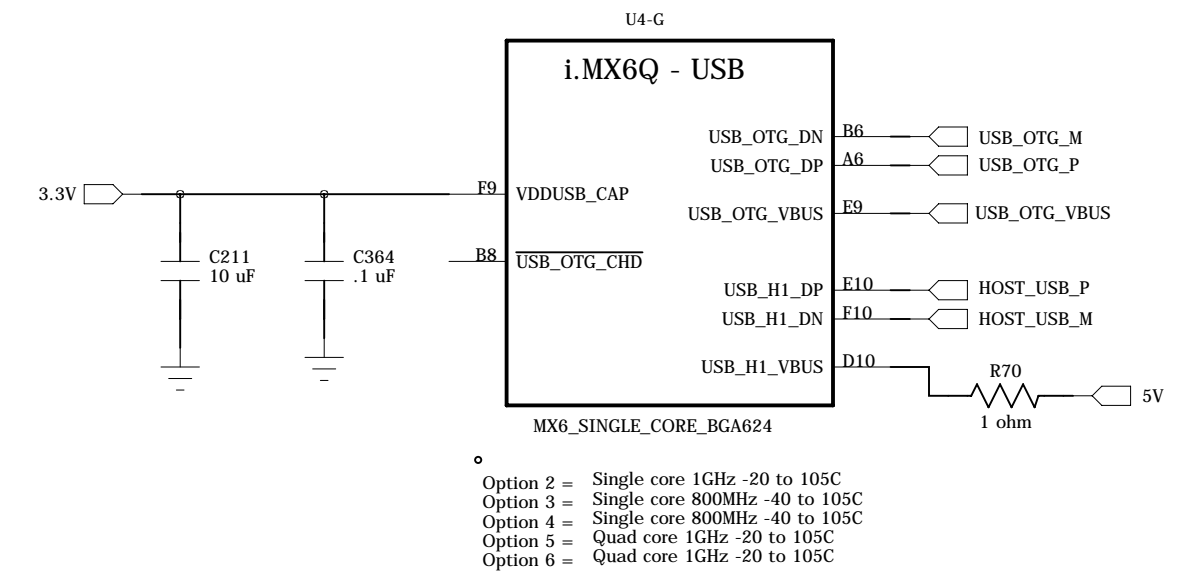
Not populated for Single Core CPU



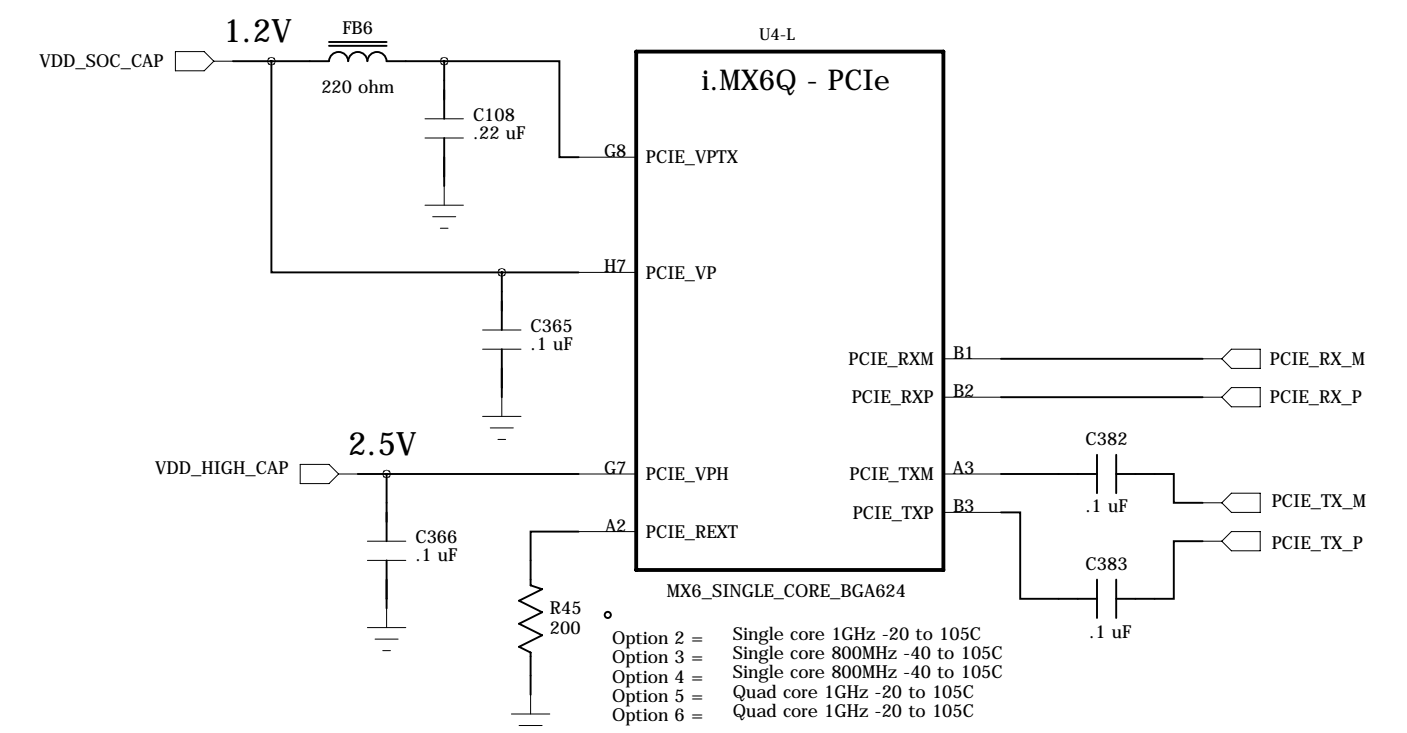
SD, GPIO, NAND



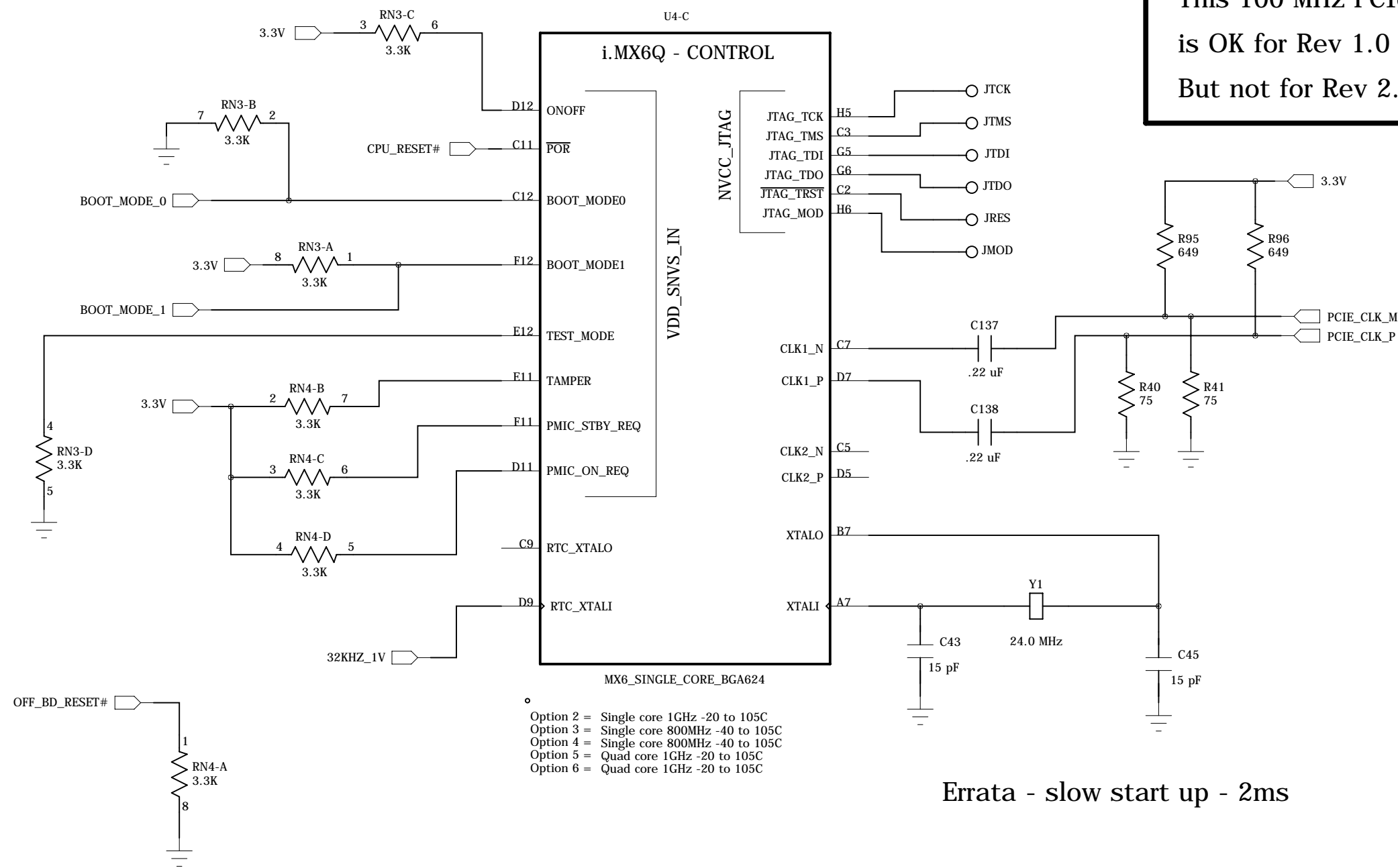
USB



PCIe

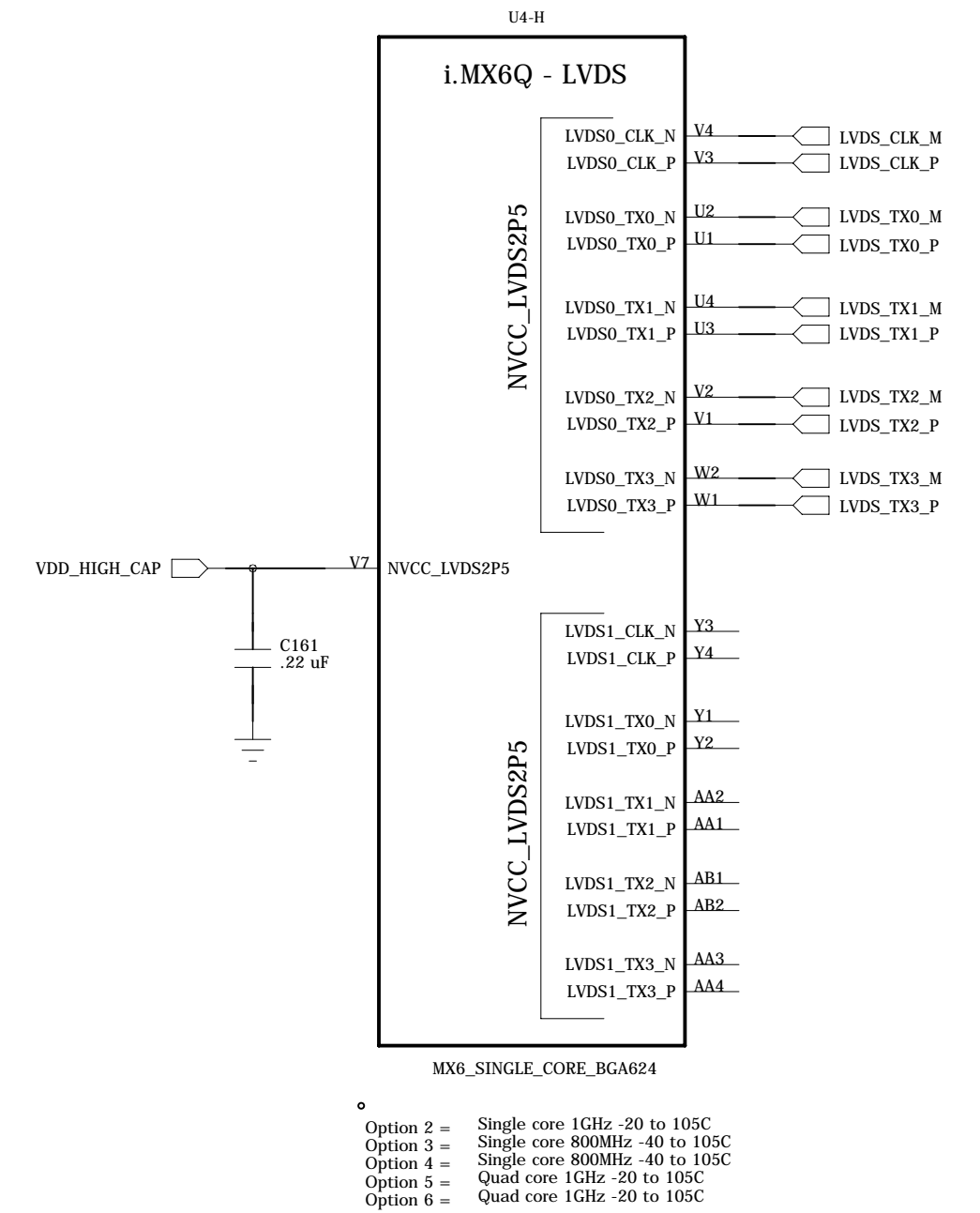


Control

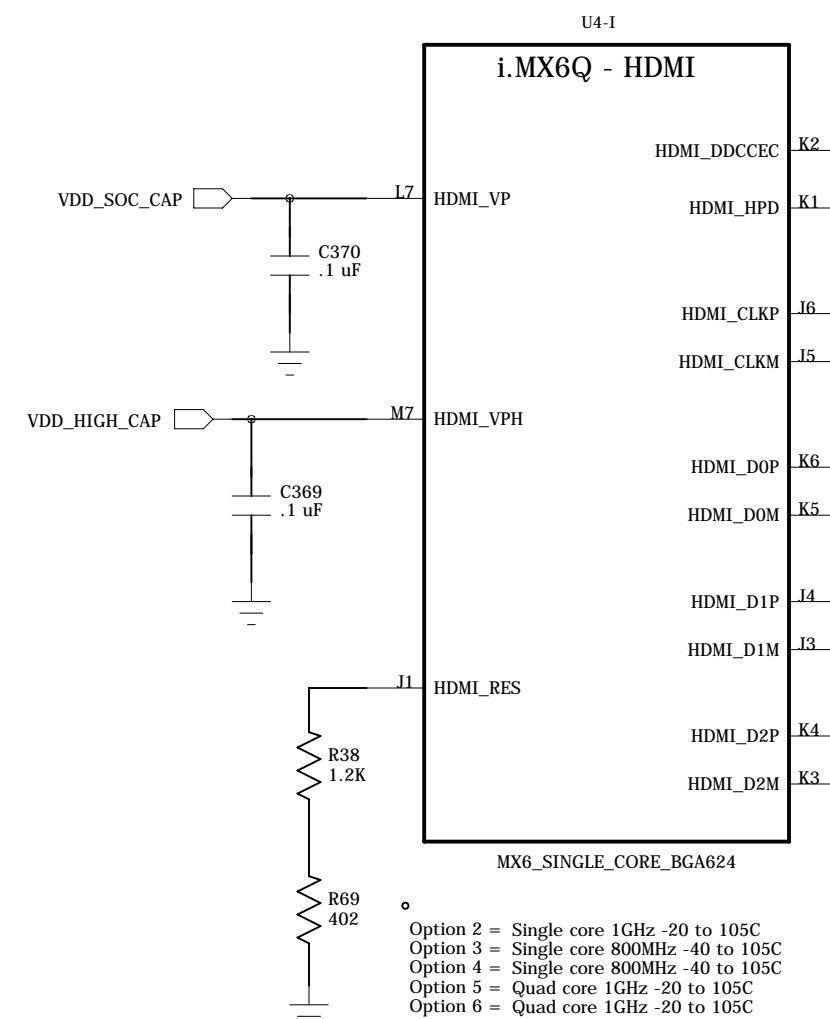


Errata - slow start up - 2ms

LVDS

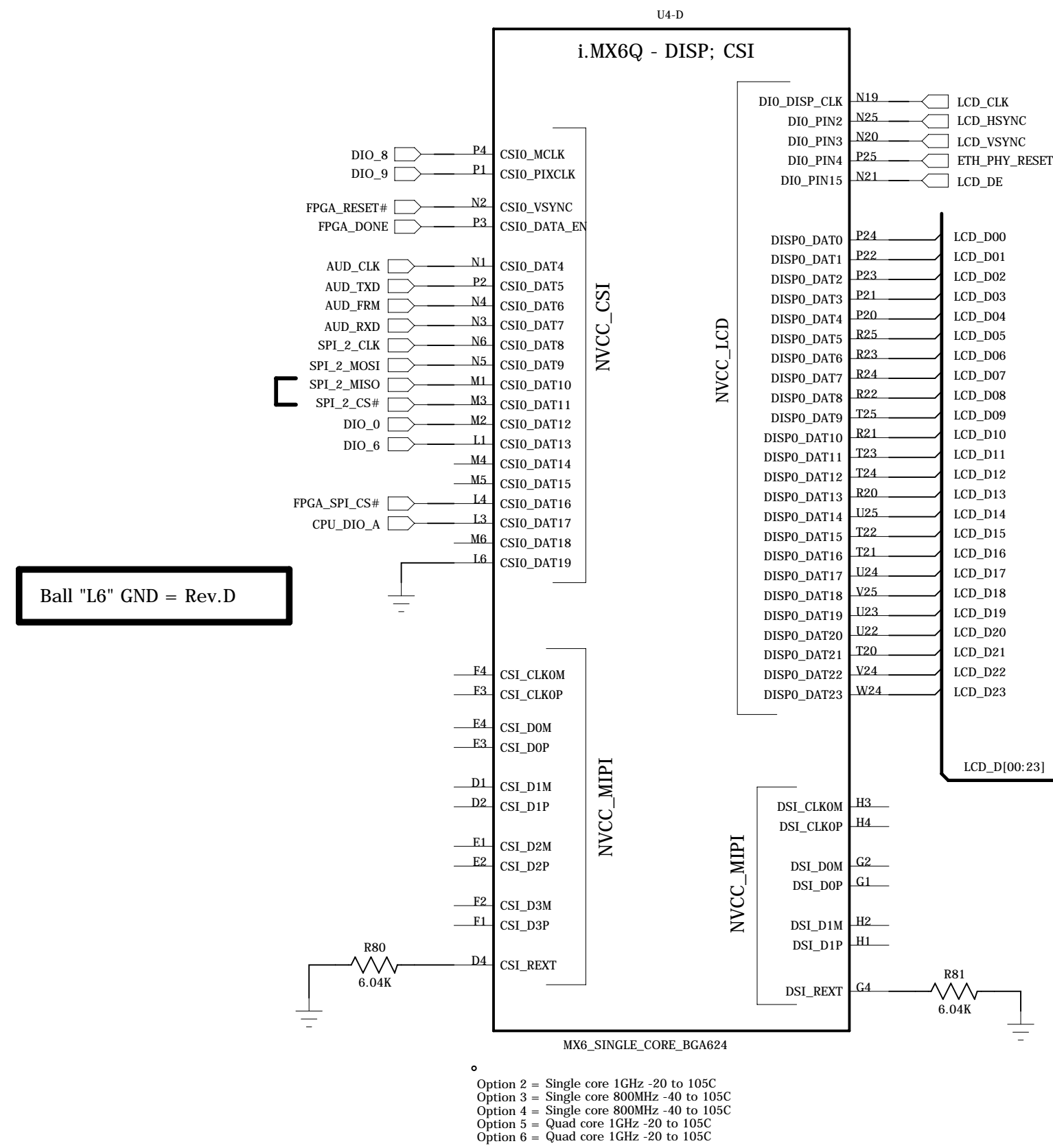


HDMI

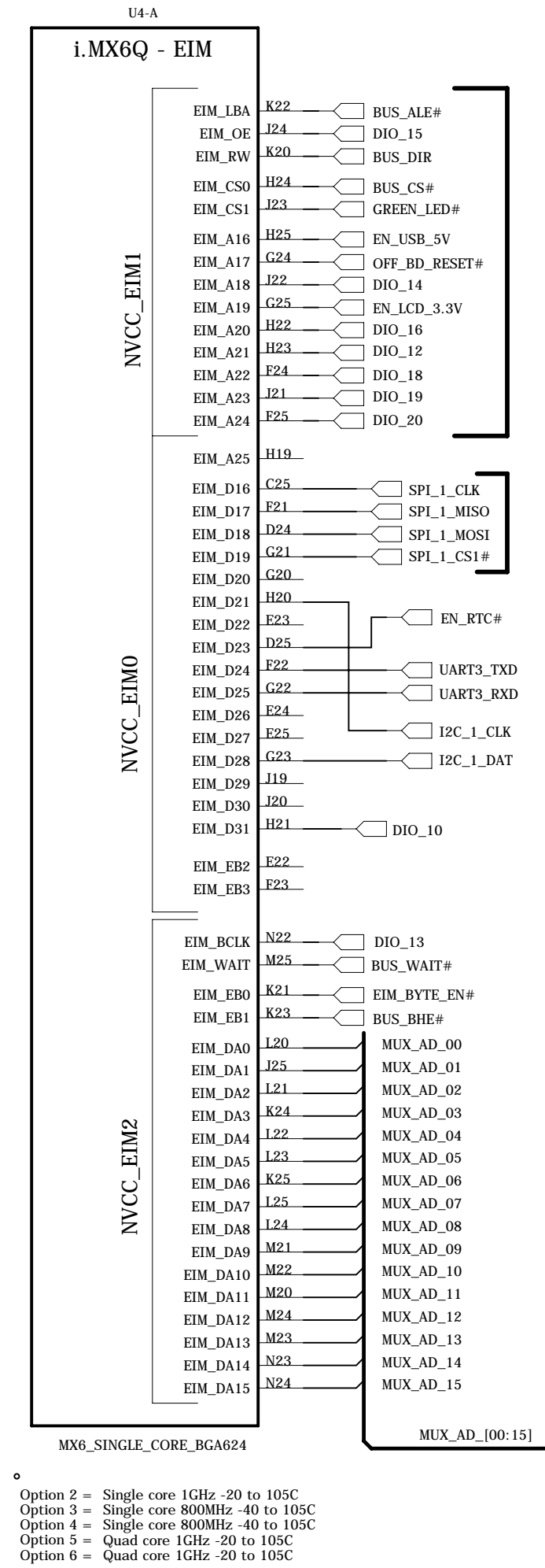


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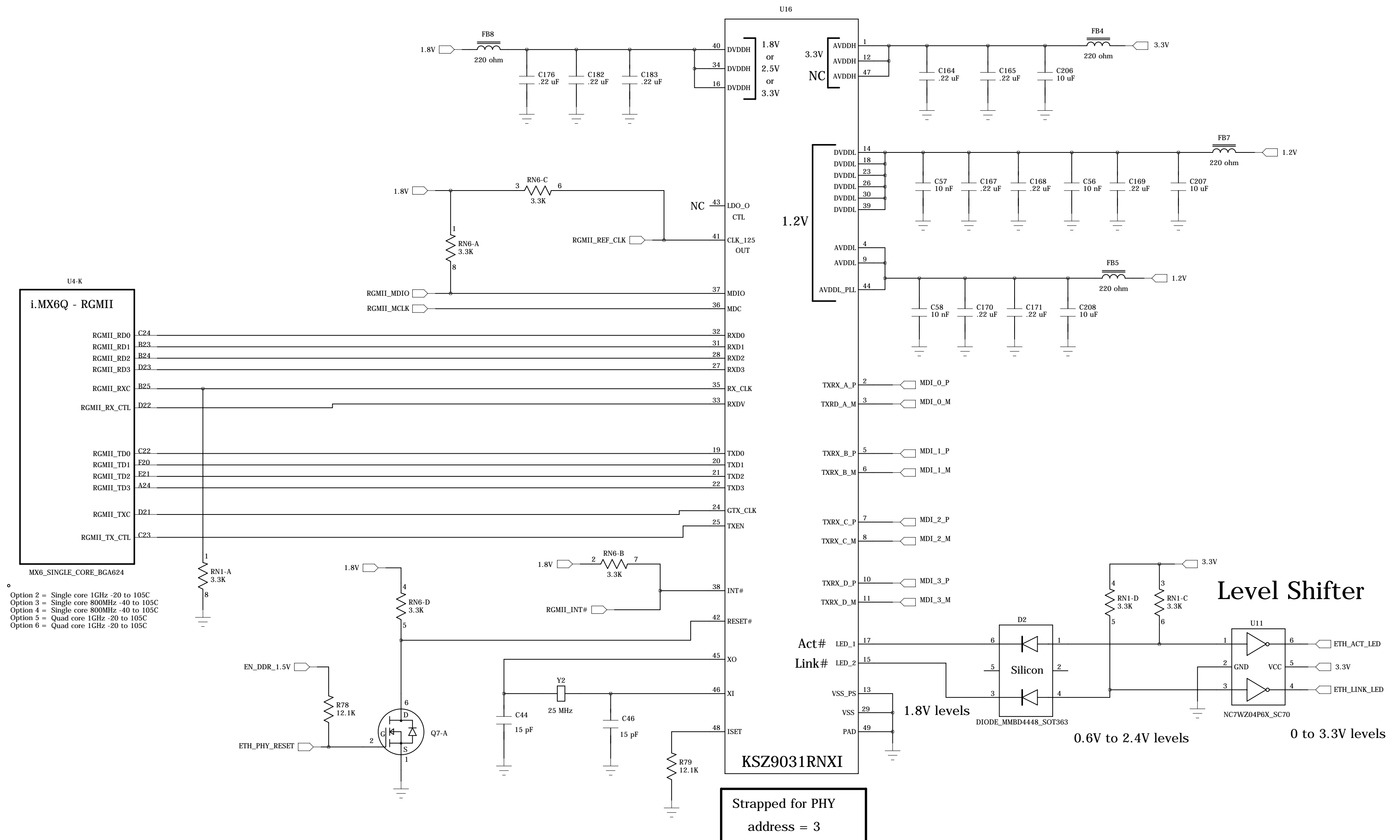
LCD



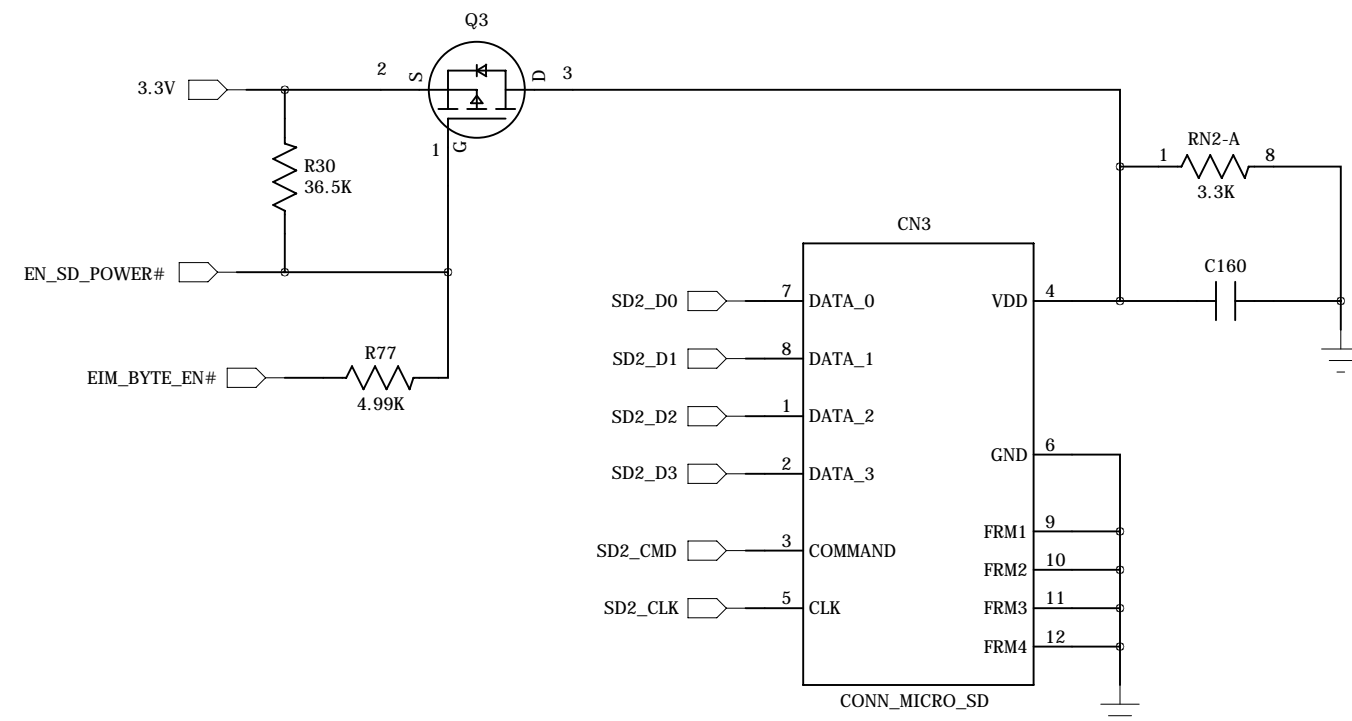
EIM



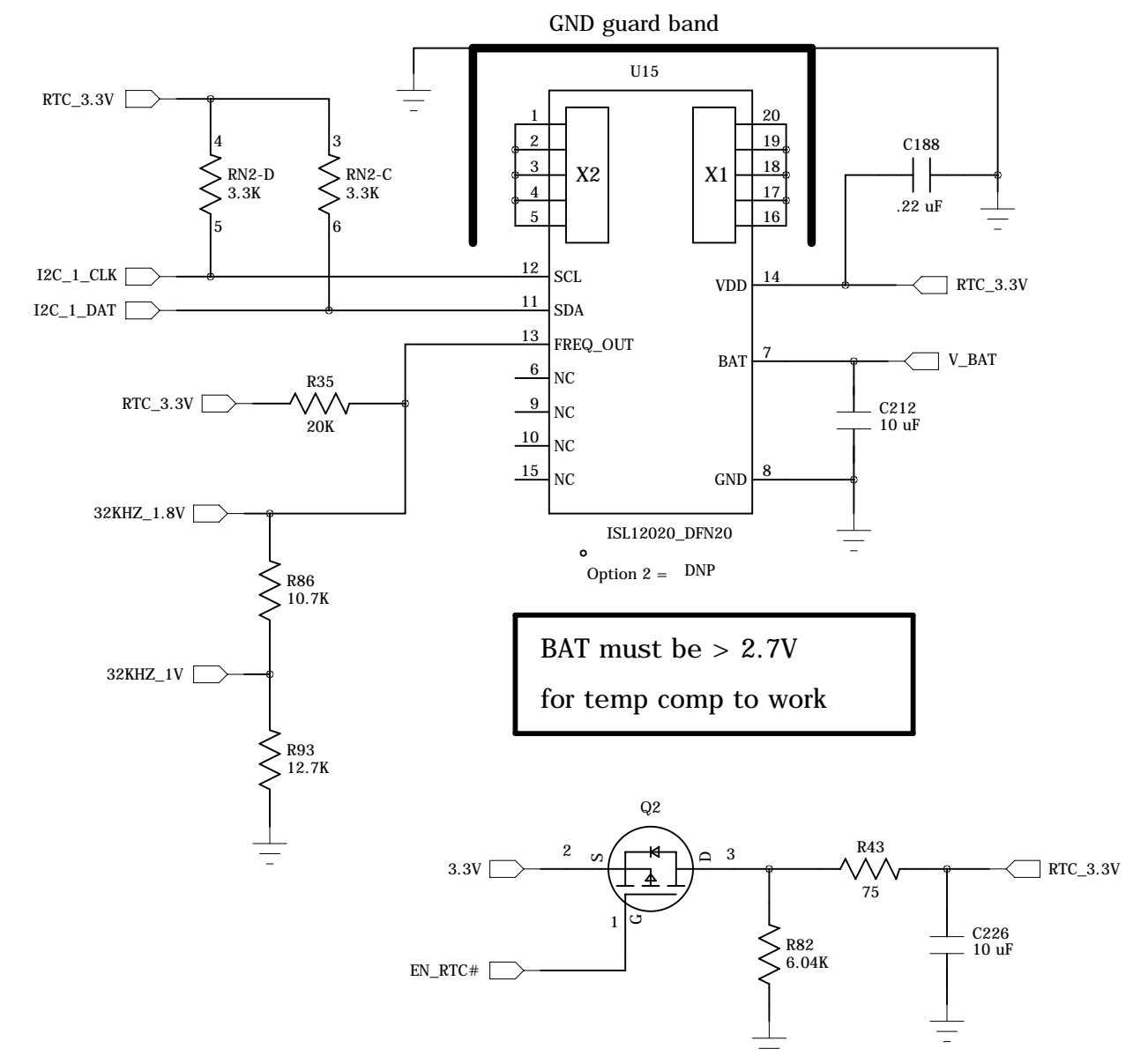
10/100/1000 Ethernet PHY



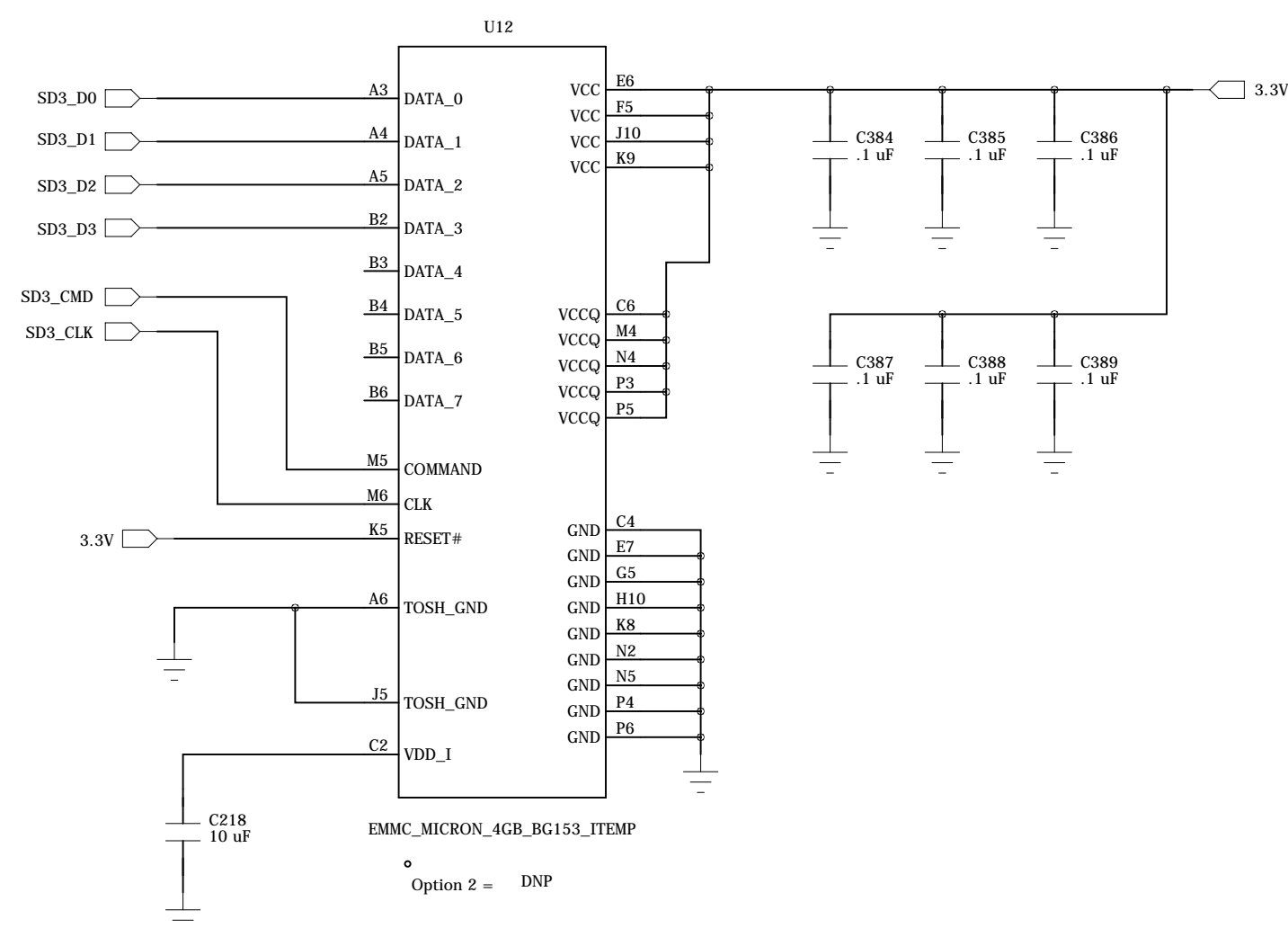
Micro SD Card Socket



RTC and Temp. Sensor

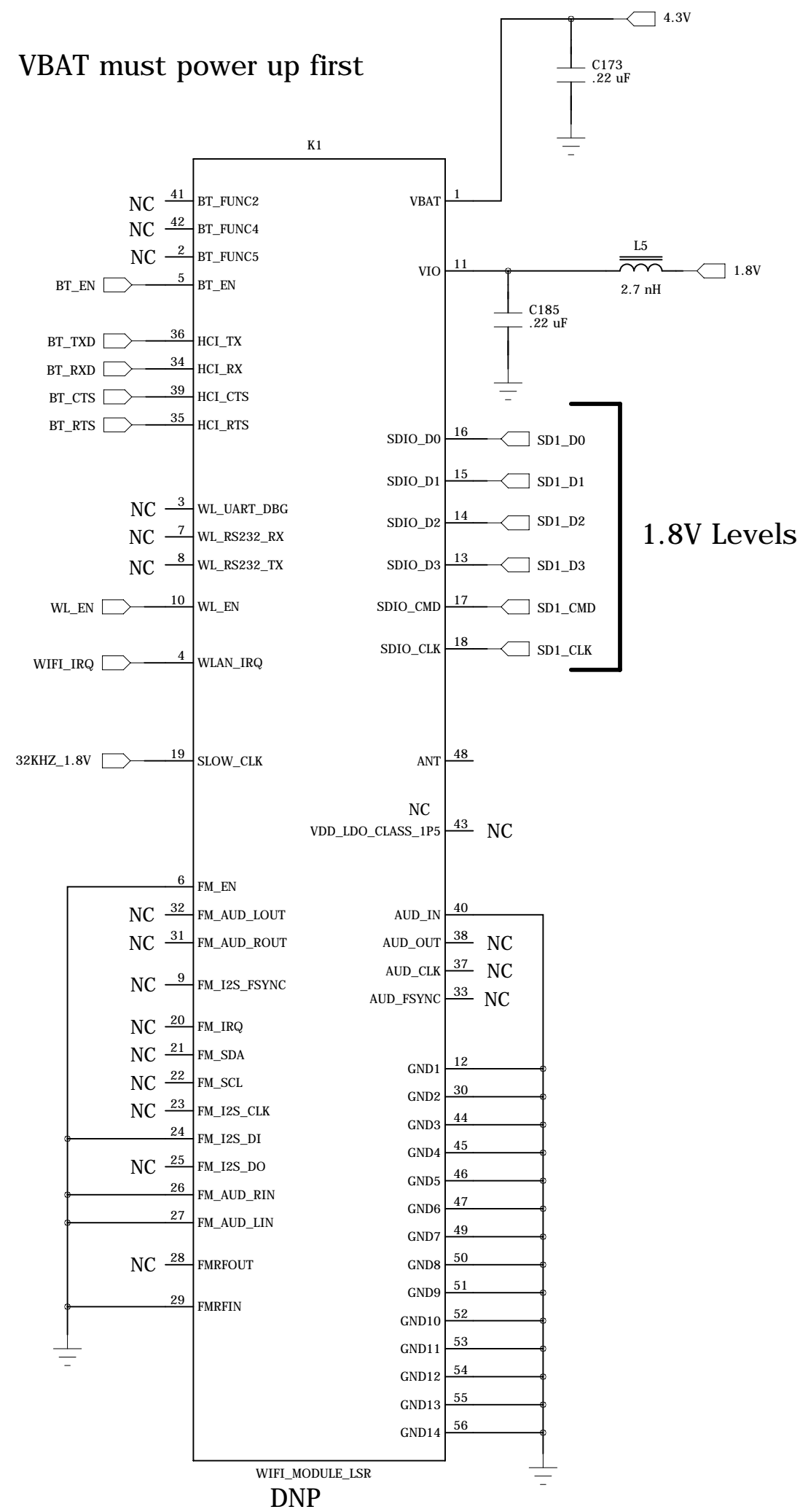


eMMC 4GB



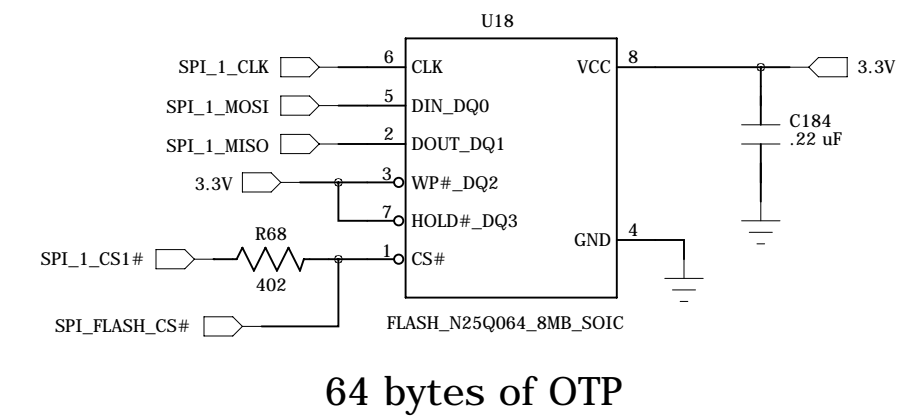
EN_RTC# has weak PU on CPU DIO
At system power up, FET is off

WiFi Radio

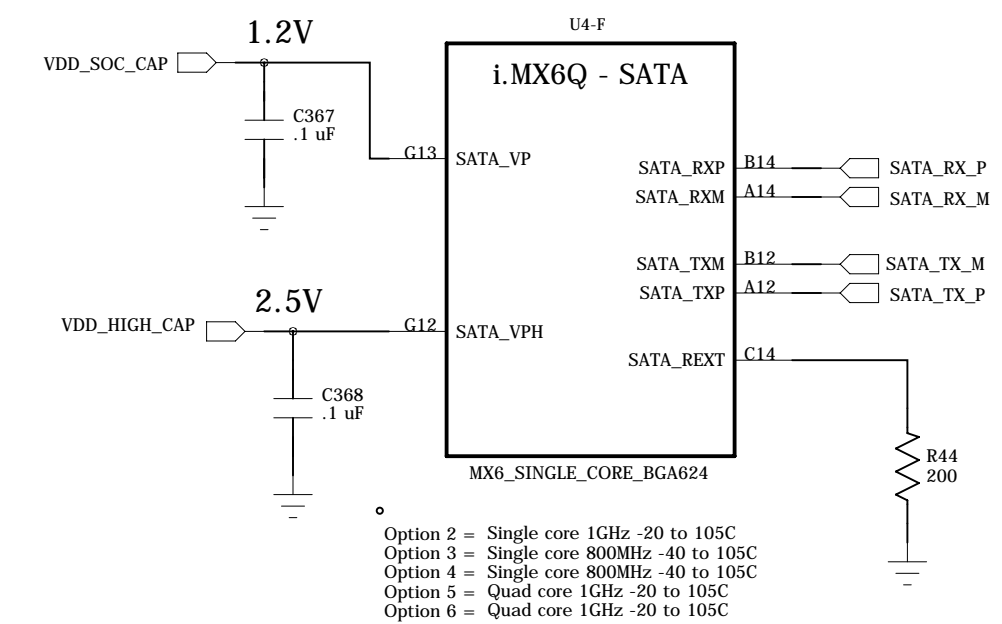


Option 4 = LS Research TIWI-BLE SDIO WiFi 802.11BGN and Bluetooth 4.0
Option 6 = LS Research TIWI-BLE SDIO WiFi 802.11BGN and Bluetooth 4.0

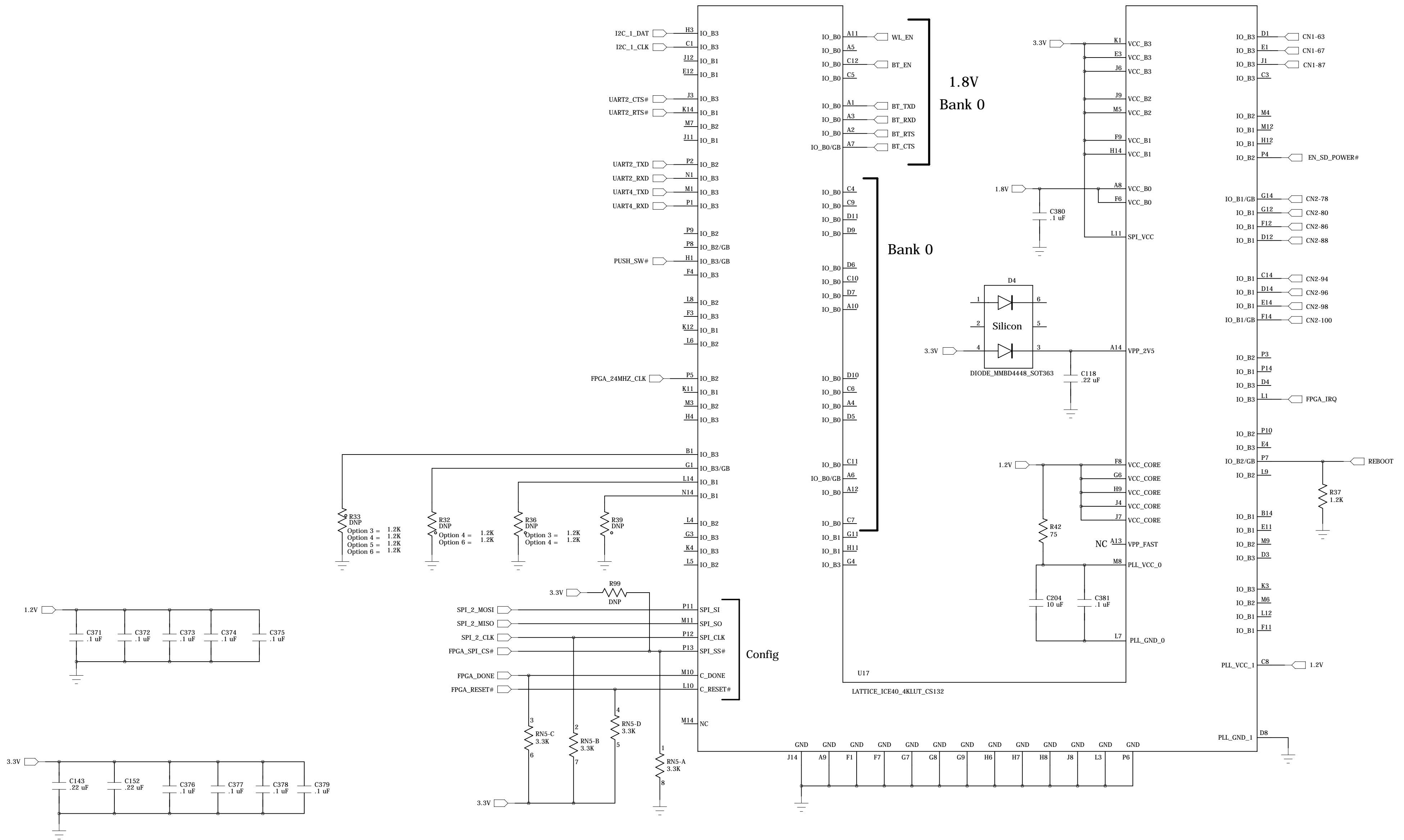
SPI Boot Flash



SATA



iCE40 FPGA



Two 100-pin Off-board Connectors

"5V" pins supply all power to the module
Apply 4.5V to 5.5V to these pins

OFF_BD_RESET# is an Output
used to reset all peripherals

EXT_RESET# is an Input
used to reboot the CPU

Do not drive active high
(use open drain)

⚠ All signals driving DIO on CN1 & CN2 must be powered by the 3.3V on CN2, or remain at 0V until the CN2 3.3V rail is > 3.0V

3.3V rail can supply up to 700 mA to base board

Maximum off-board load on AN_1.8V is 10 mA

CN1-Pin 63 = UART4 TXEN
CN1-Pin 67 = UART0 TXEN

Rev.C Change
CN1-65 (DIO_10) and CN1-99 were swapped on CPU

If Bus is not needed, all Bus signals can be changed to DIO

LVDS pairs are length matched

PCIe Diff Pairs have been Polarity swapped

SATA can NOT have polarity swapped

SATA and PCIe Diff pairs do NOT have to be length matched

Rev.C Change
CN2 pins 56, 58, and 60 are different iMX6 balls on Rev.C than on Rev.A

