

Standard Options

XOPP1
NC
ASSEMBLY_OPTIONS

NC
1
PCB_99

Option 1 TS-7120-PROTO NXP i.MX6UL 695MHz ARM A7, Prototype, (-40 to 85C)

Optional Components/Features Summary

OBD-II Option:

Requires parts on Page 30 of schematic

ADD: CN9, U57, U60

REMOVE: CN17

Web Schematic: Some proprietary information has been withheld.

Technologic Systems	Date	Aug. 22, 2018
Title: TS-7120		
Rev: P1	Designer	Sheet 1 of 34

6UL Serial Ports

All 4 RS-232 levels

Mikro Bus UART

FPGA Serial Ports

Nimbelink with Flow Control

Two 485 ports with TX_EN

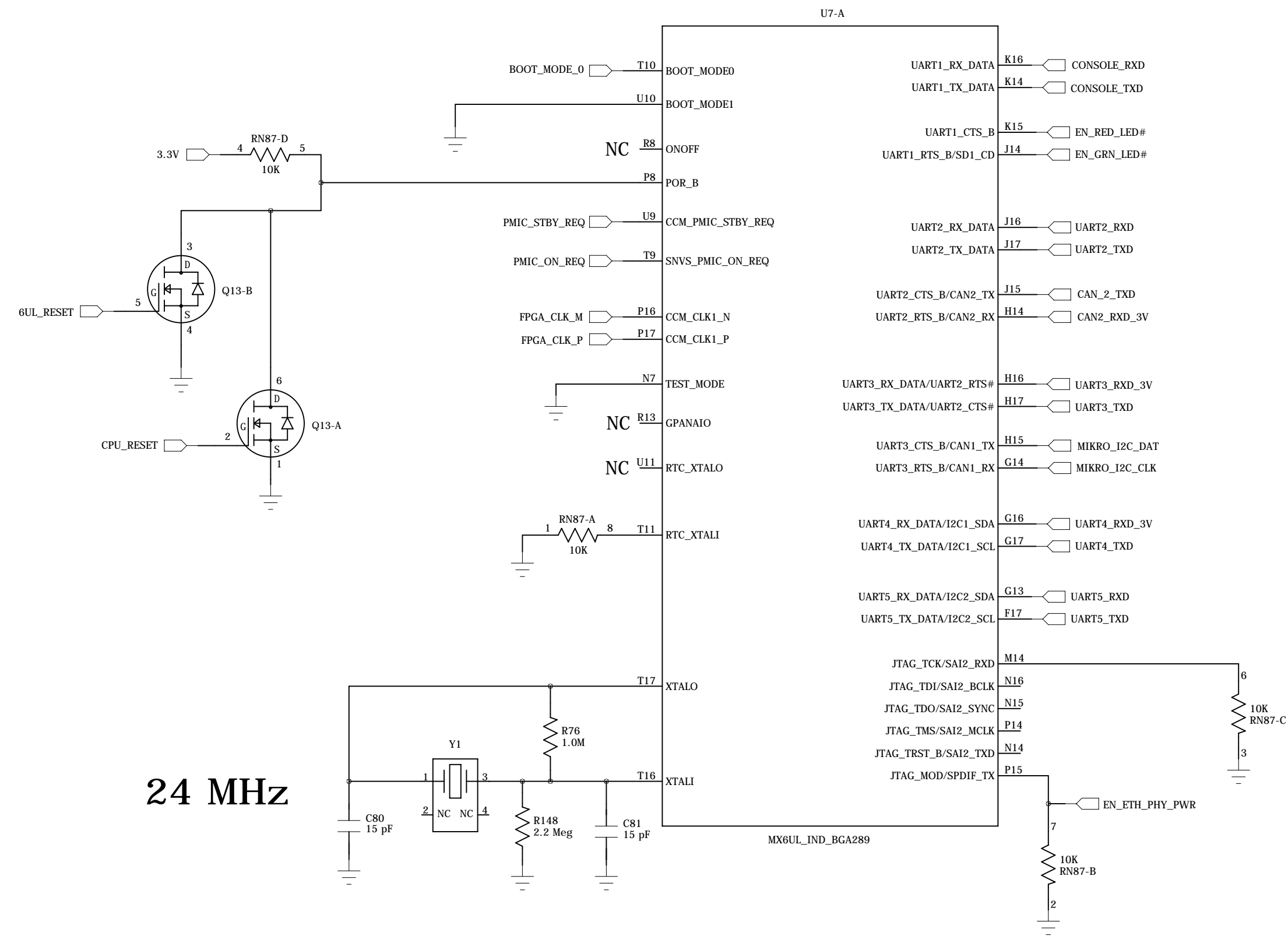
DMX port - bastard format

GPS UART

OBD-II UART

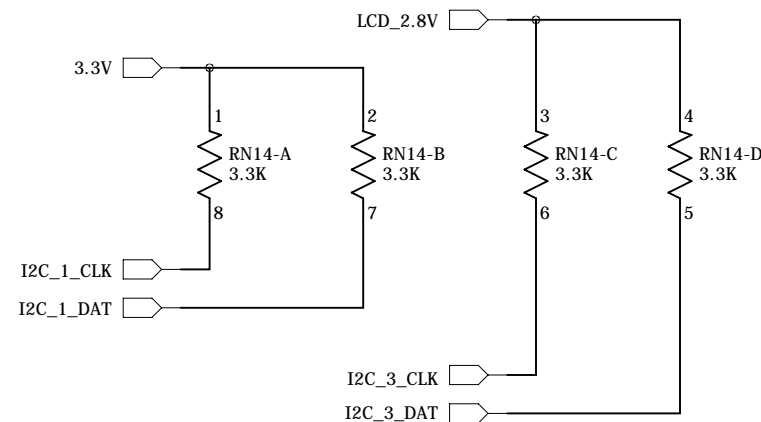
Technologic Systems	Date	Aug. 22, 2018
Title: TS-7120		
Rev: P1	Designer	Sheet 2 of 34

6UL UART and Control

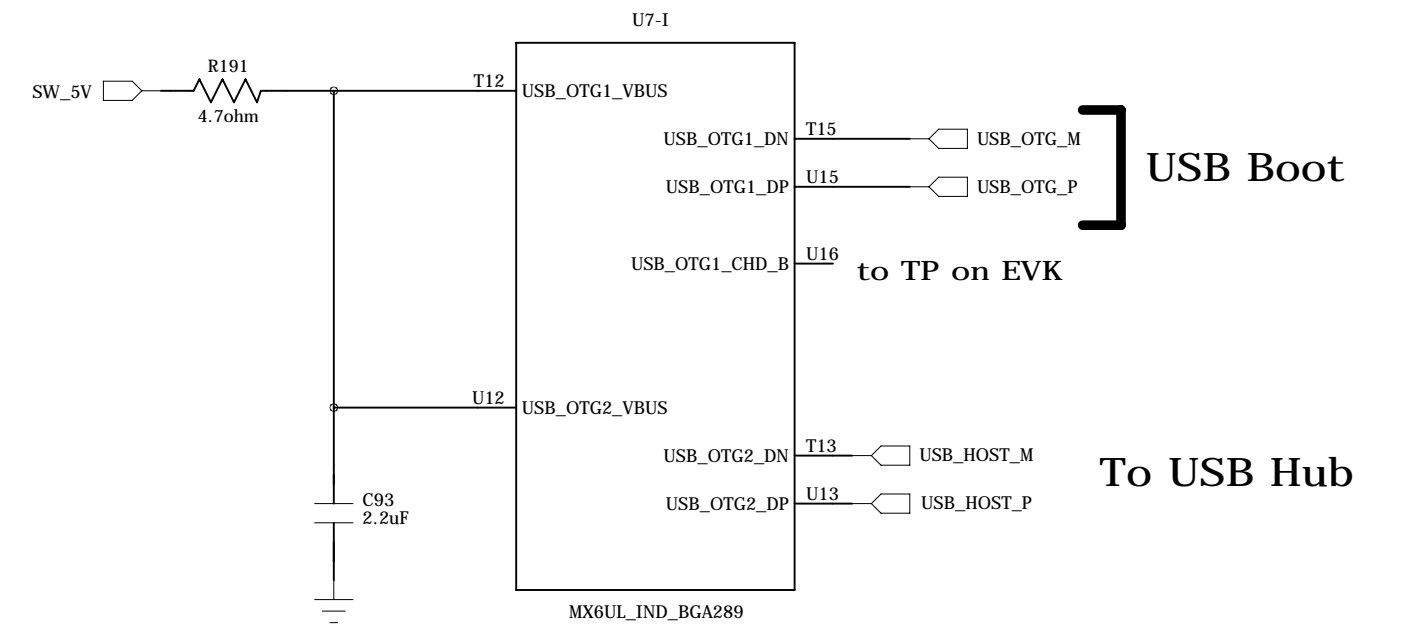


24 MHz

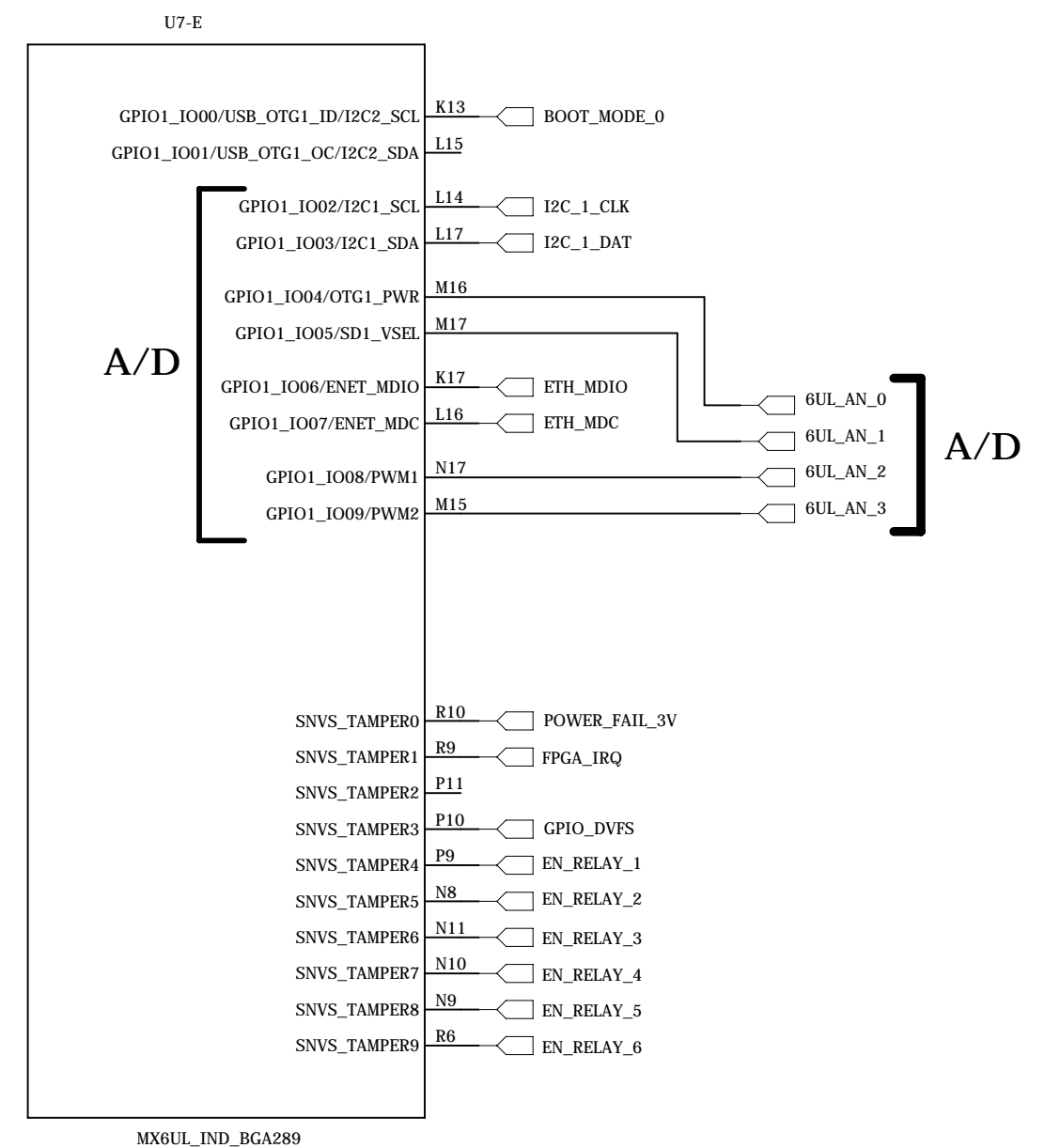
I2C PU Res.



6UL USB Ports

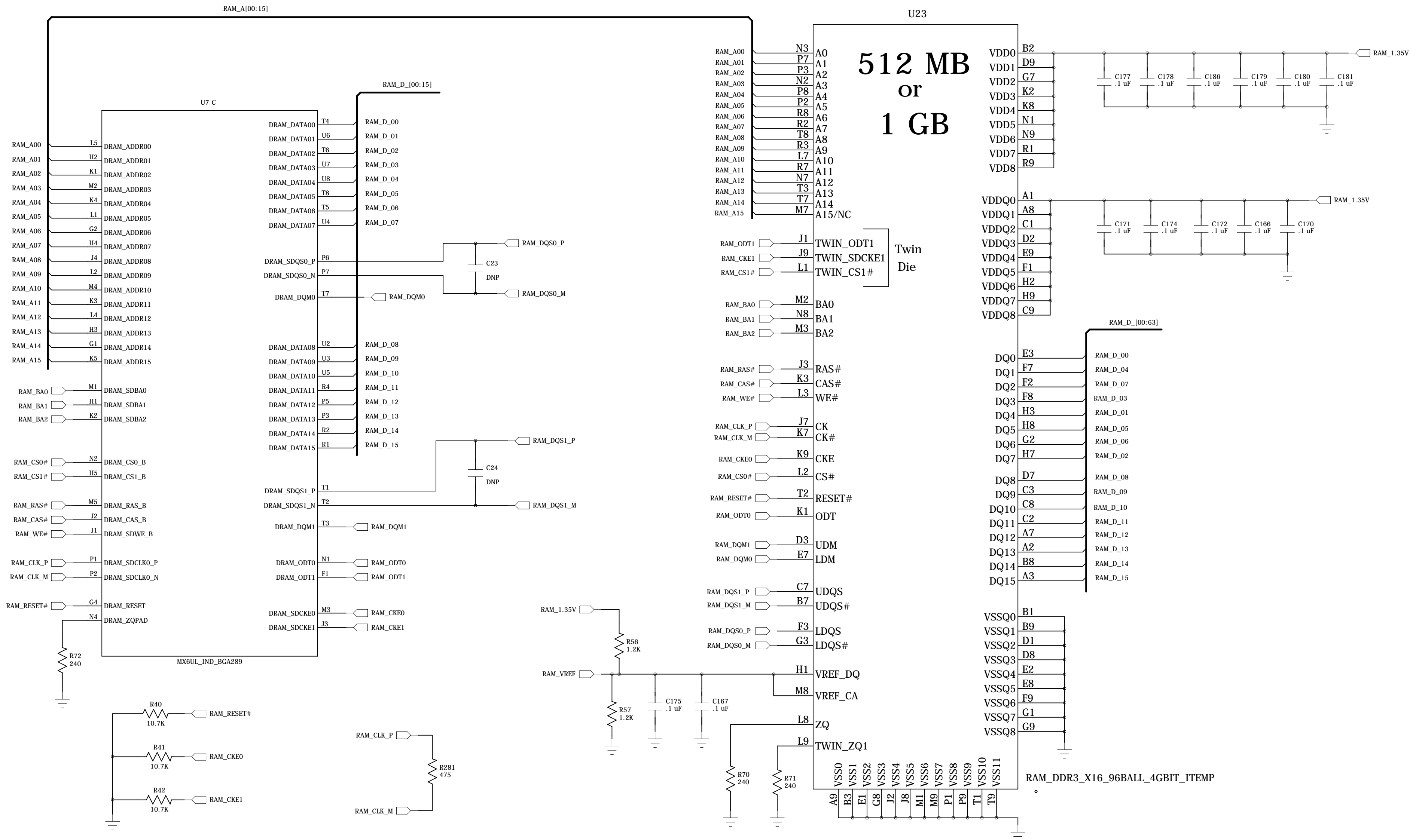


6UL DIO

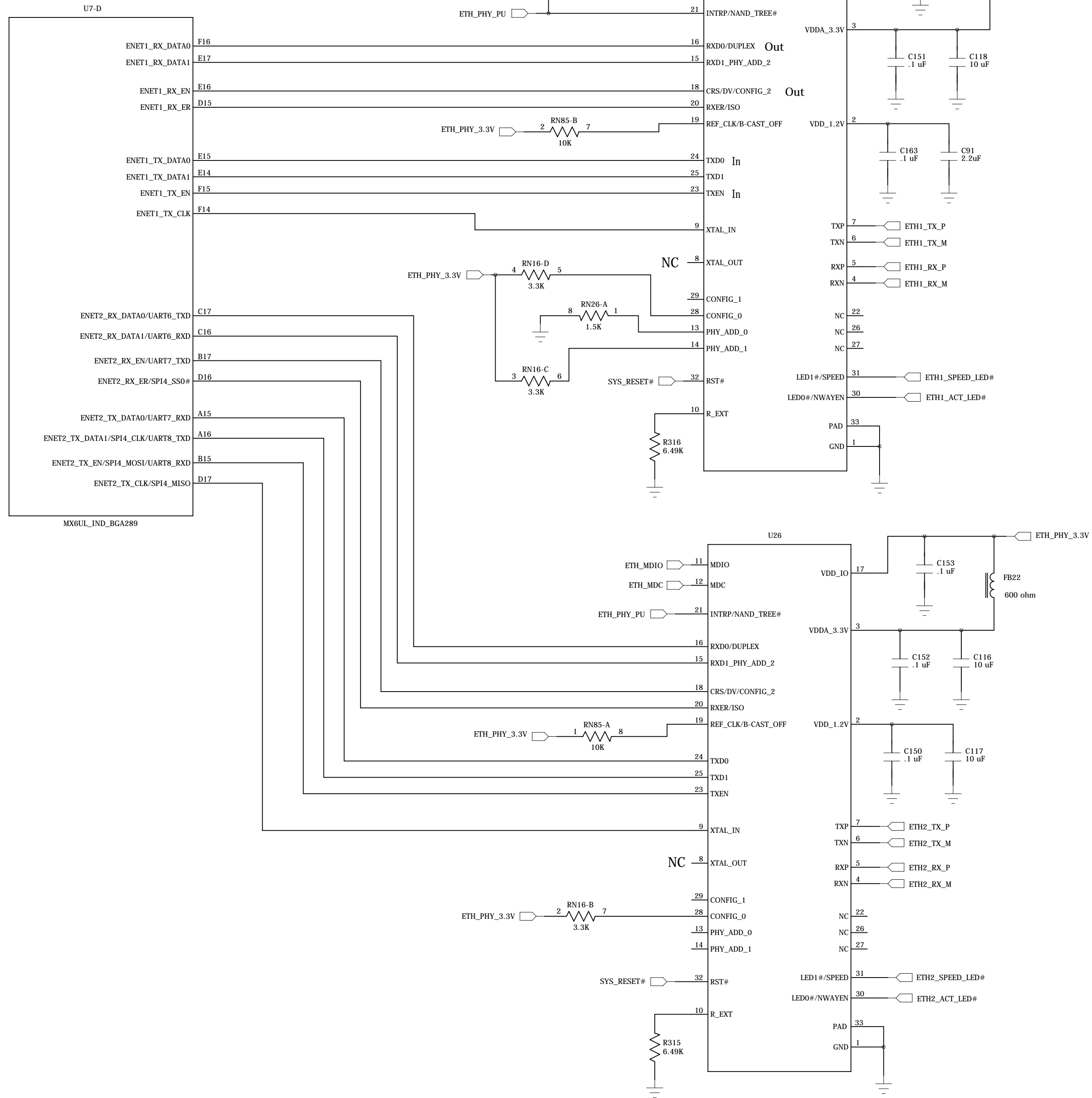


6UL RAM Interface

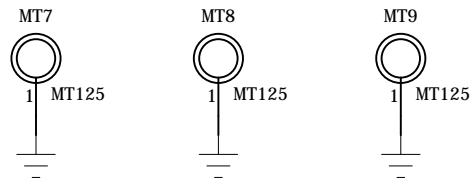
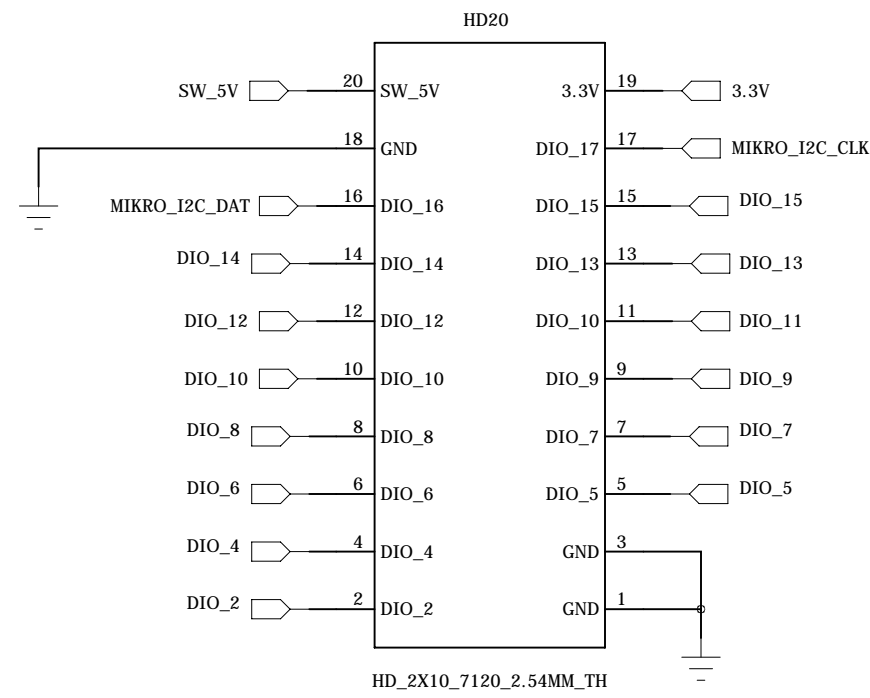
DDR3 RAM



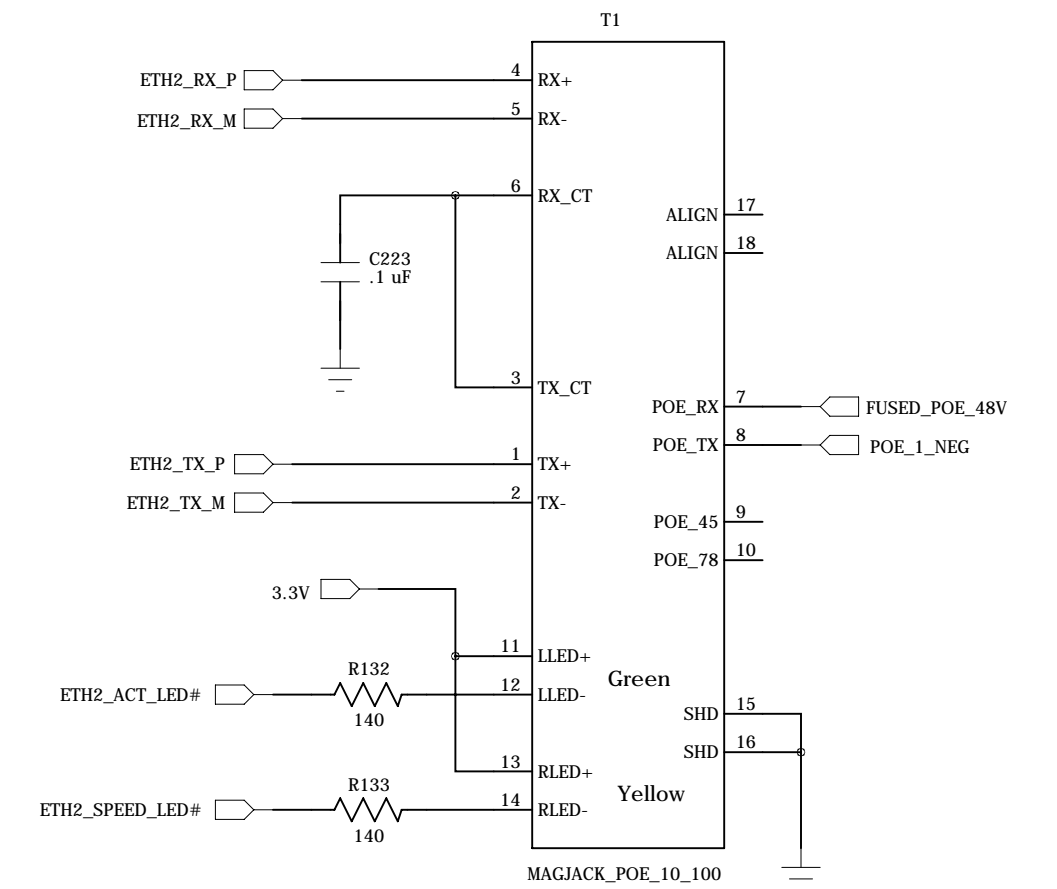
6UL Ethernet



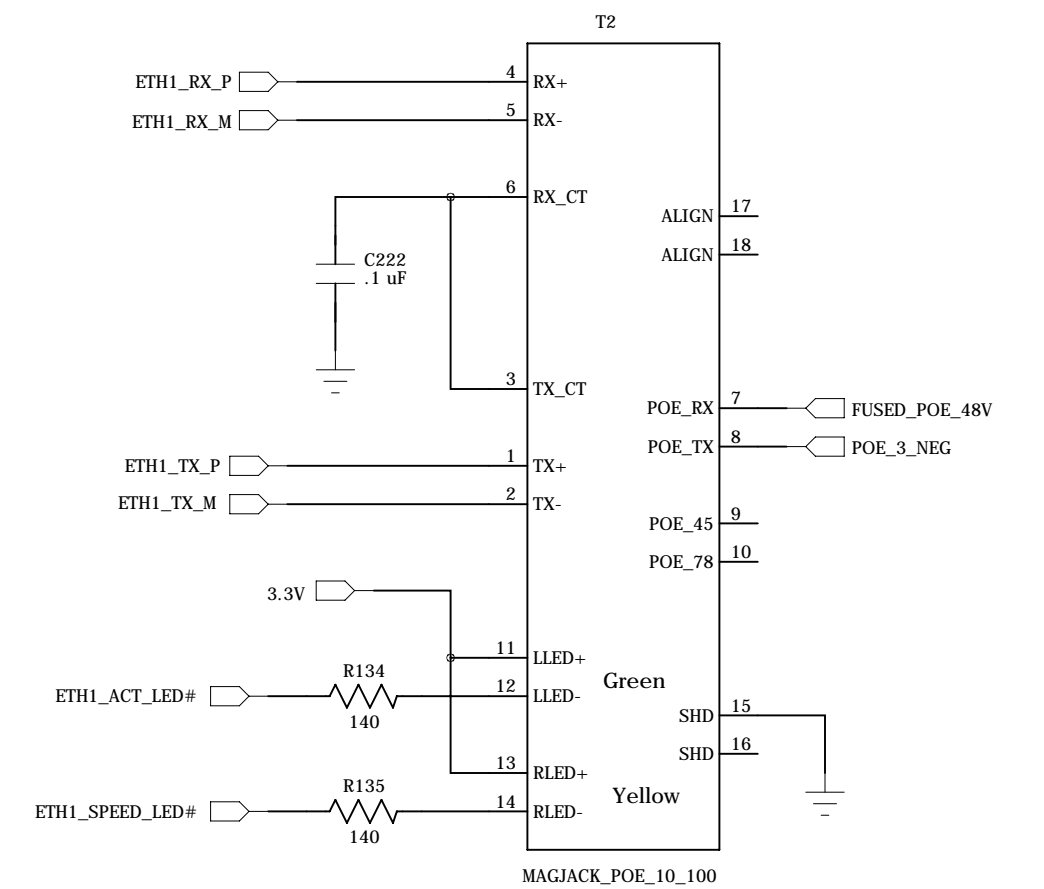
Daughter Card Interface



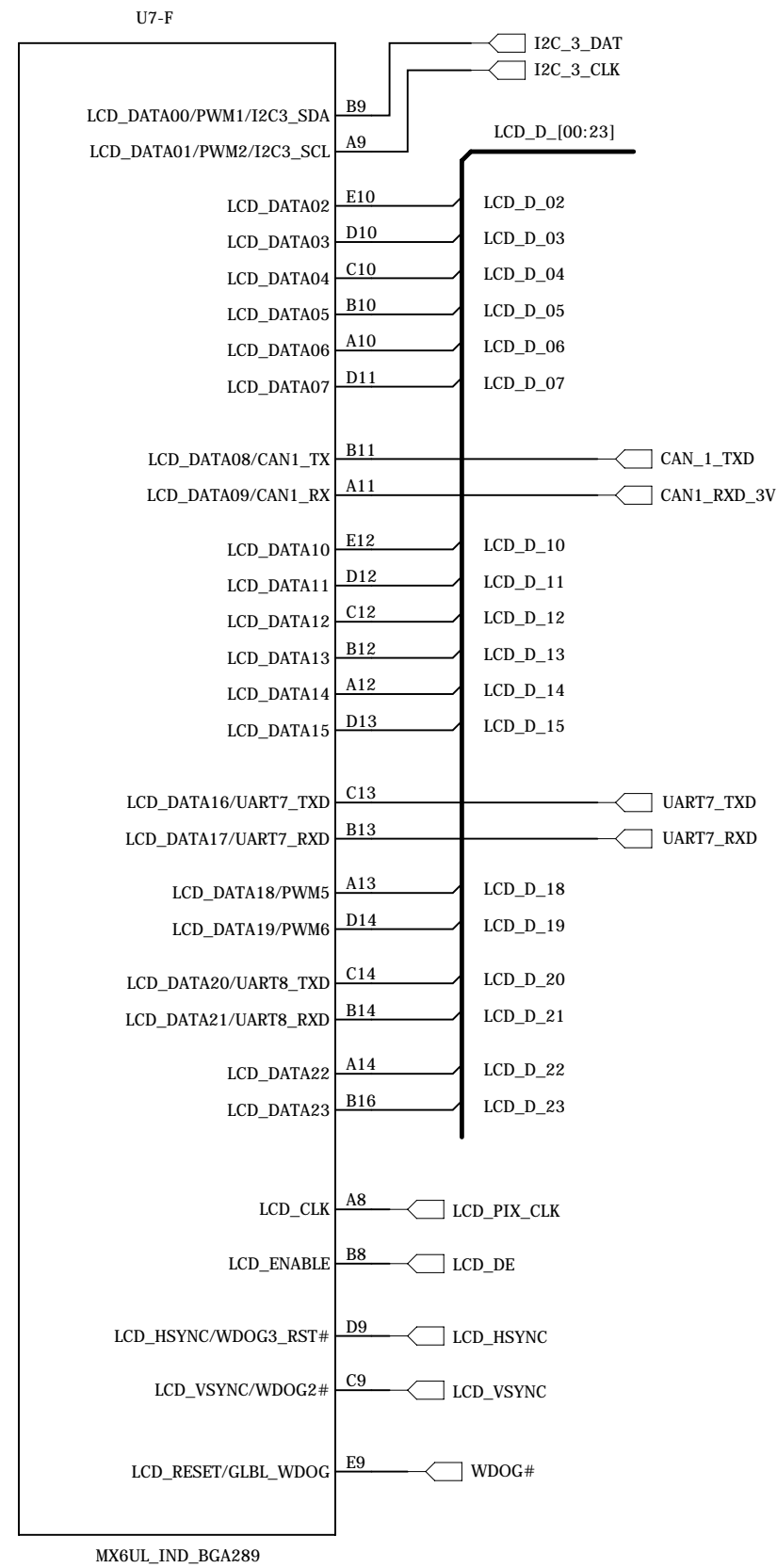
10/100 MagJack



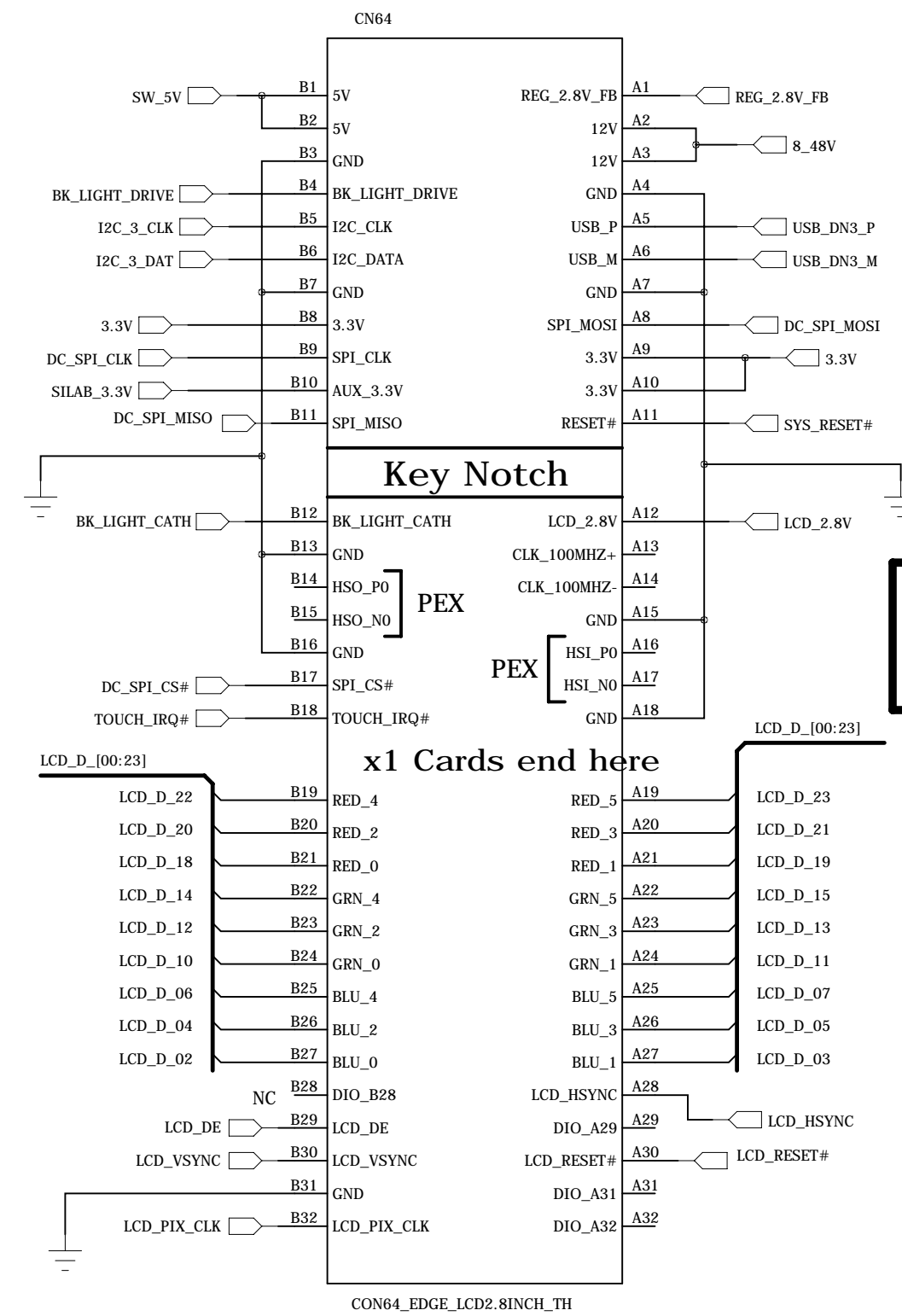
10/100 MagJack



6UL LCD



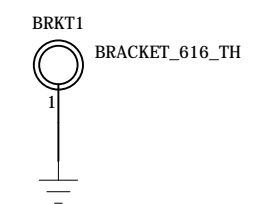
Daughter Card Conn.



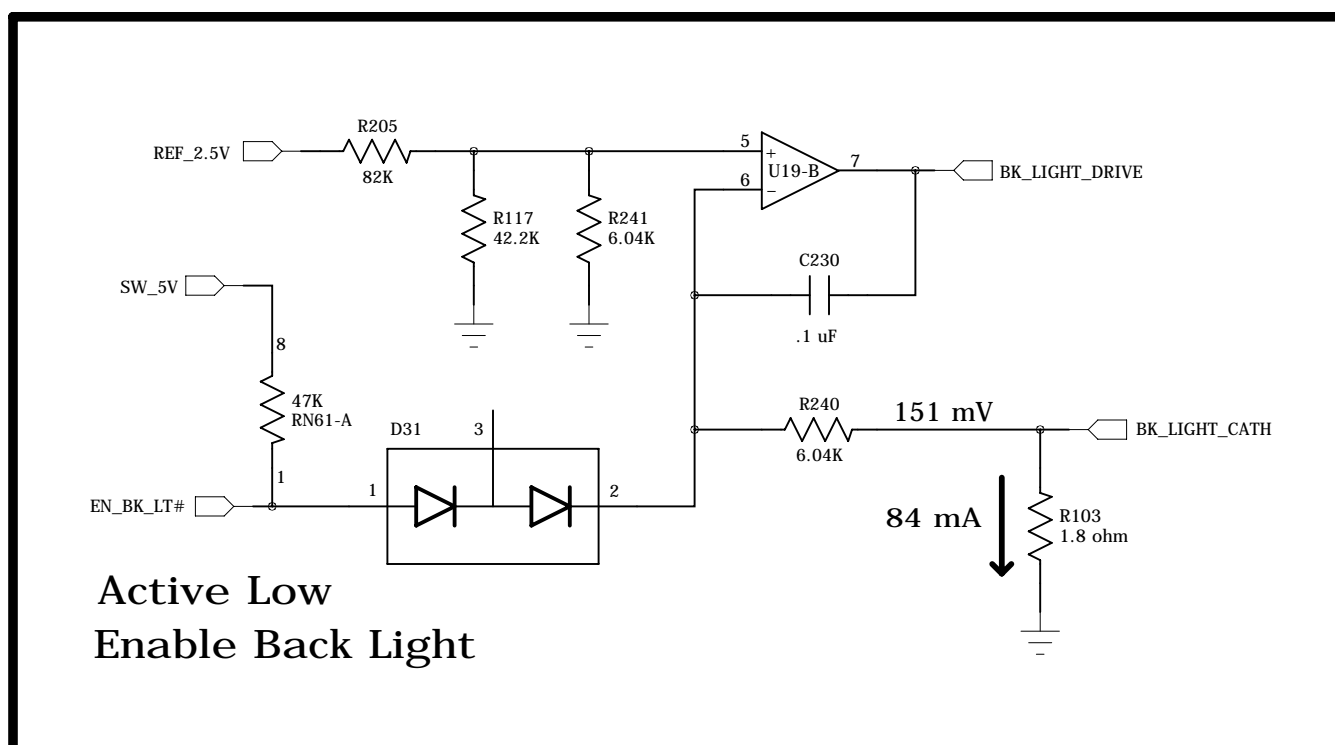
- 9 GND
- 9 Power
- 6 Rsvd for PEX
- 2 for I2C
- 2 for USB
- 4 for SPI Bus
- 2 for Reset and IRQ
- 2 for LCD Backlight
- 1 2.8V_FB
- 27 for FPGA DIO

Tianma 2.8 inch LCD

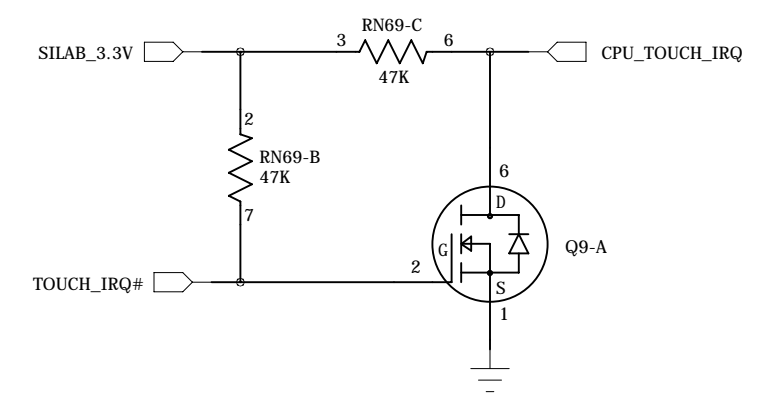
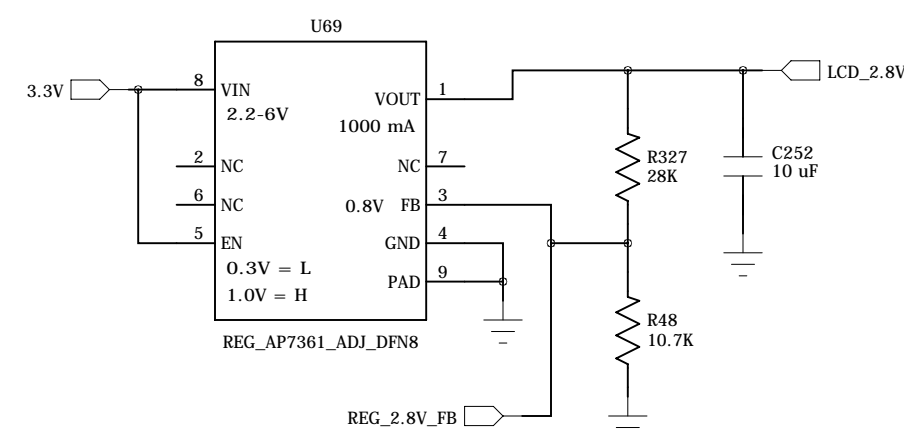
Daughter Bd Bracket



2.8 inch LCD Back Light Driver

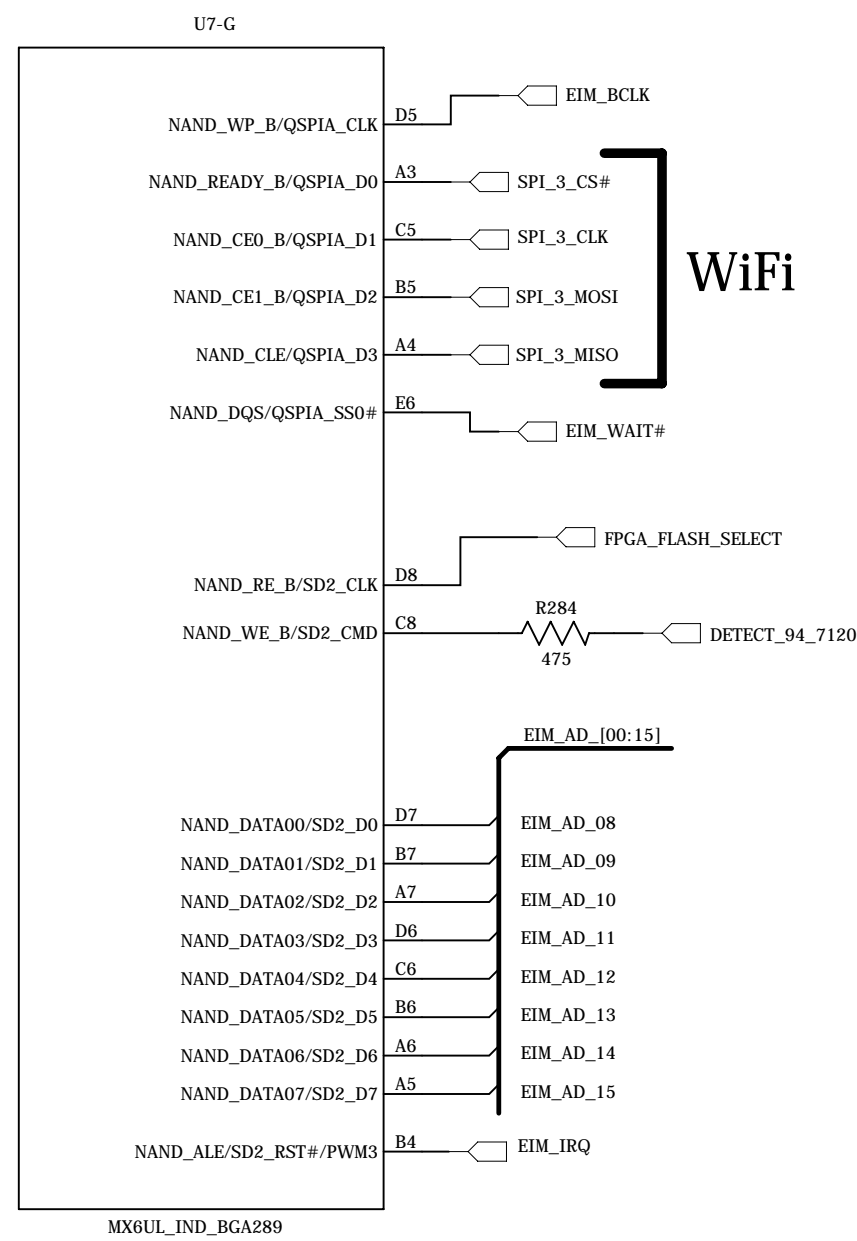


LCD 2.8V Reg.

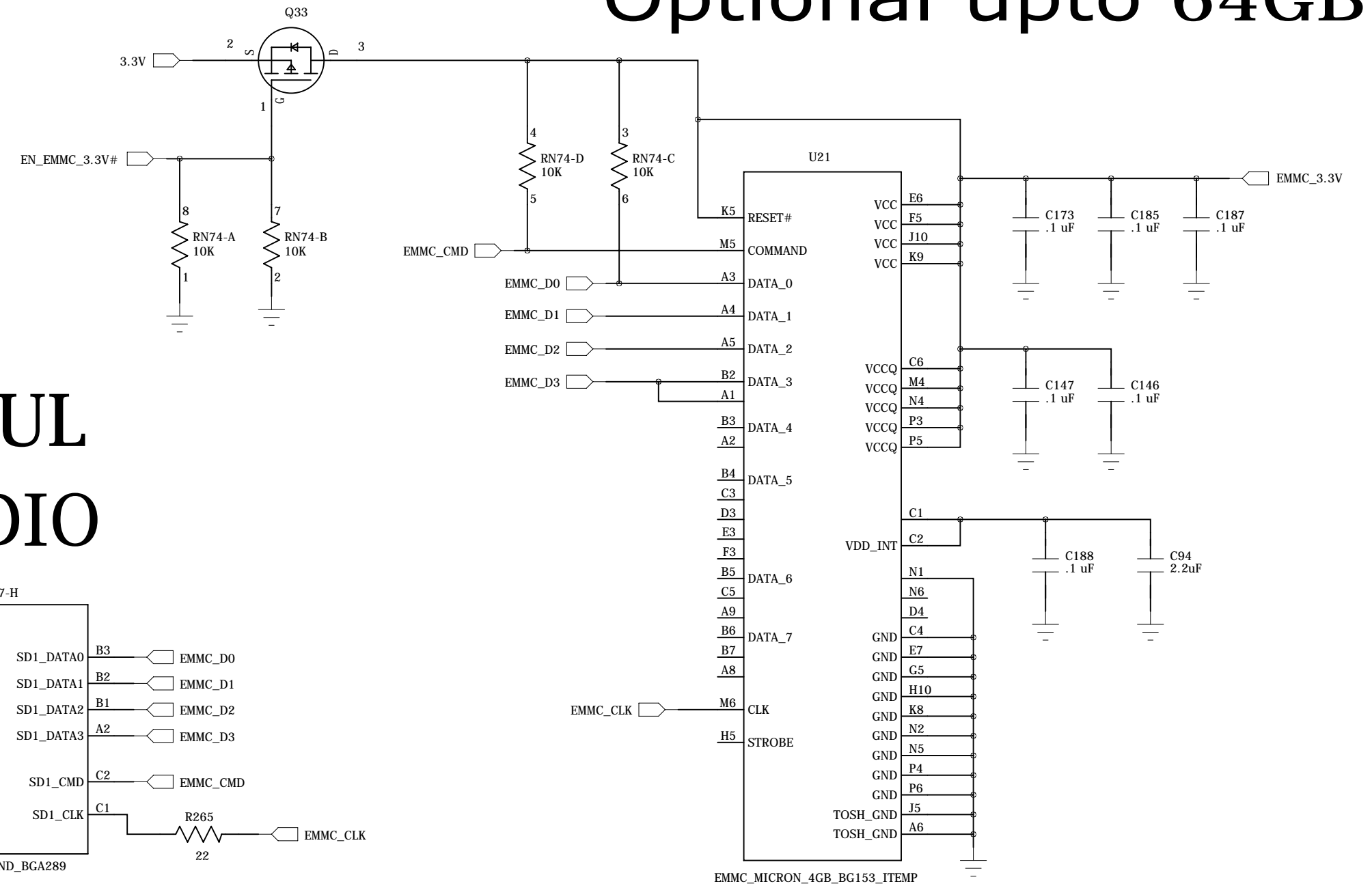
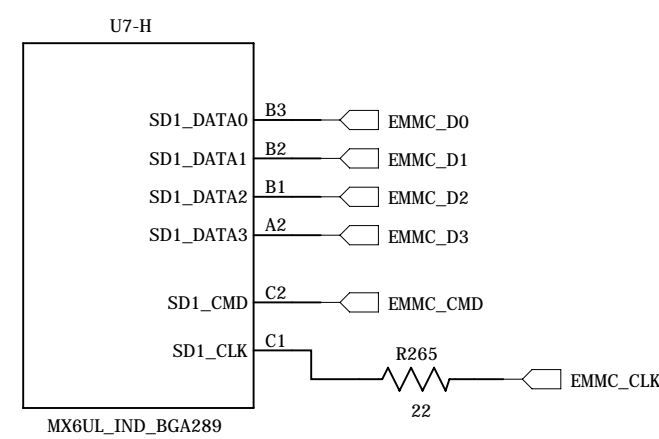


eMMC 4GB Optional upto 64GB

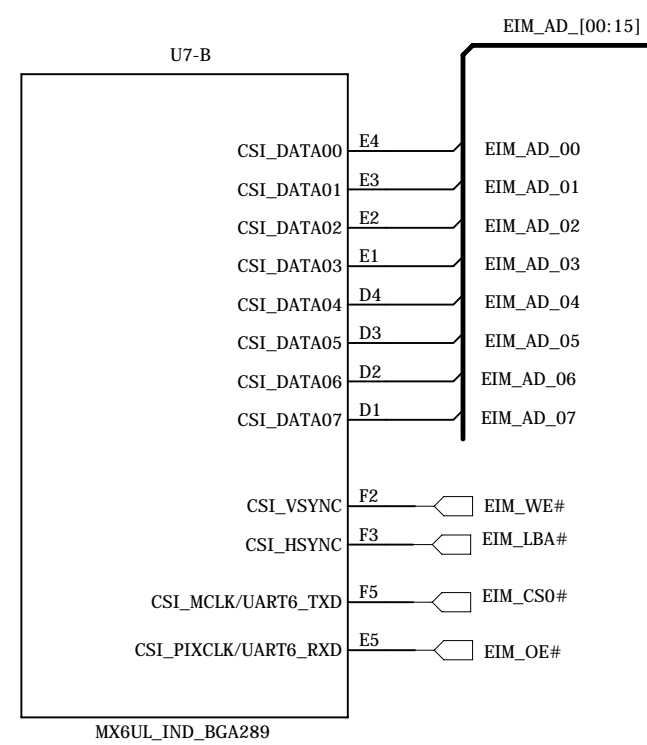
6UL EIM



6UL SDIO

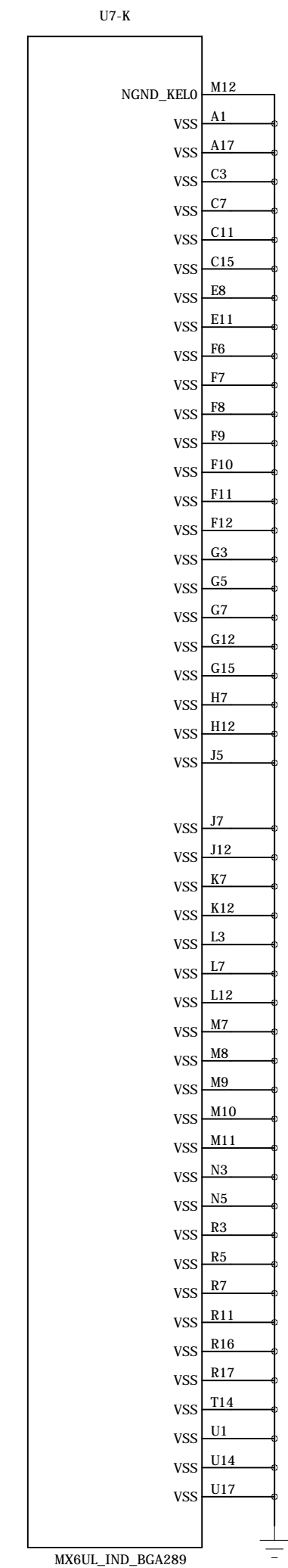
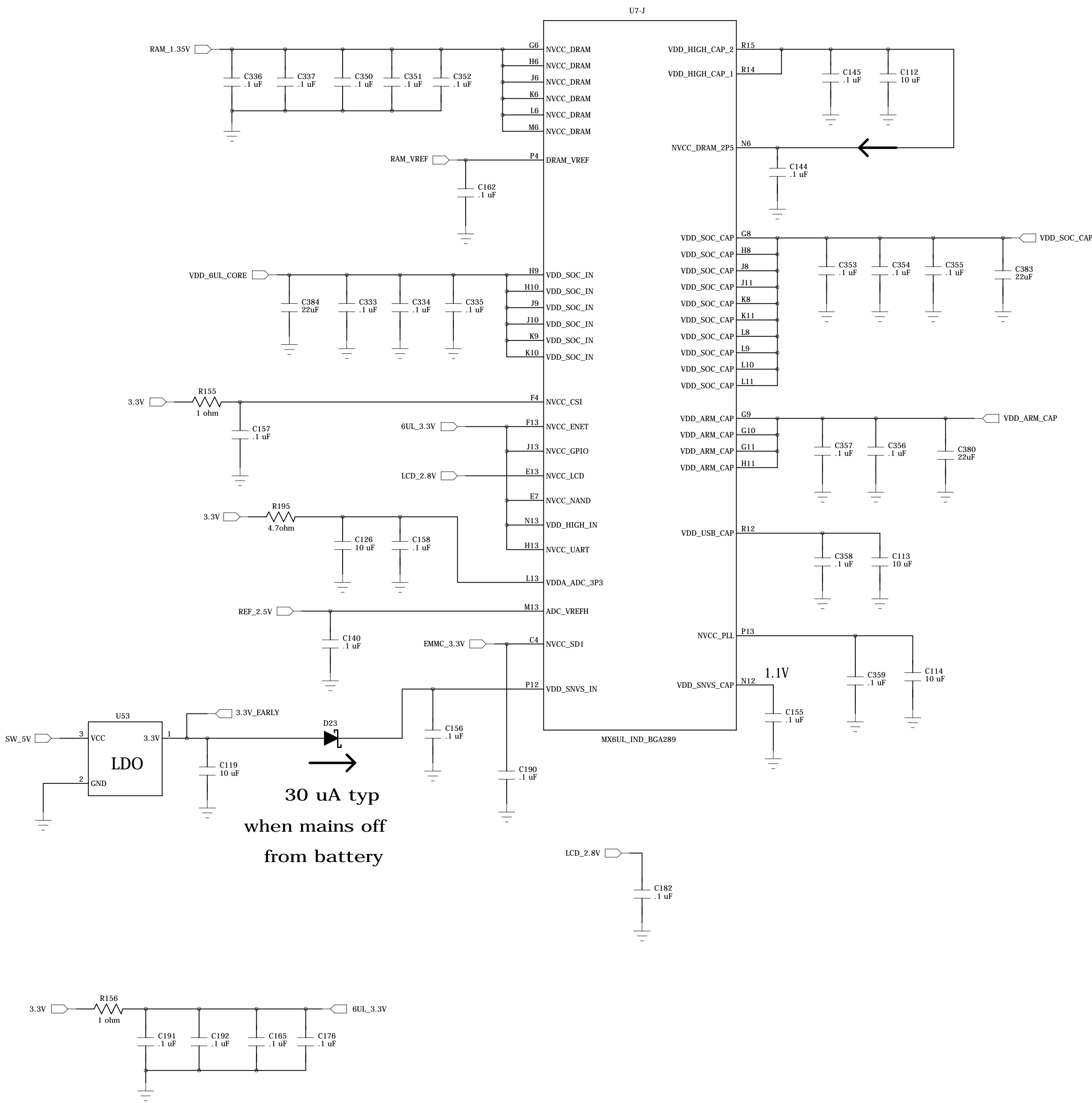


6UL EIM



6UL Power

6UL GND



3.3V 2A Reg #1

SW_5V

3.3V

CPU Core 1A Reg #2

SW_5V

VDD_6UL_CORE

RAM 1.35V 1A Reg #2

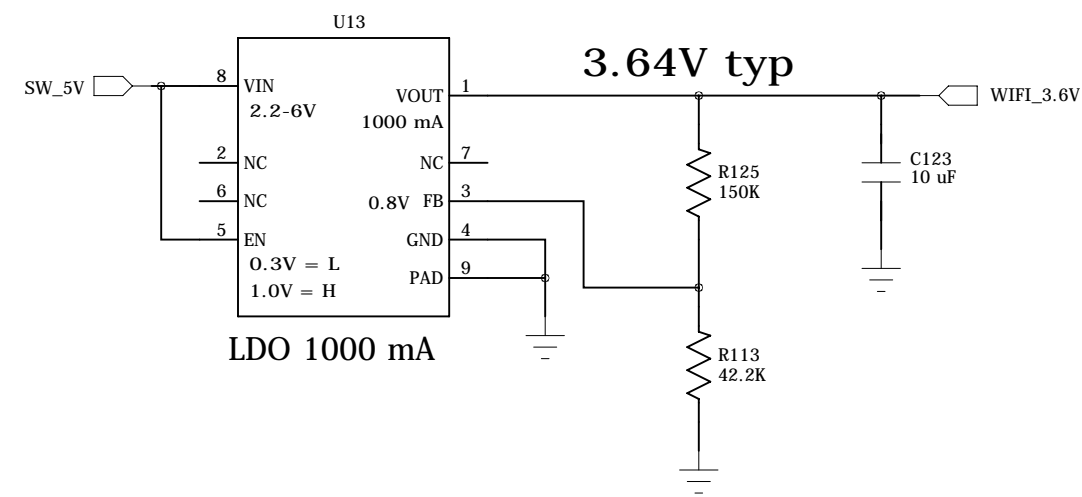
SW_5V

RAM_1.35V

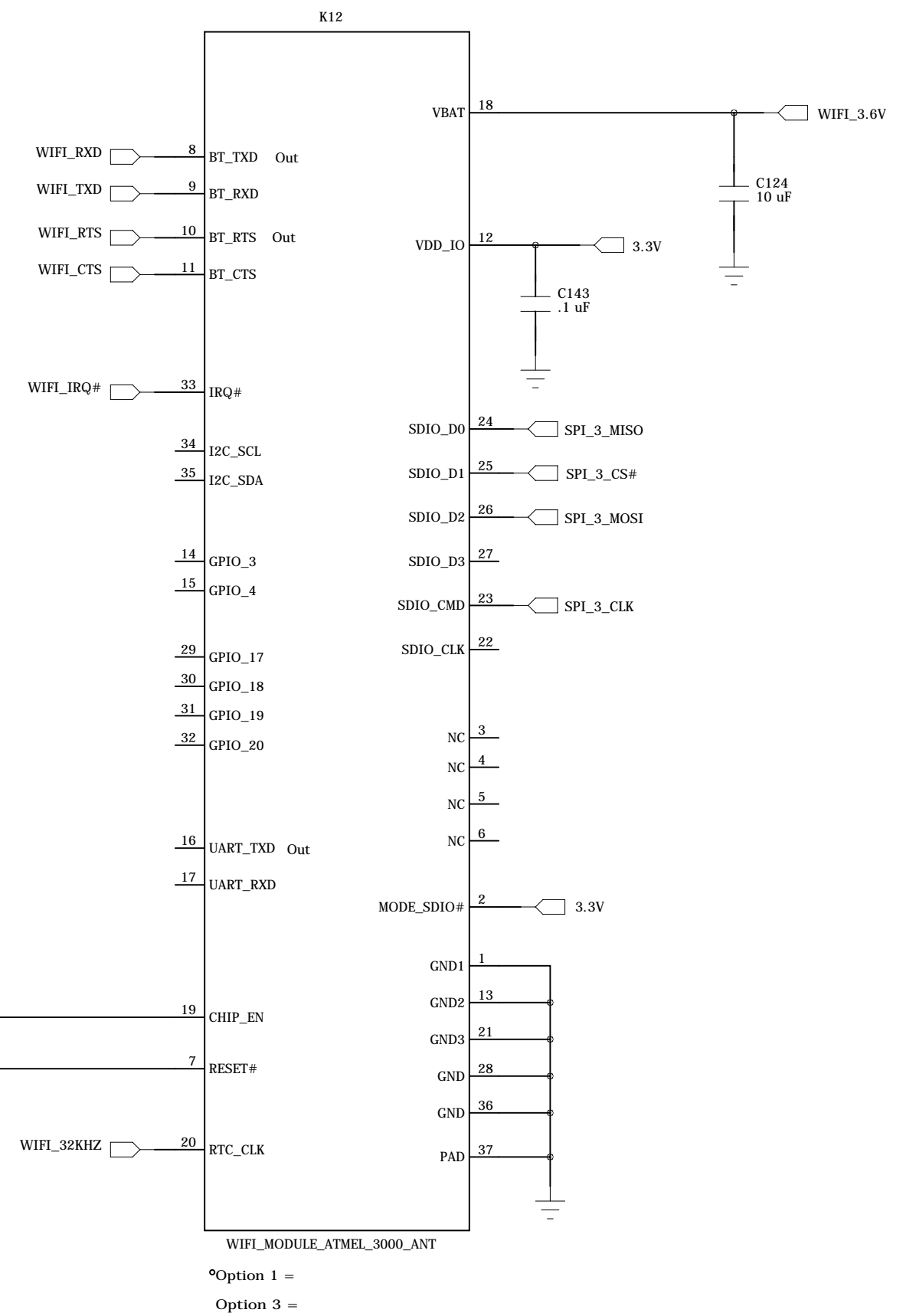
Technologic Systems	Date	Aug. 22, 2018
Title: TS-7120		
Rev: P1	Designer	Sheet 12 of 34

WiFi

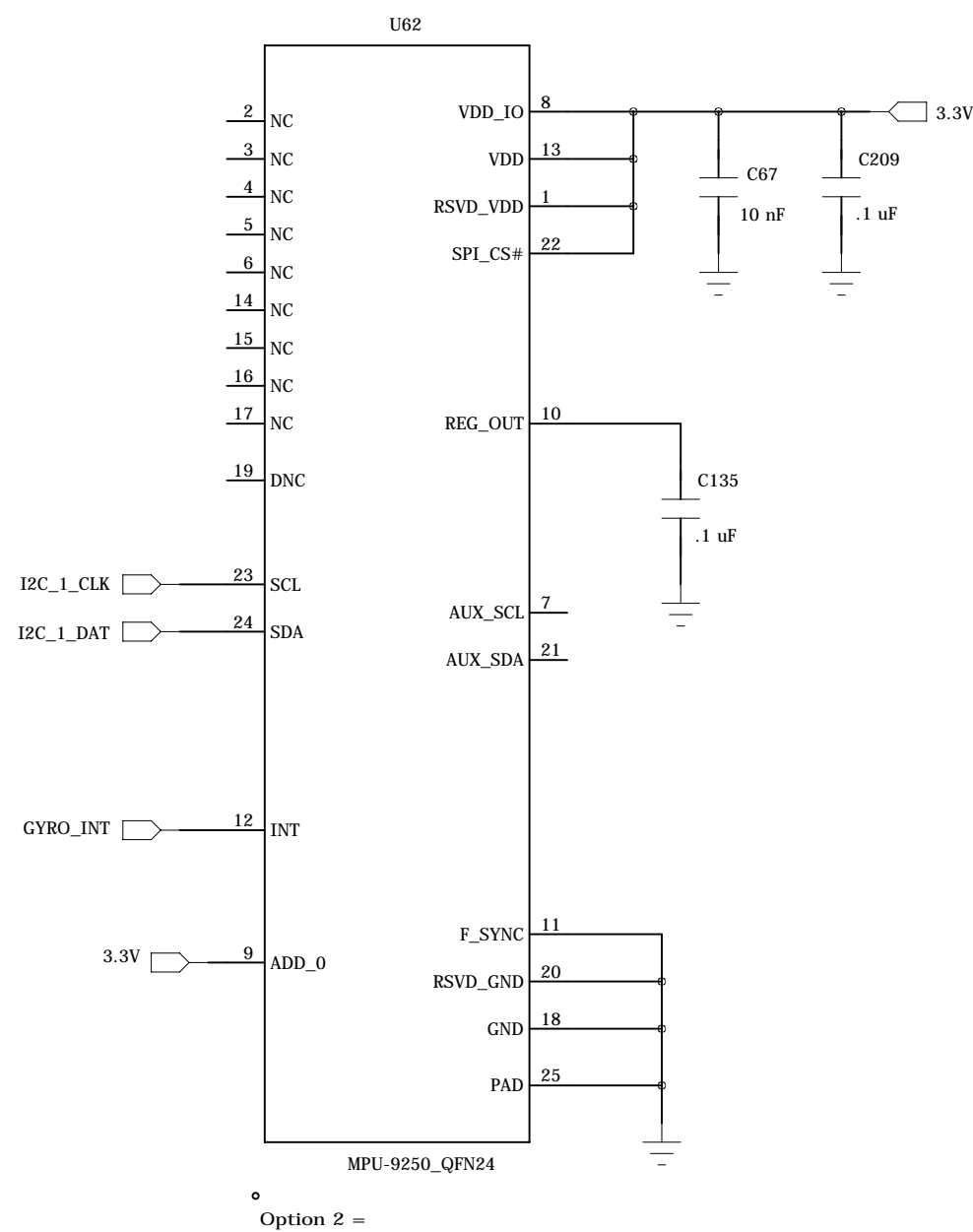
WiFi 3.6V Regulator



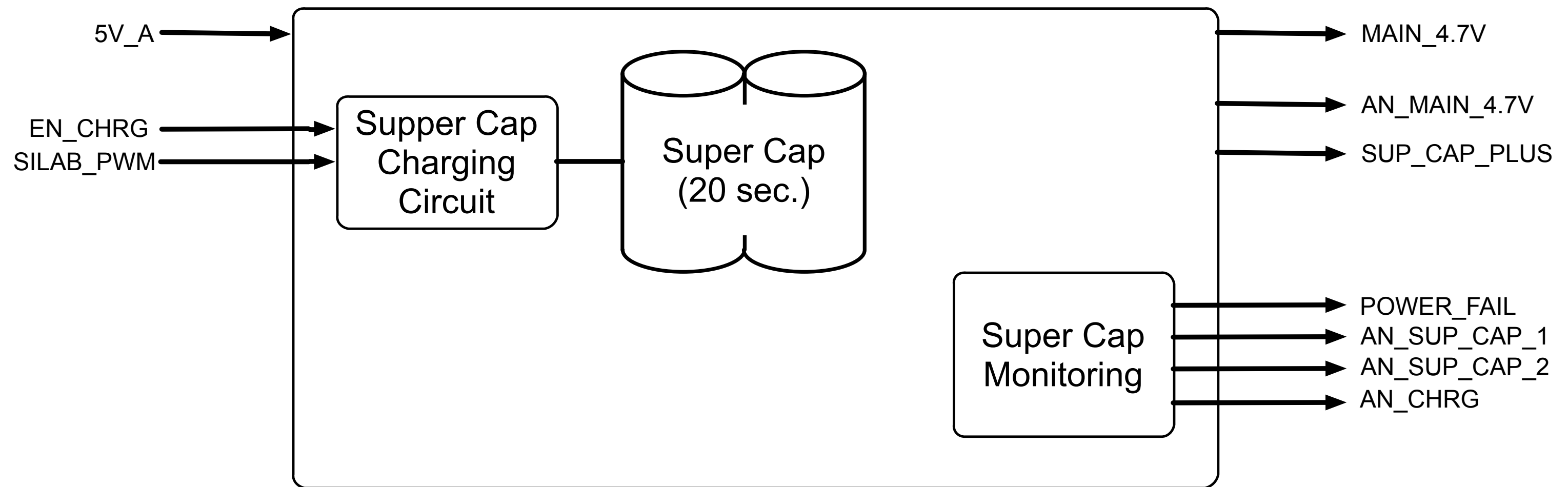
WiFi / Bluetooth Radio Module



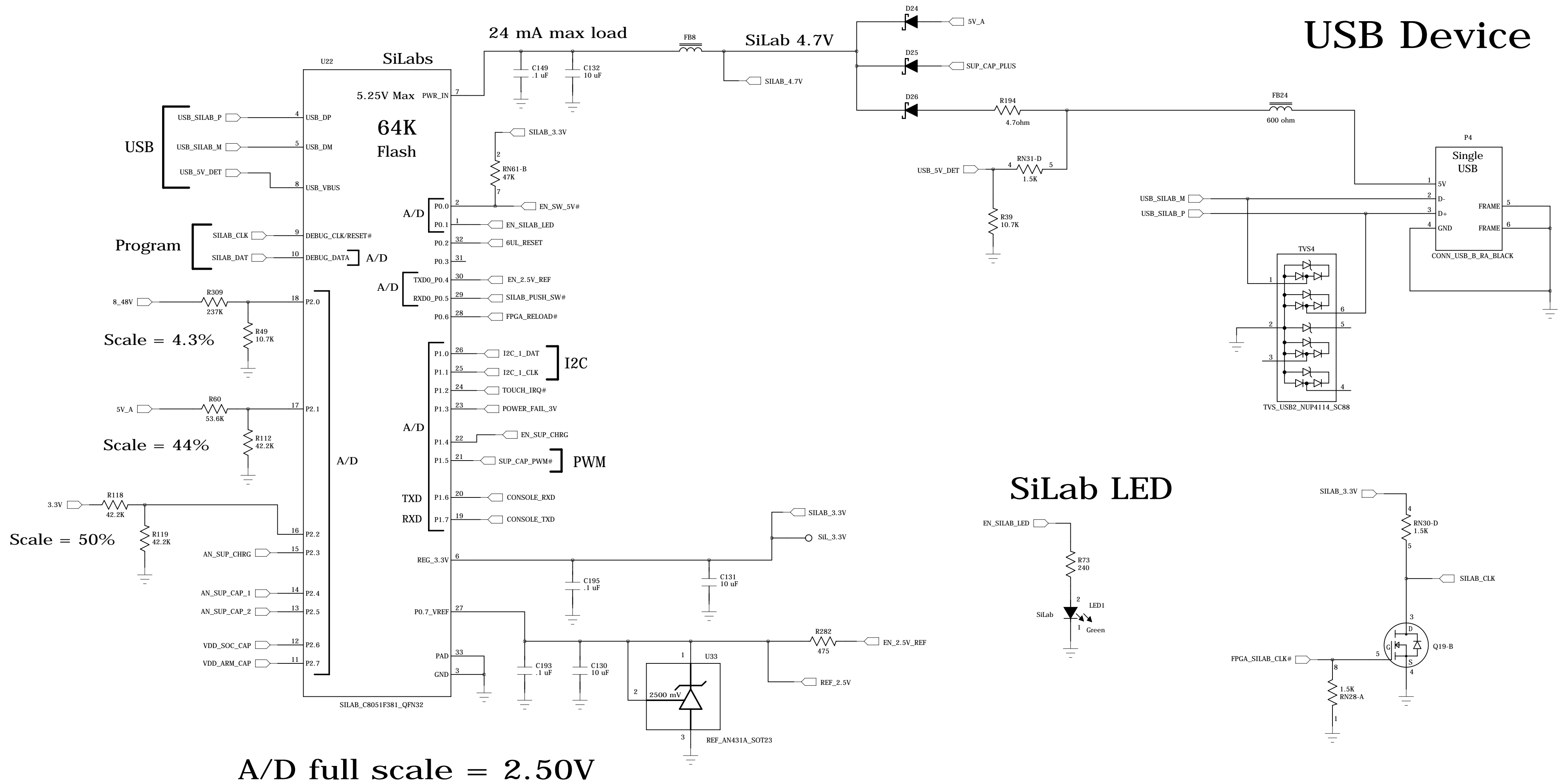
Gyro-Accelerometer



SuperCap 20 Second Power Hold

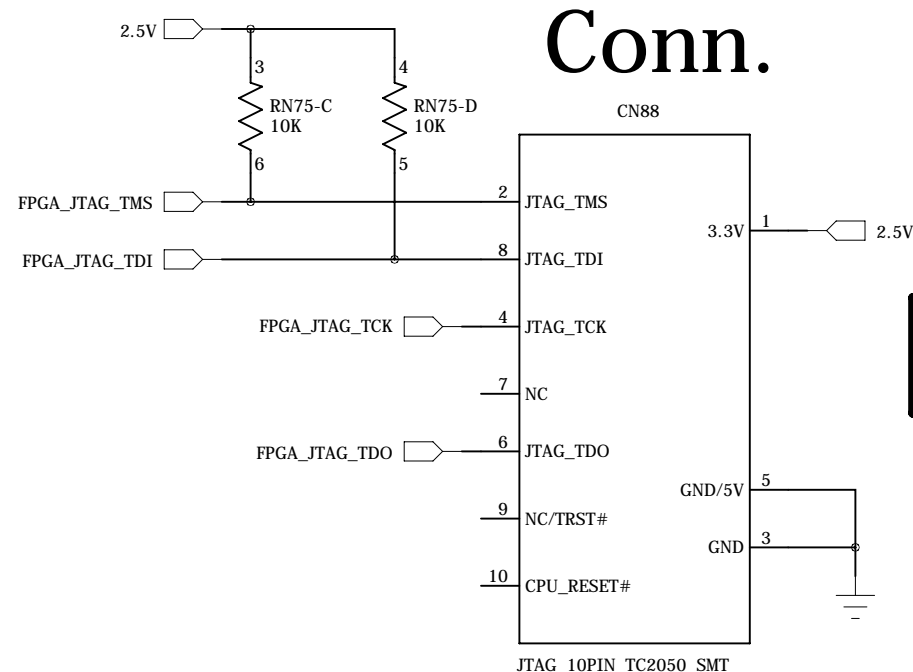


USB Device Port and SiLab uC



FPGA JTAG

Conn.

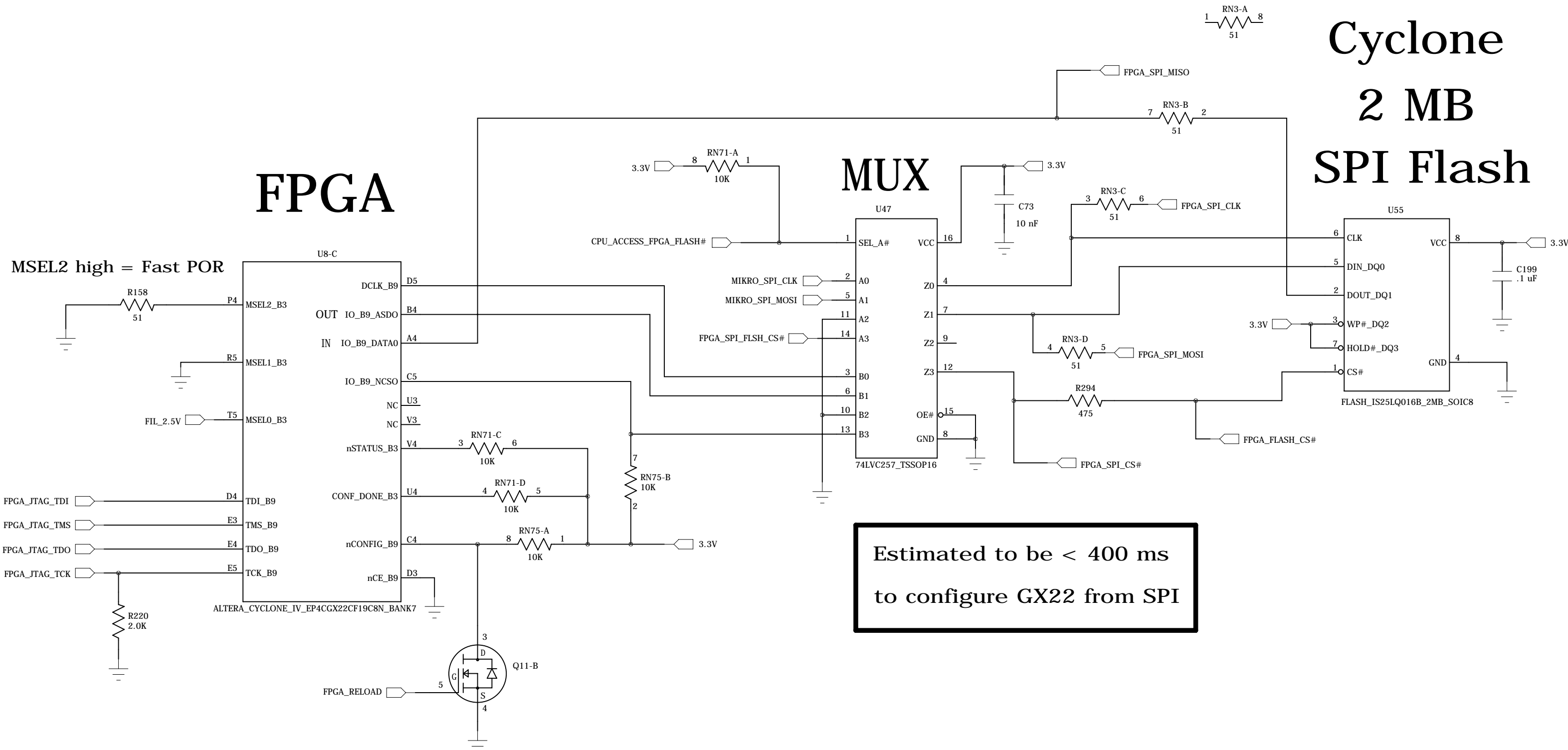


Tag-Connect

Cyclone 2 MB SPI Flash

FPGA

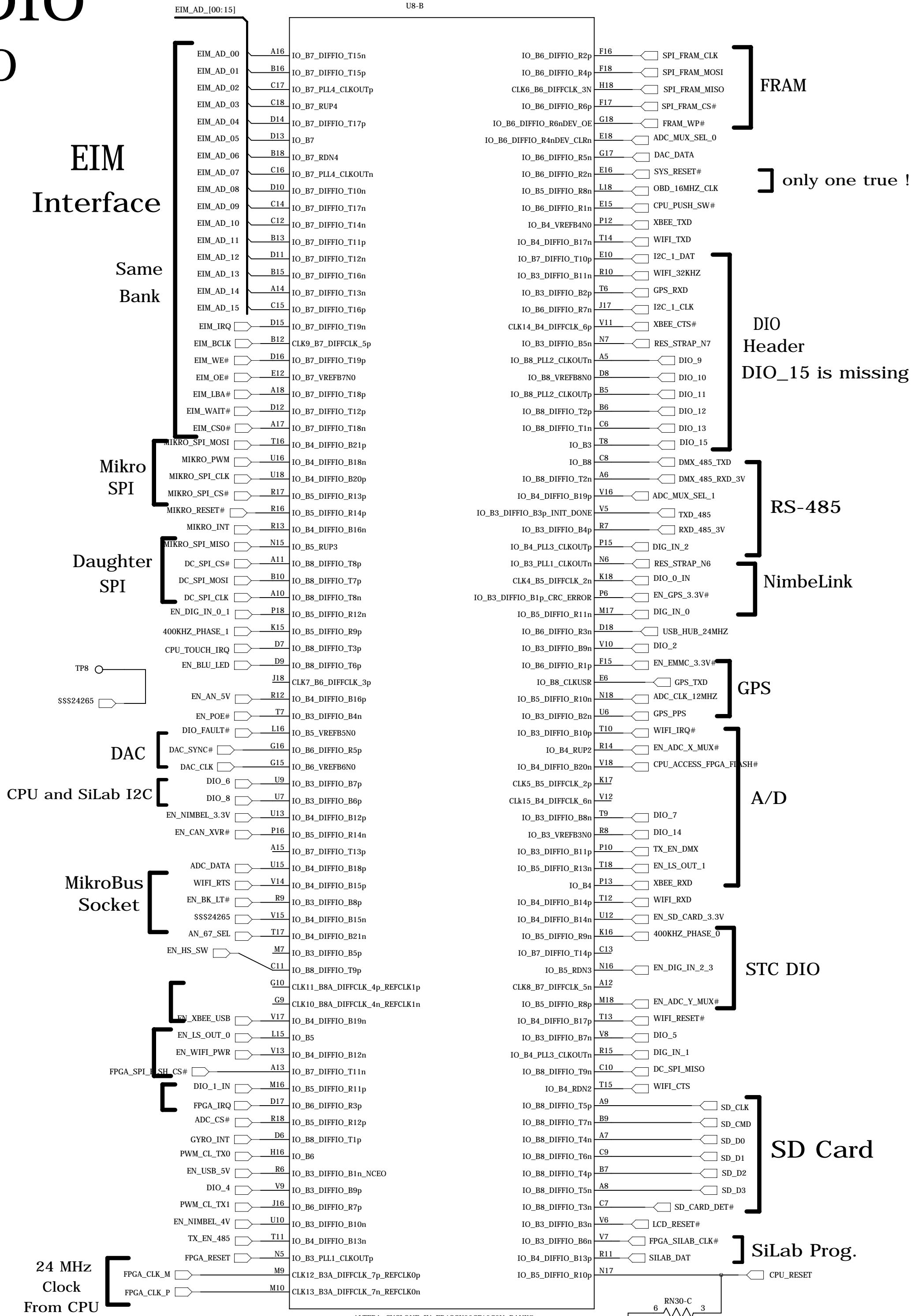
MUX



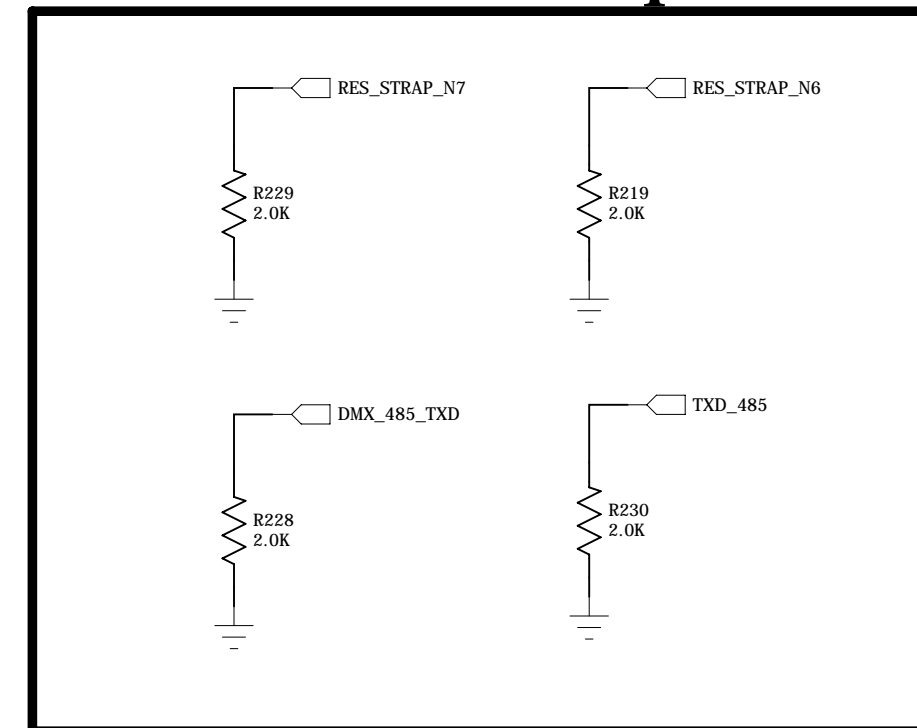
Technologic Systems		Date Aug. 22, 2018
Title: TS-7120		
Rev: P1	Designer	Sheet 17 of 34

FPGA DIO

147 DIO



Res. Straps

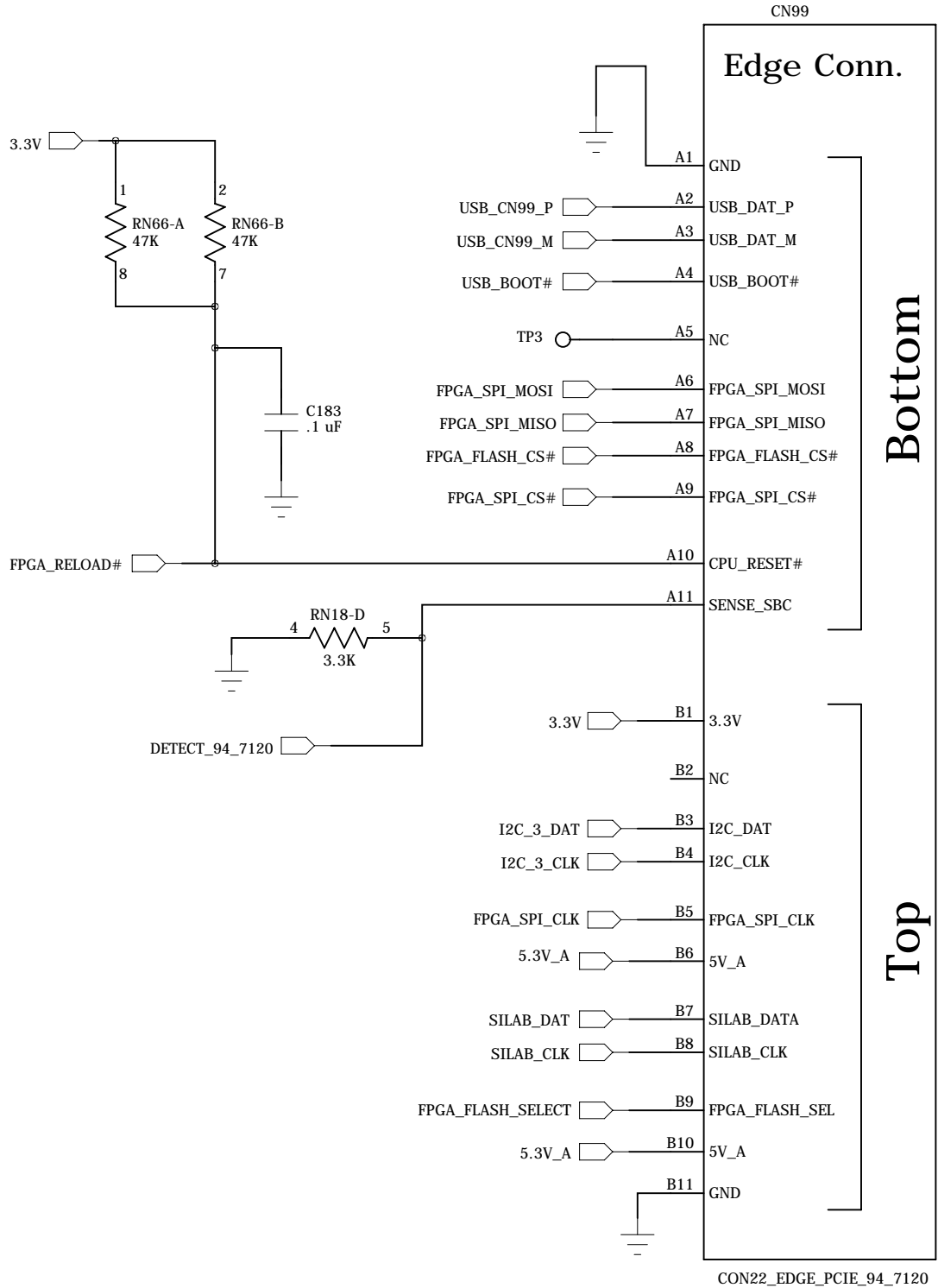


Technologic Systems	Date	Aug. 22, 2018
Title: TS-7120		
Rev: P1	Designer	Sheet 18 of 34

FPGA Stuff

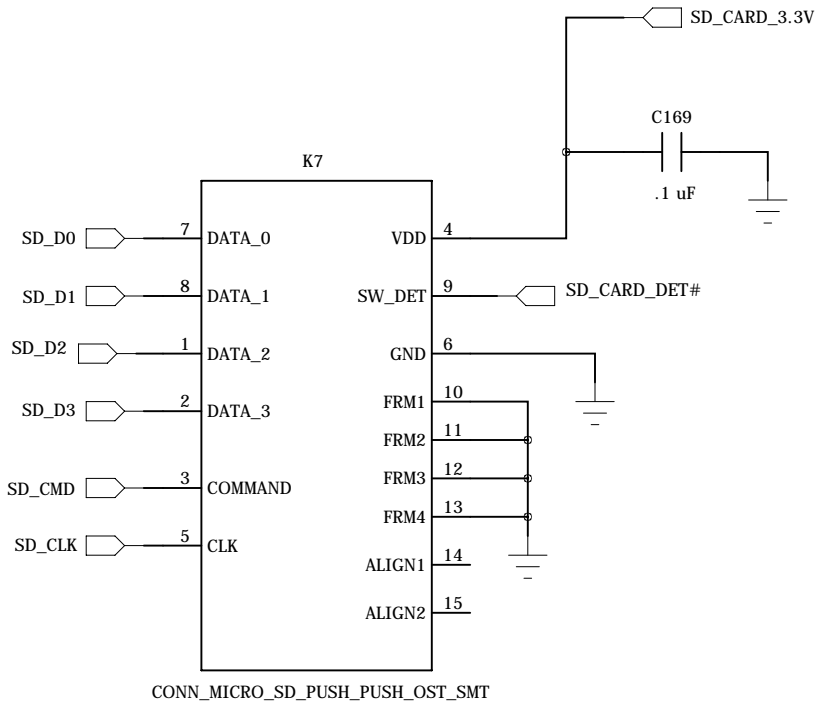
CN99

Factory Programing Interface

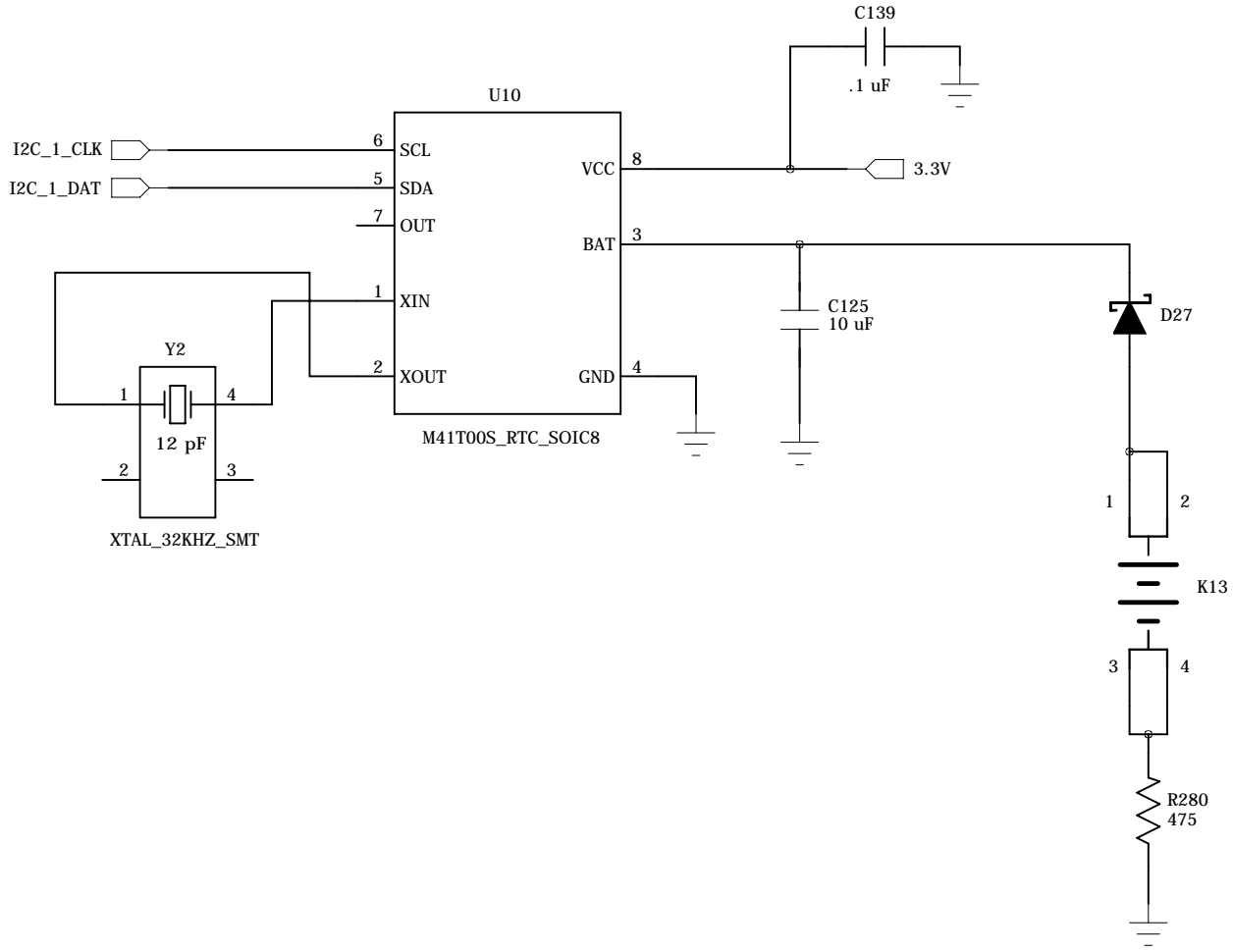


Technologic Systems		Date Aug. 22, 2018
Title: TS-7120		
Rev: P1	Designer	Sheet 19 of 34

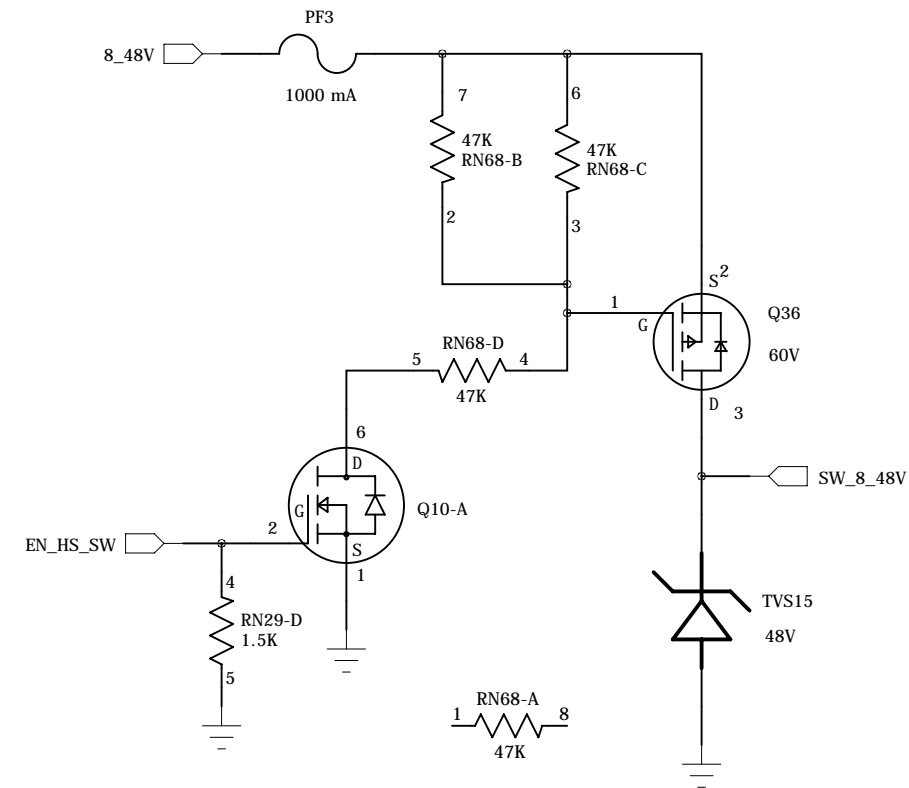
Push-Push Micro SD Card Socket



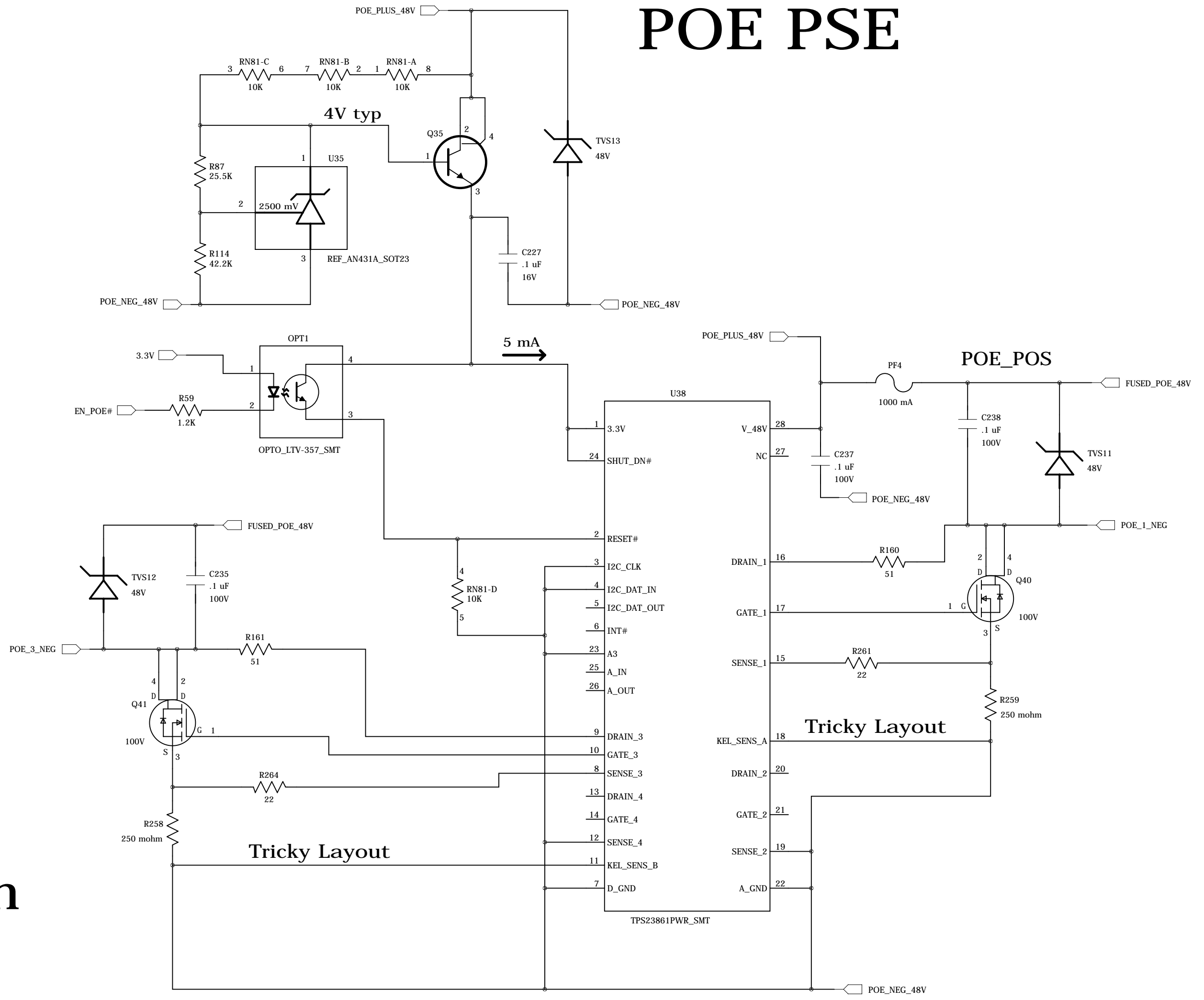
ST Micro RTC



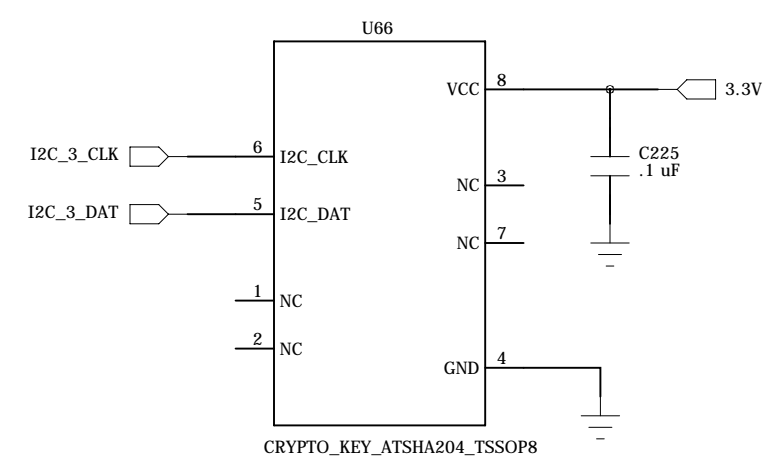
STC High-Side Switch



POE PSE

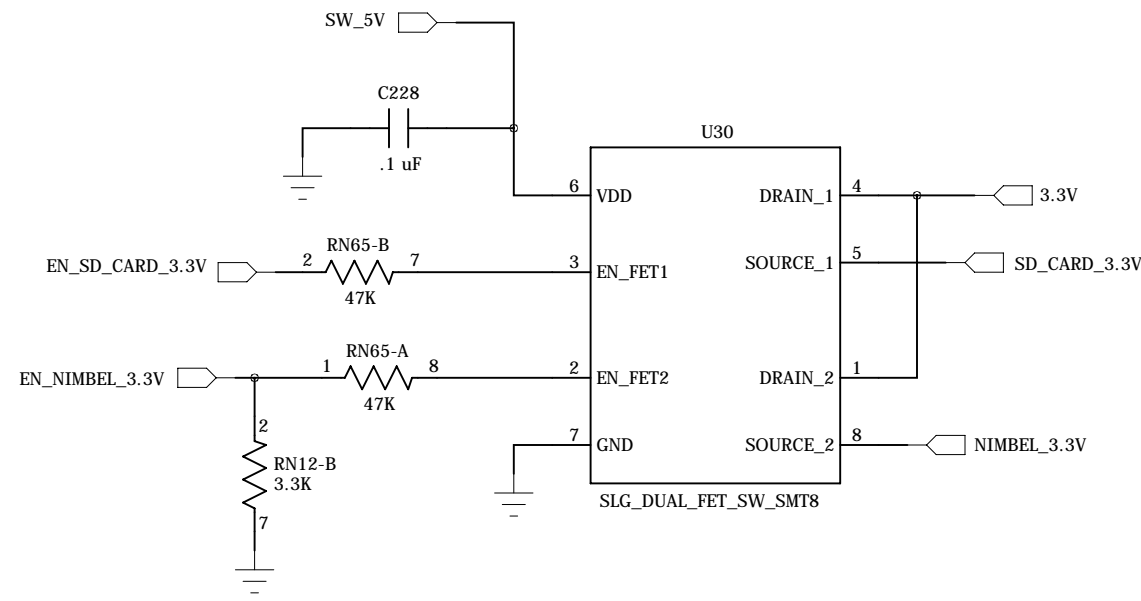


Crypto Authentication

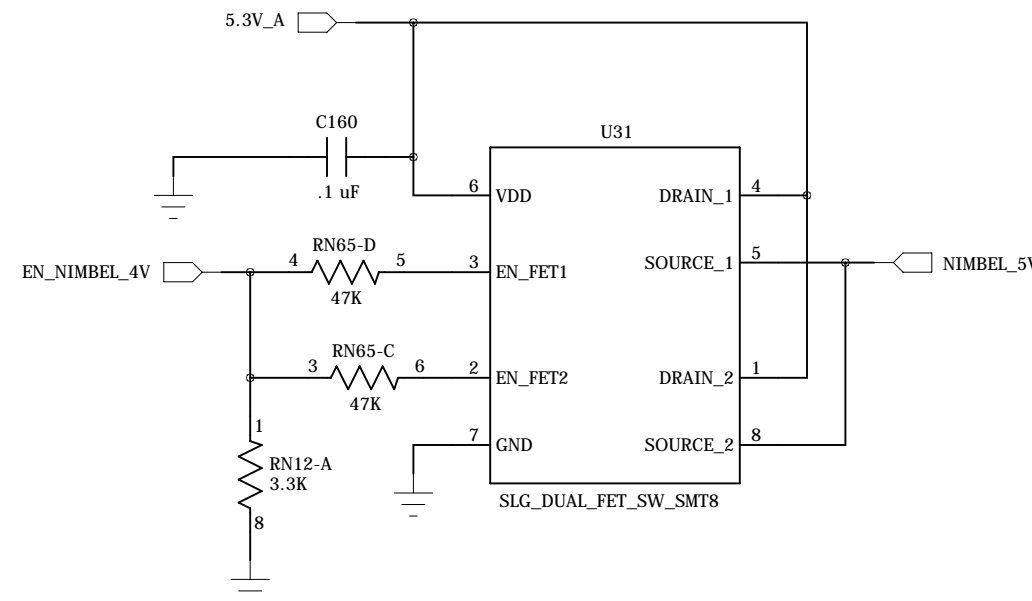


Technologic Systems		Date Aug. 22, 2018
Title: TS-7120		
Rev: P1	Designer	Sheet 22 of 34

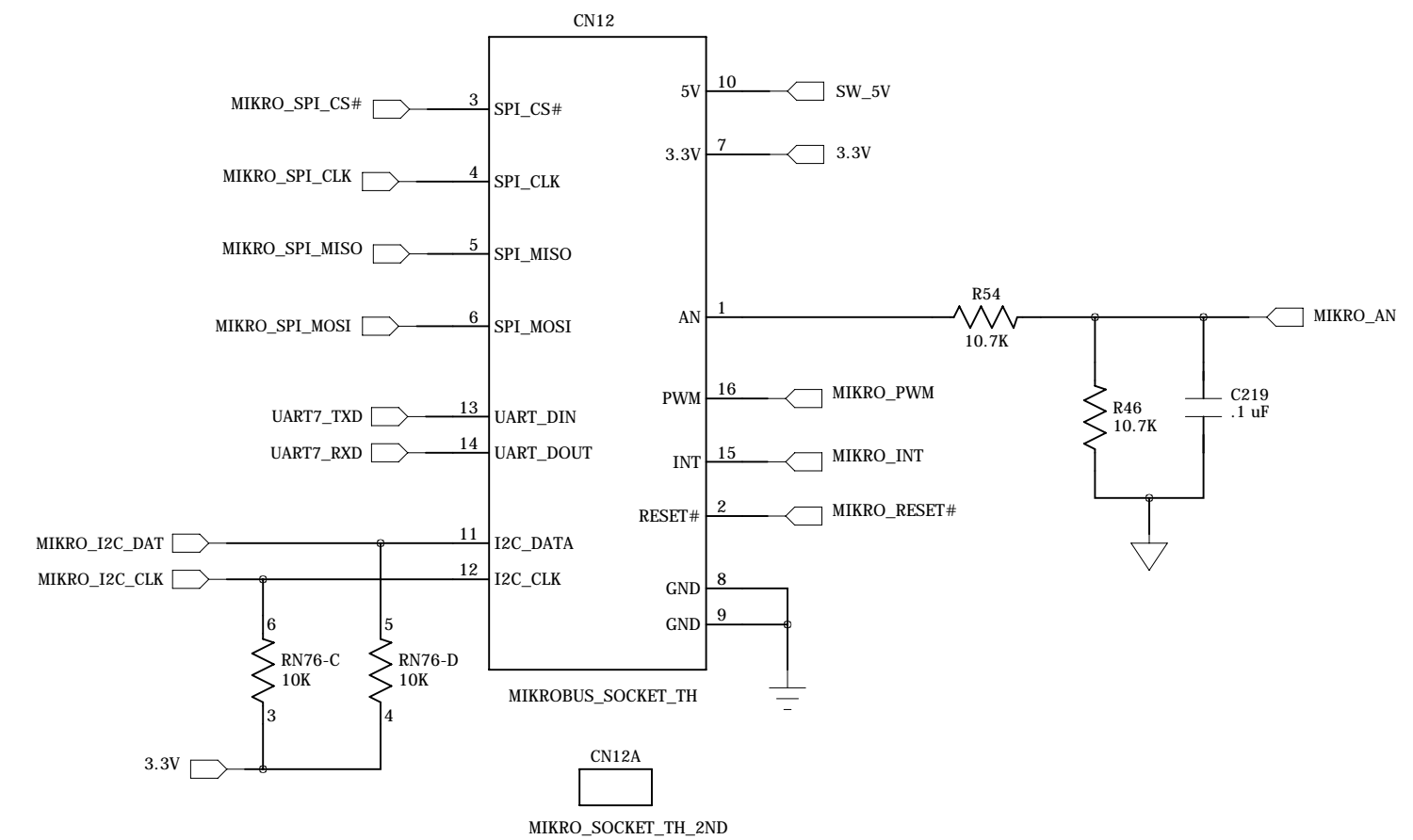
NimbeLink and SD Card Sw. 3.3V



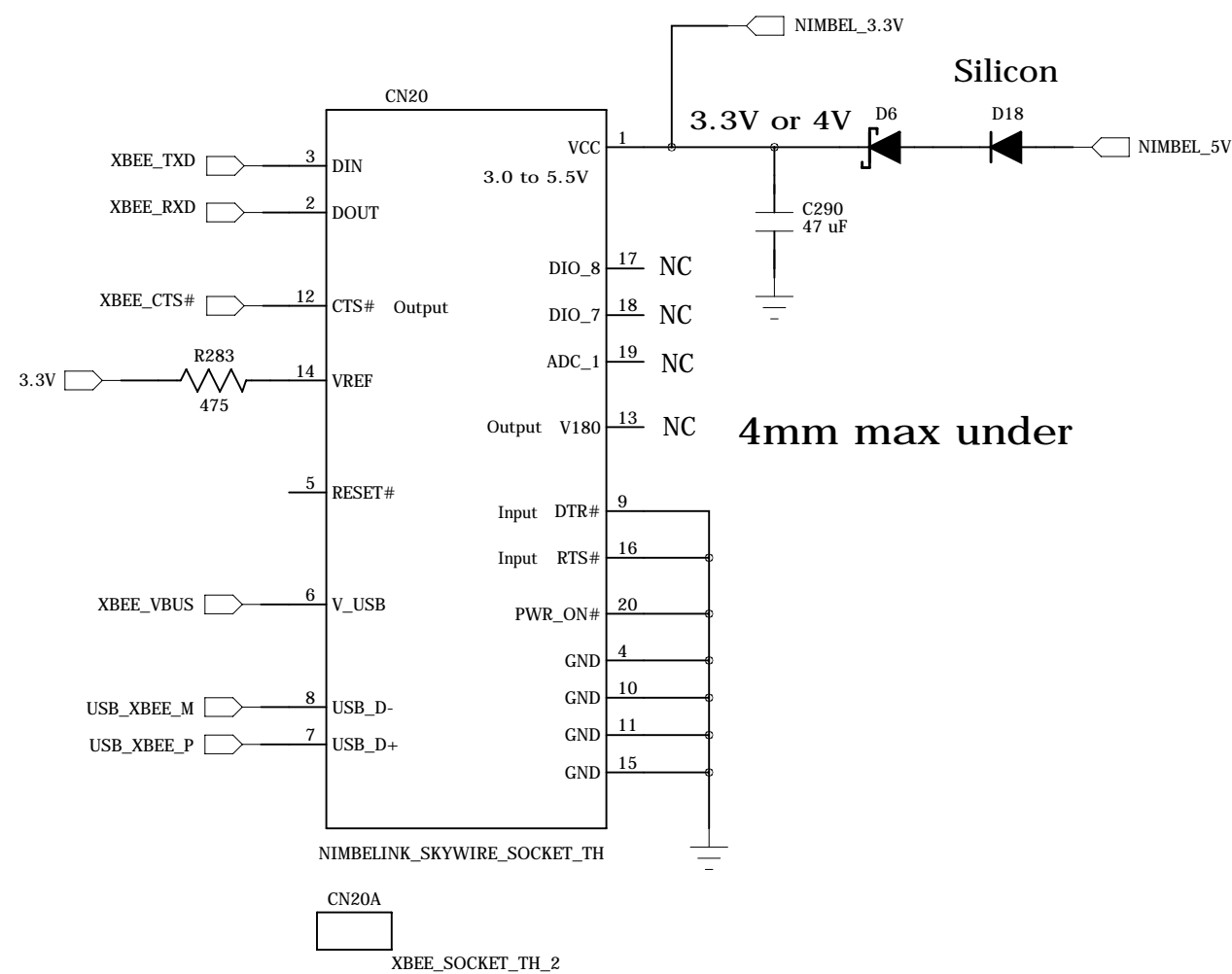
NimbeLink 4V Switched Power



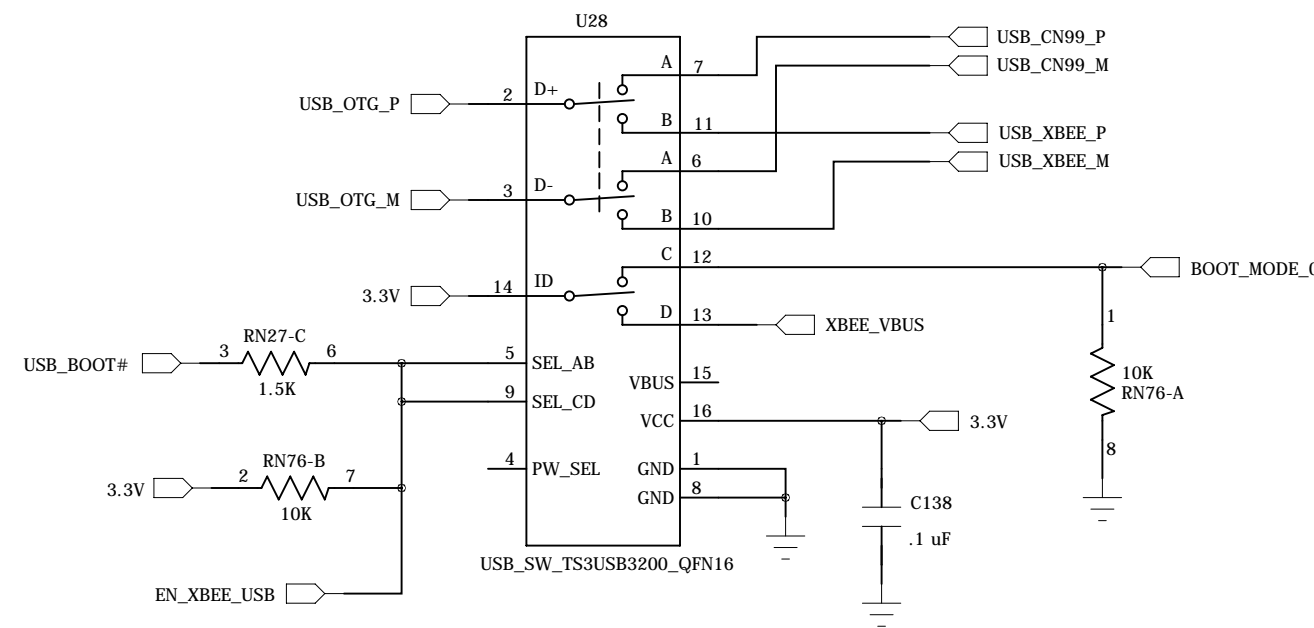
Mikro Bus Socket



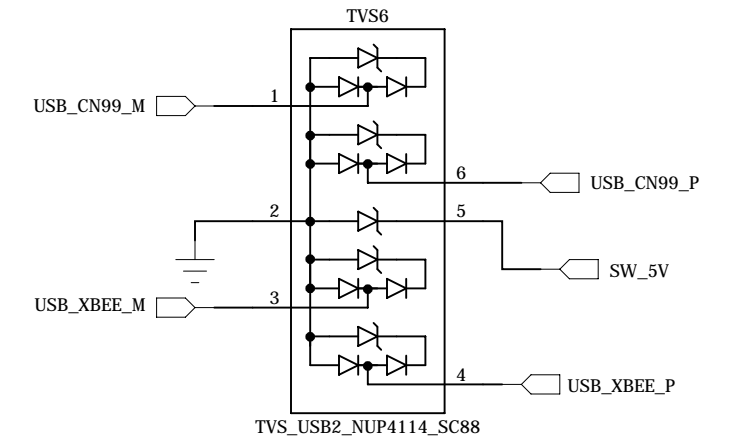
NimbeLink or Xbee Modem Socket



USB OTG MUX To Xbee or CN99 Boot

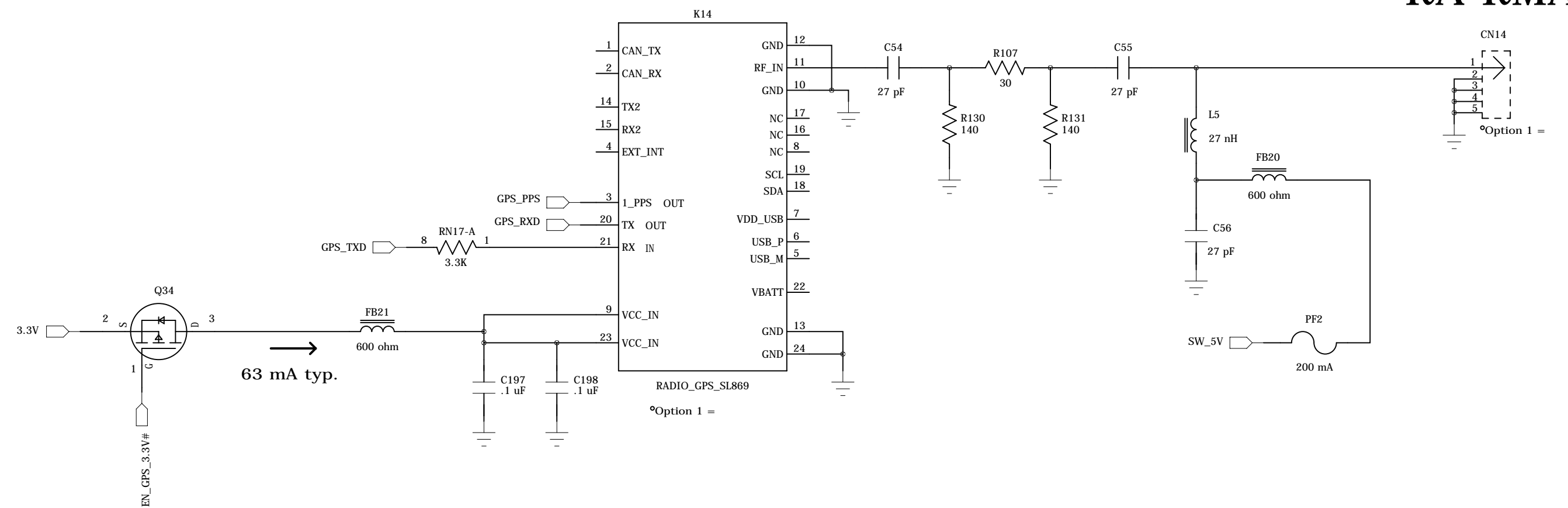


OTG TVS

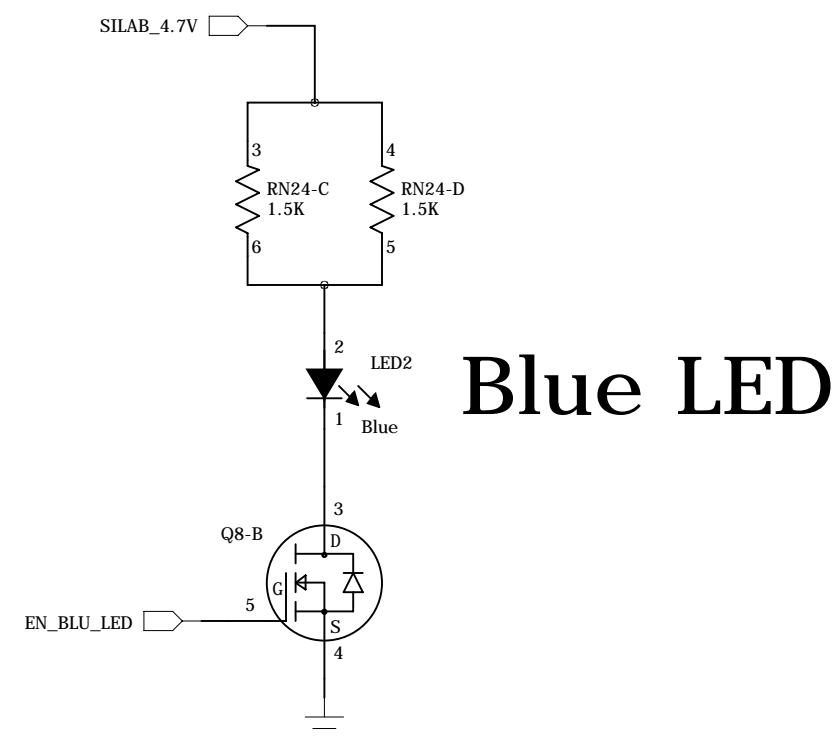
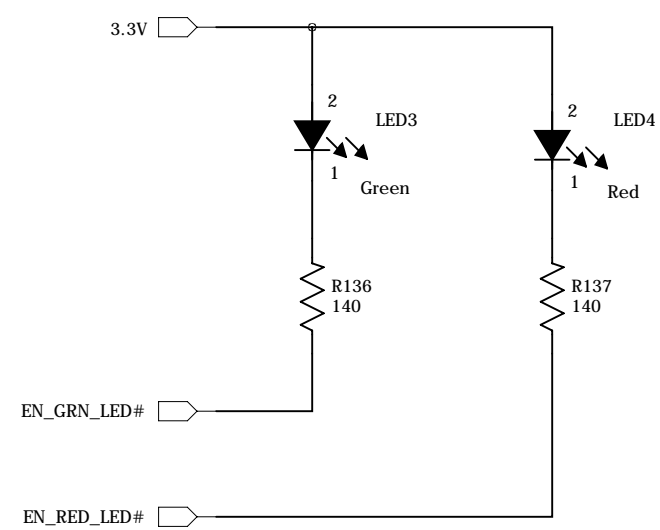


Telit SL869 GPS Radio

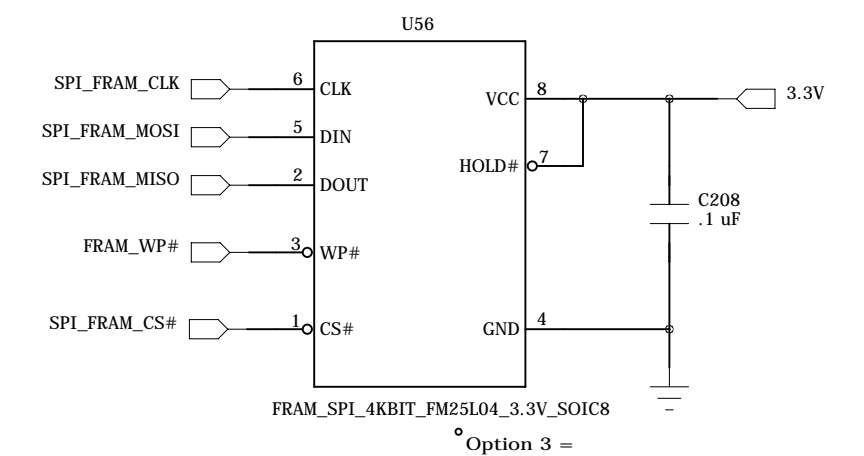
RF Conn.
RA RMA



SMT RA LEDs



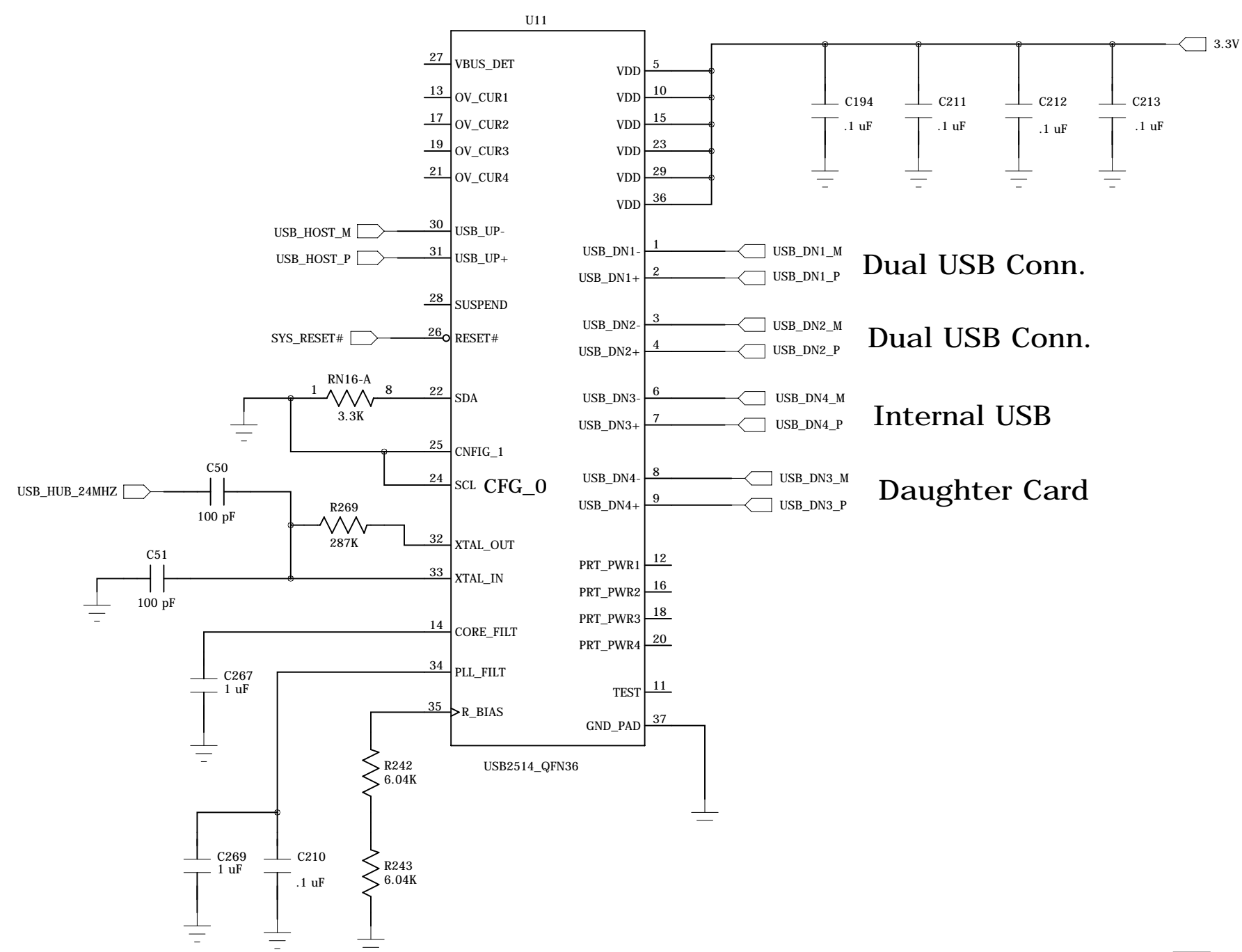
FRAM Memory



2K Bytes

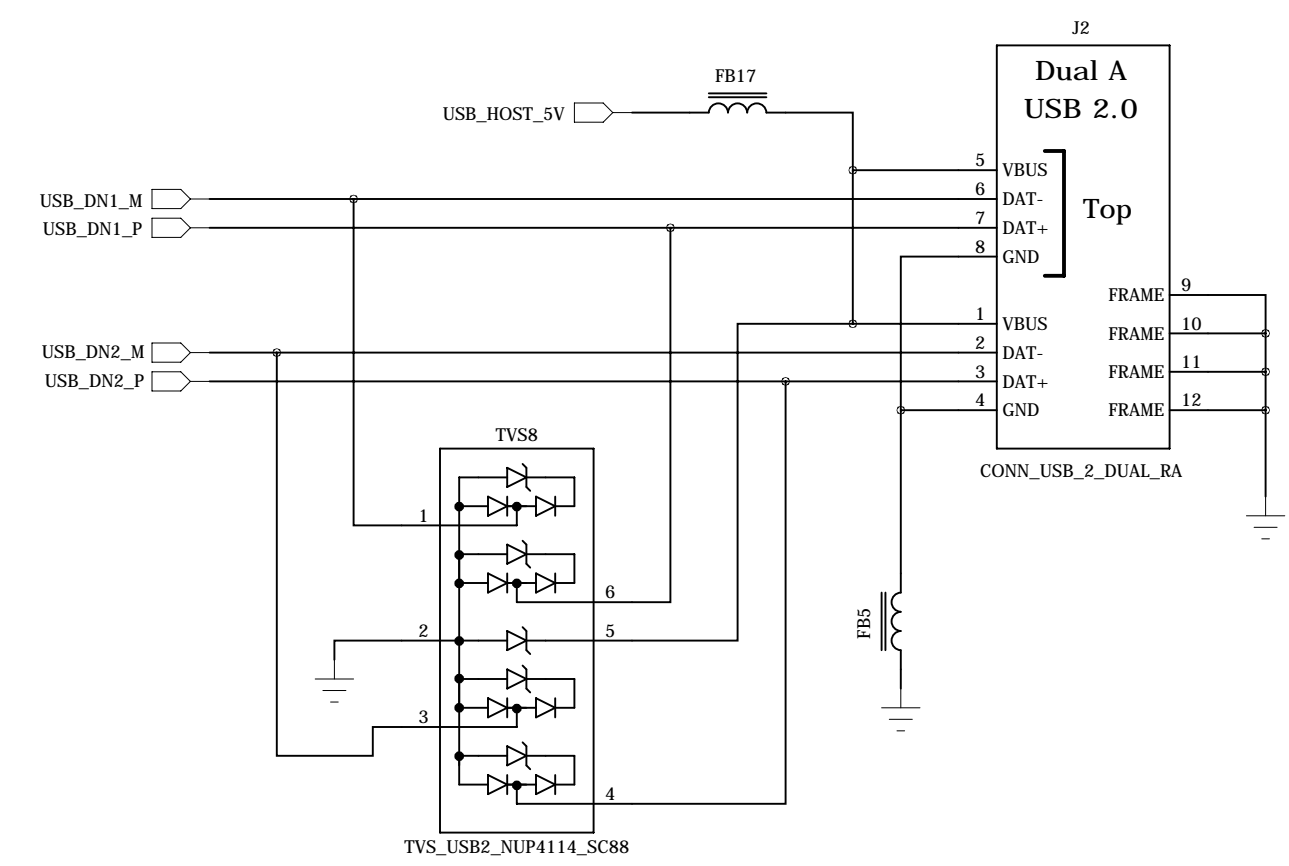
Technologic Systems		Date Aug. 22, 2018
Title: TS-7120		
Rev: P1	Designer	Sheet 24 of 34

USB2 Hub

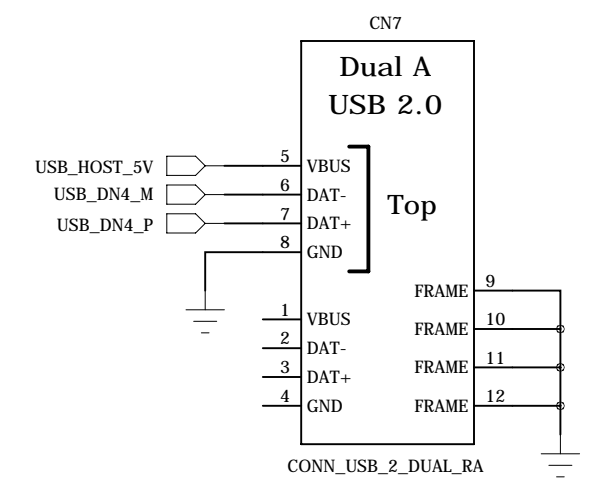


Dual USB Conn.
Dual USB Conn.
Internal USB
Daughter Card

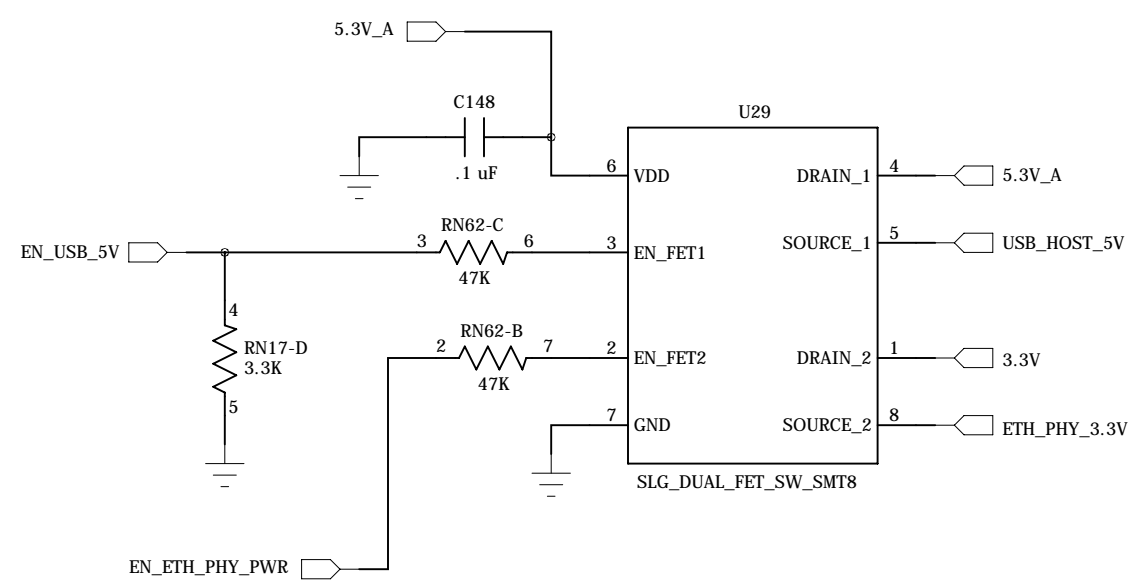
Dual Host USB 2.0



Internal Host USB



Eth PHY and USB Switched Power



Rise time of both outputs
measured at ~1V/ms

Analog Inputs 0-3 --> 0-25 mA or 0-5V

Analog Inputs 4-5 --> 0-10V

HART compatible 4-20 mA

HART compatible 4-20 mA

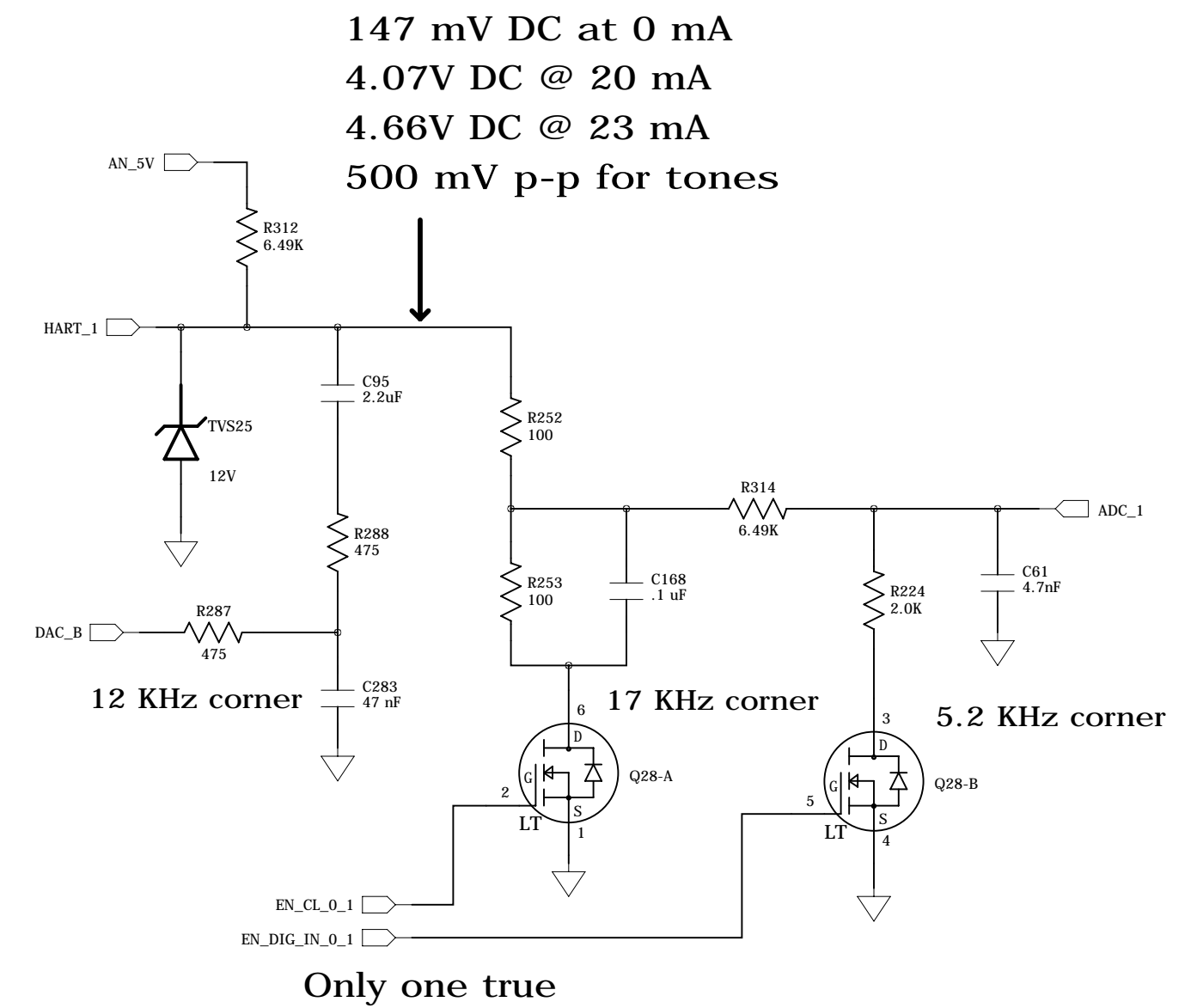
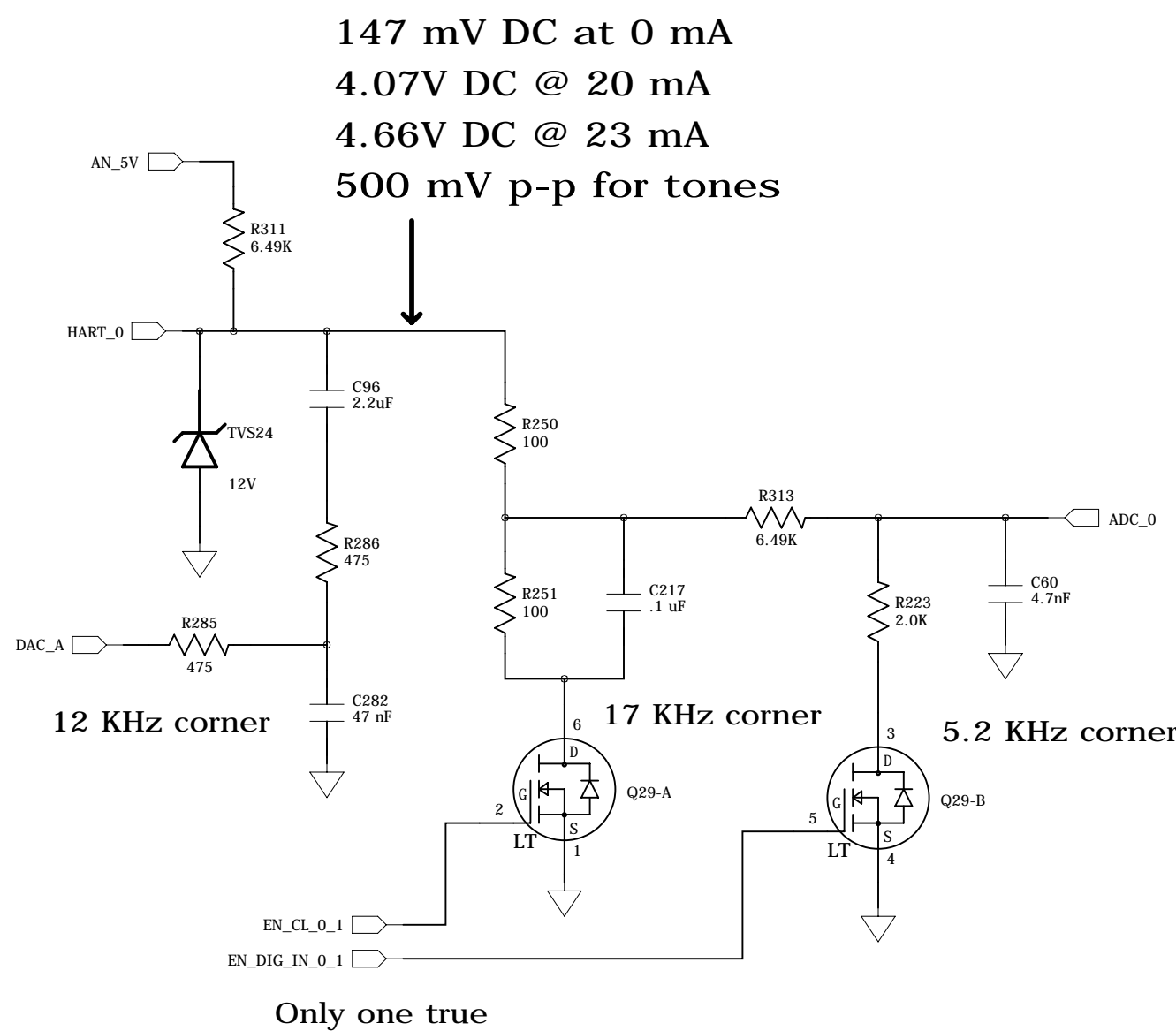
0-24 mA
or 0-5V
or Dig. Input
Dry Contact compatible

Input impedance is
196 ohm DC
163 ohms AC

3 Vp-p needed at DAC_A
to get 500 mV p-p at TVS

1 uF forms high pass
- corner at 140 Hz

$10.7K \text{ par } 200 \text{ par } 950 = 163 \text{ ohms}$

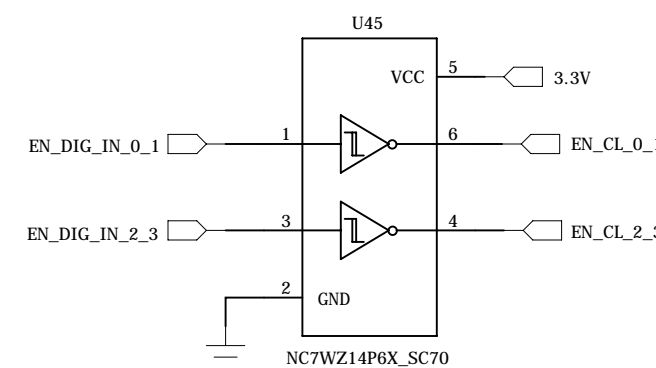


HART Protocol = Bell 202

Half Duplex 1200 baud

FSK, 1200 Hz = Mark

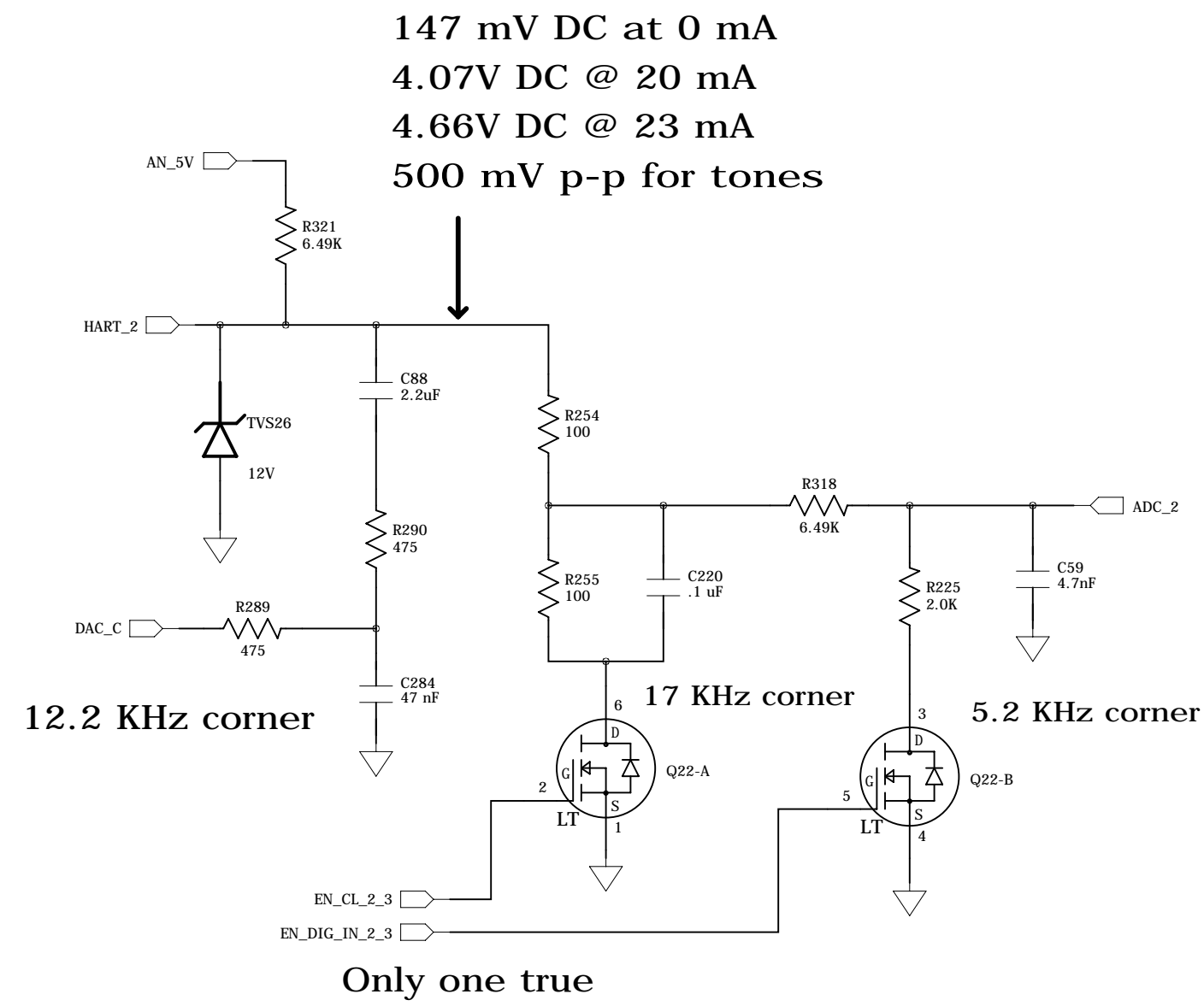
2200 Hz = Space



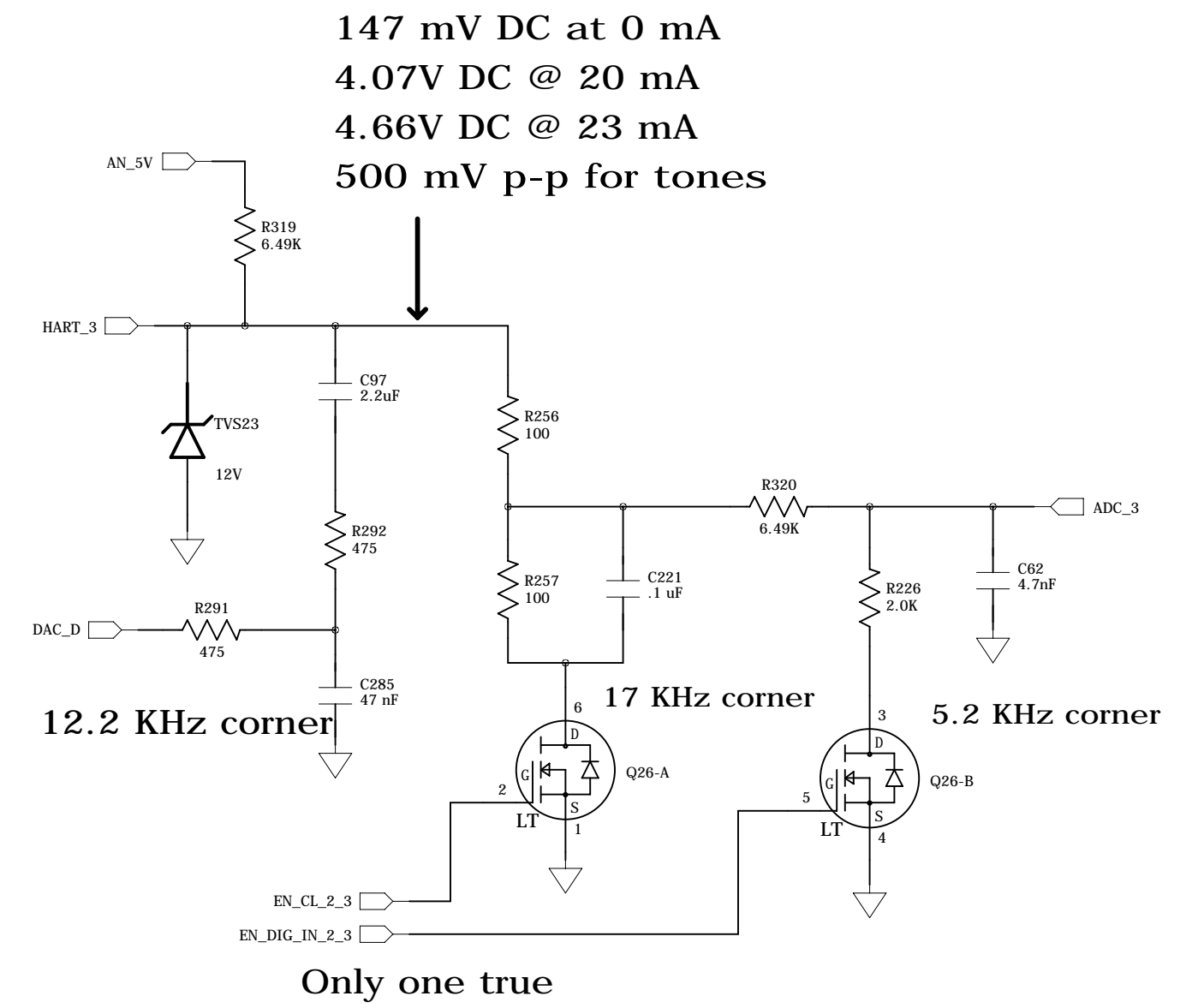
Used for Caller ID in NA

HART 2 & 3

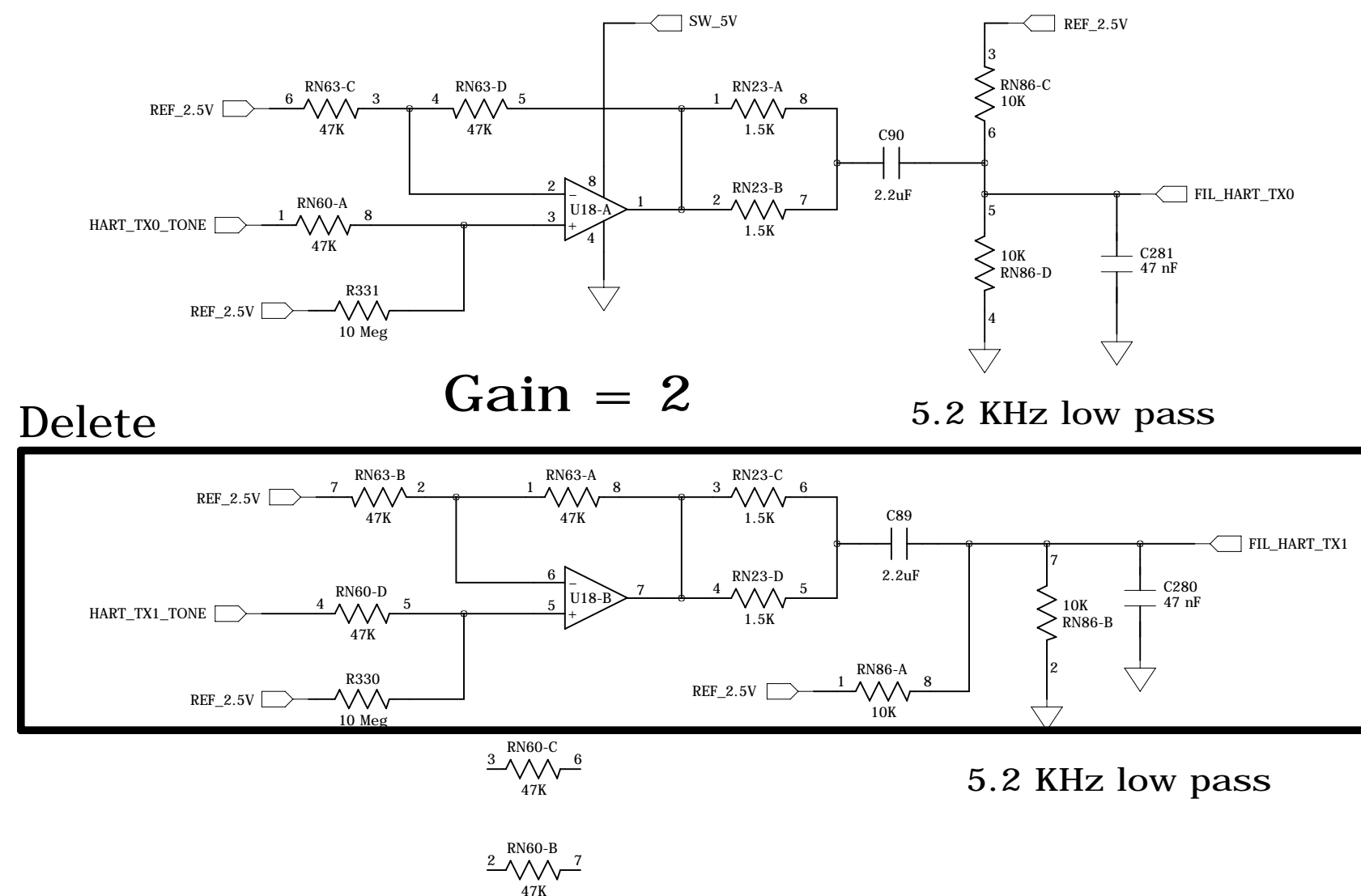
HART compatible 4-20 mA



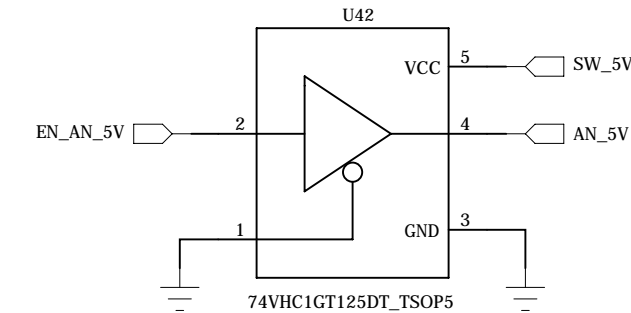
HART compatible 4-20 mA



TX_CL HART



Analog 5V

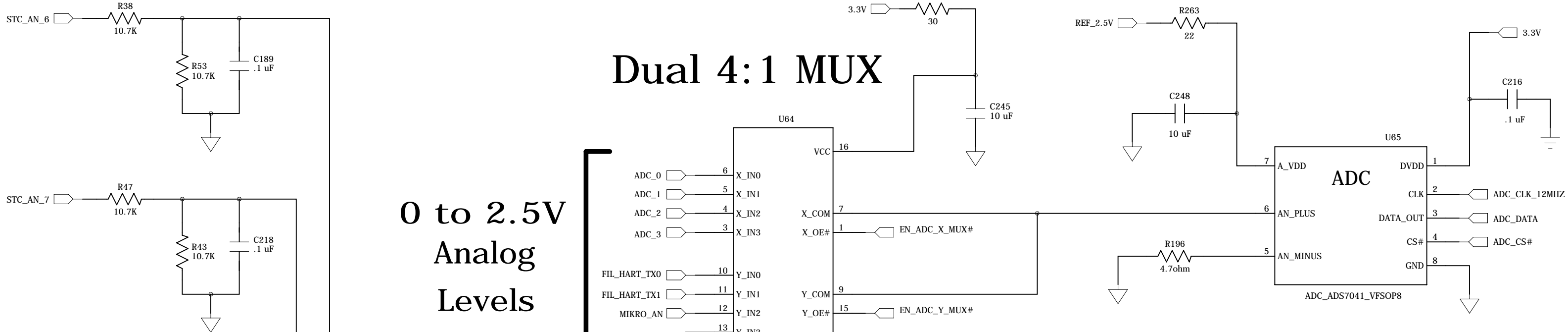


4 Channels of 8-bit DAC

6 Channels of 12-bit A/D

CH0 thru CH3 = 0-25 mA or 0-5V

10-bit A/D

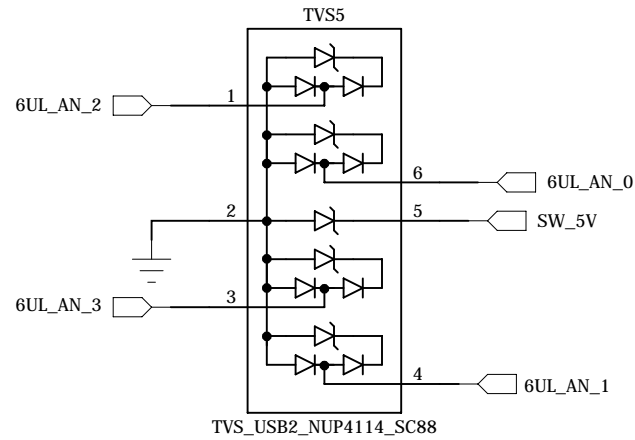


0 to 2.5V Analog Levels

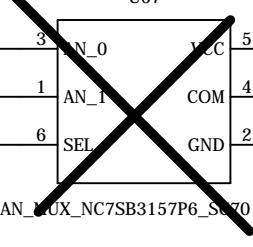
1 Mega-Sample/ sec.

Can get effective 12-bit resolution

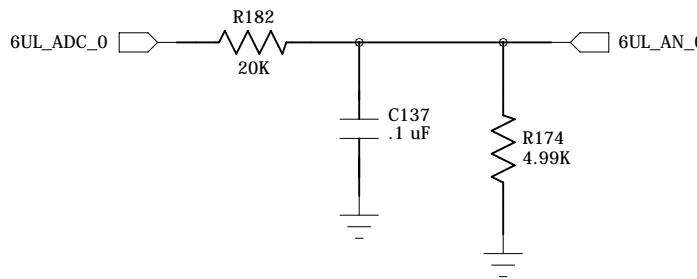
6UL_ADC TVS



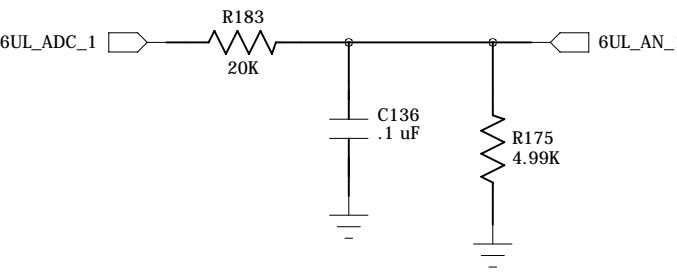
Remove



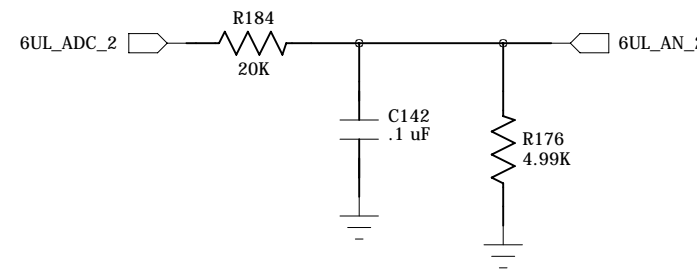
0-12.5V



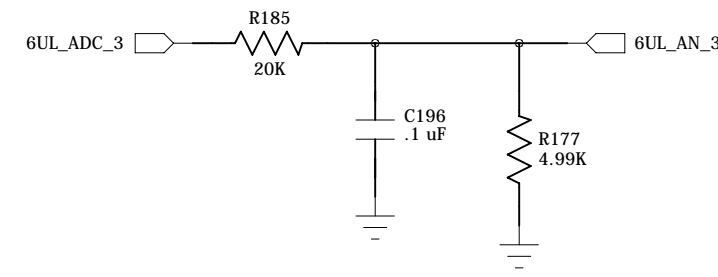
0-12.5V



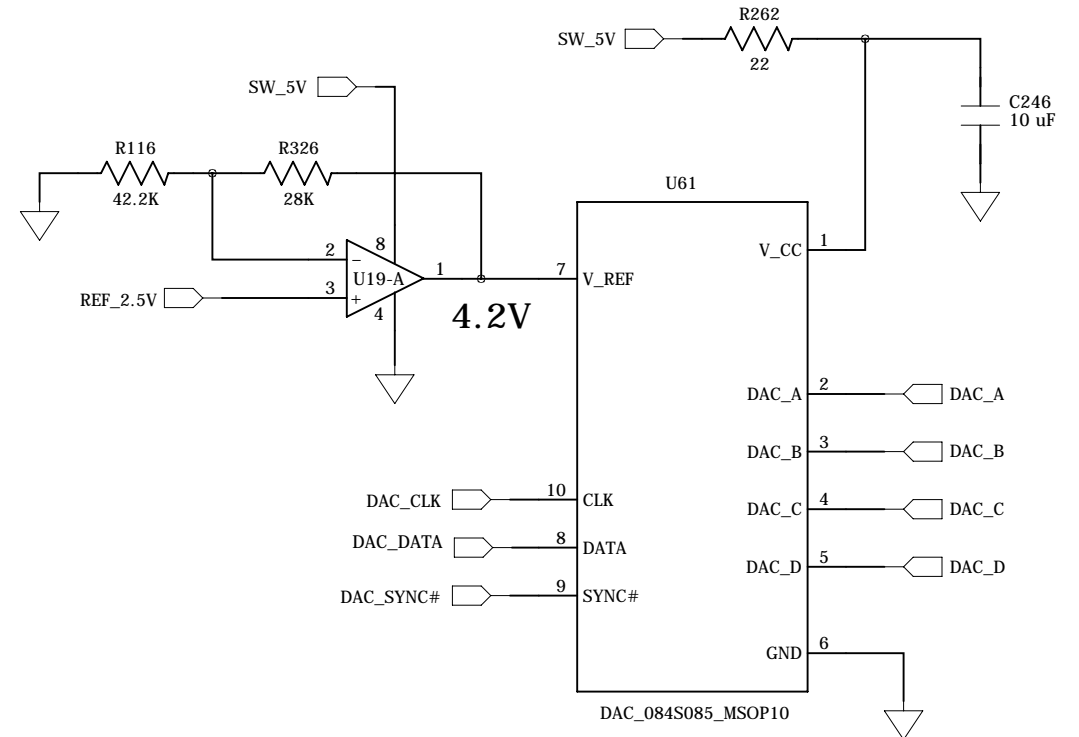
0-12.5V



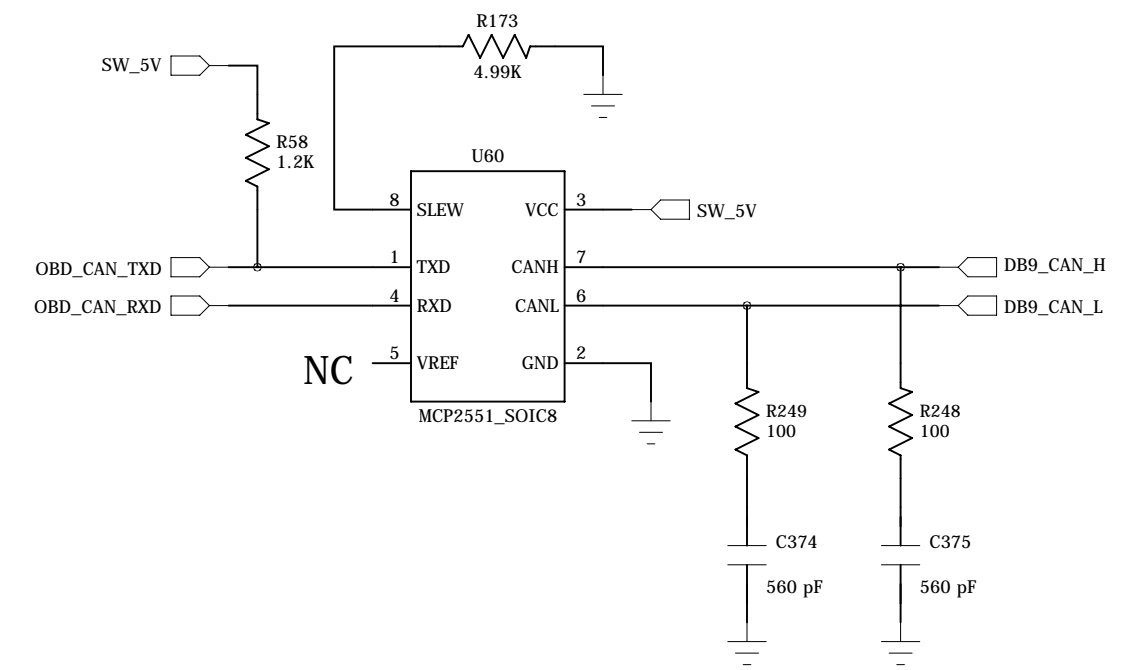
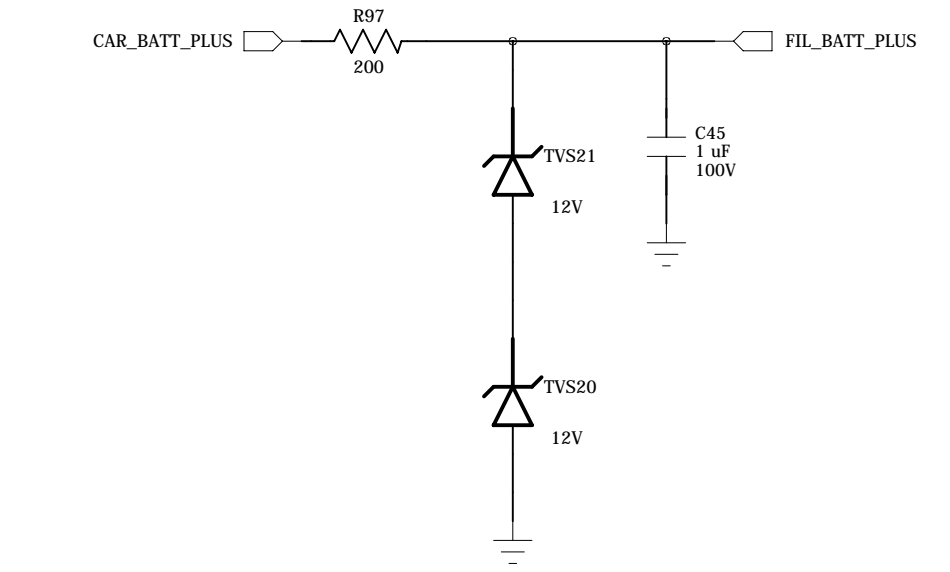
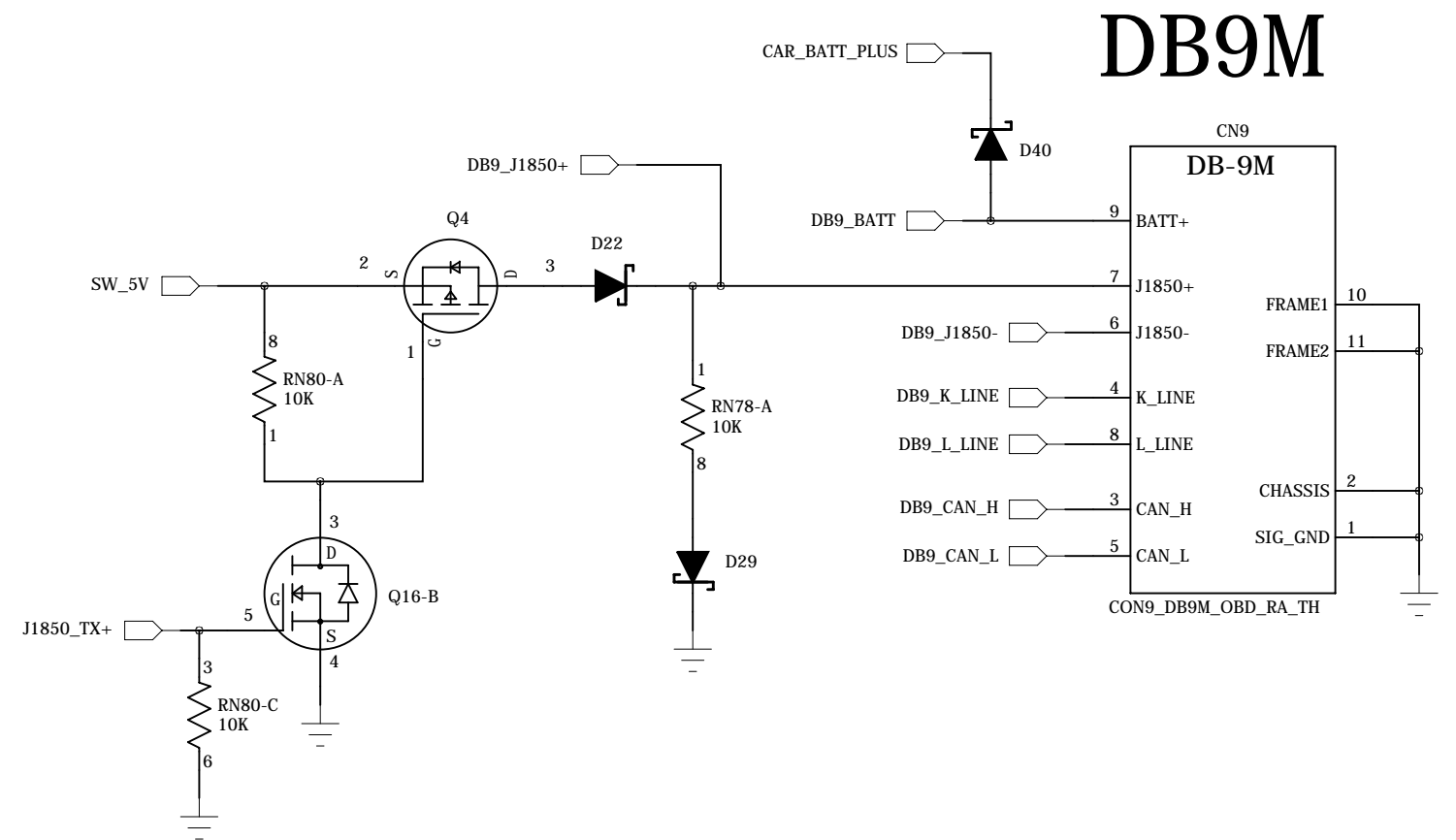
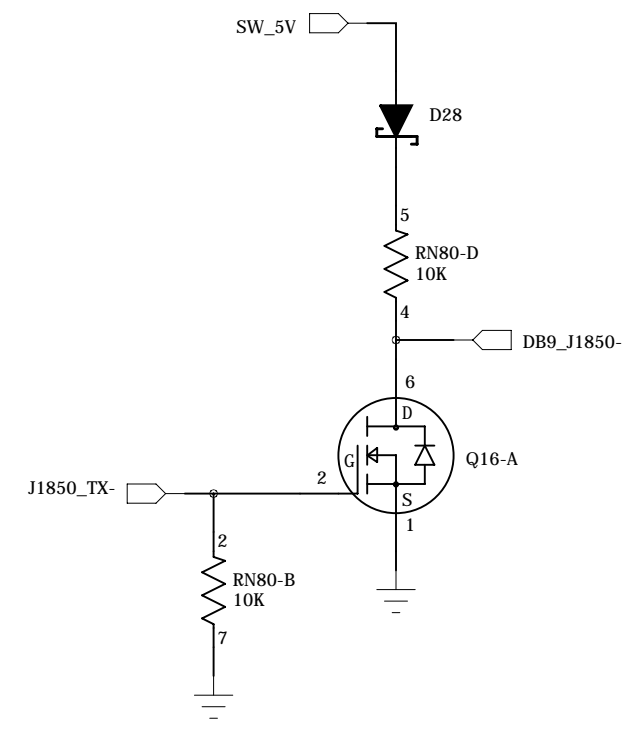
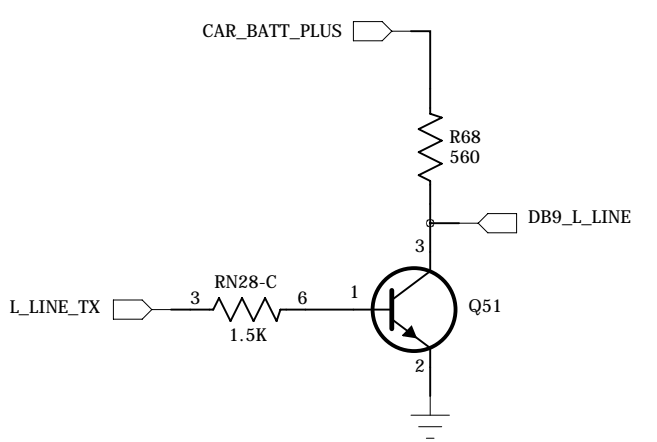
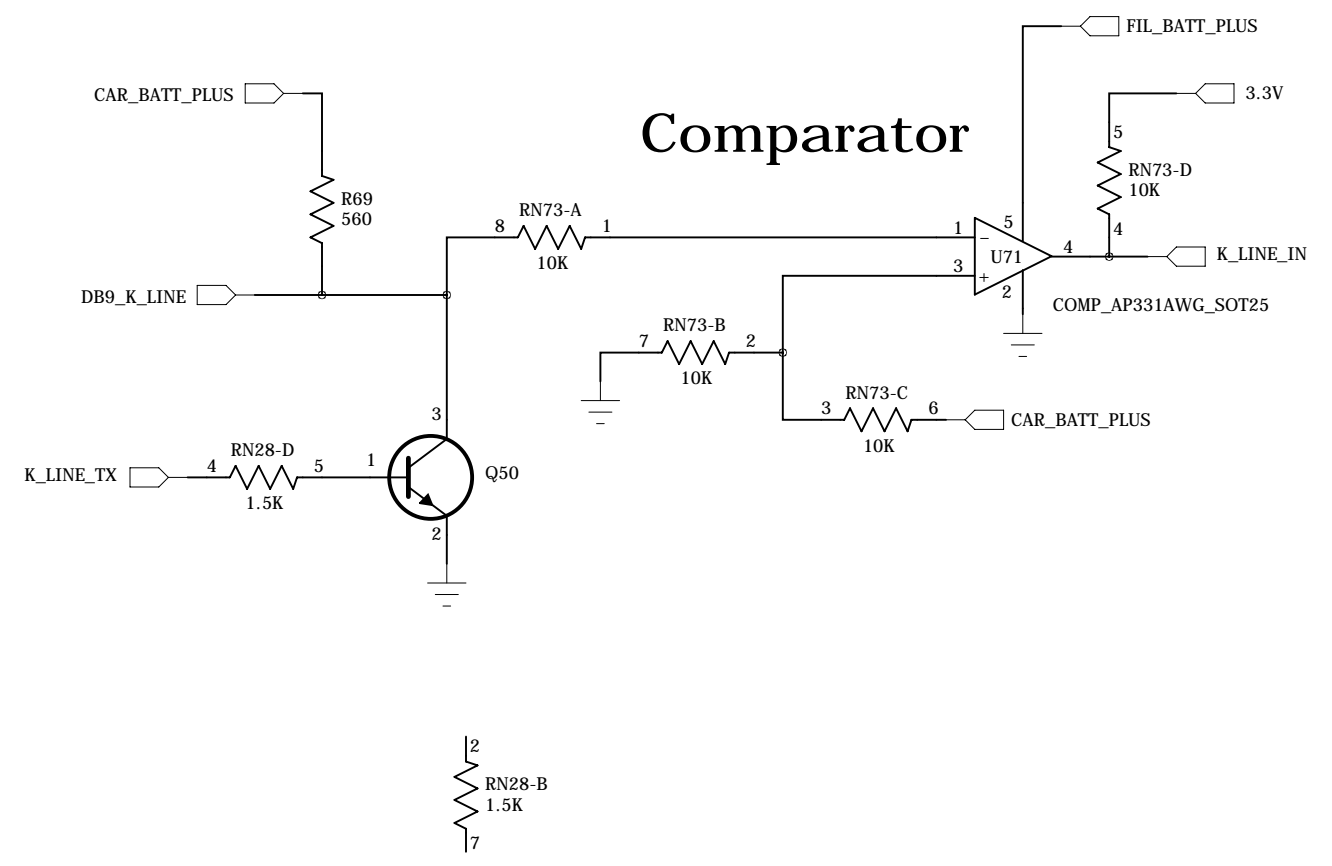
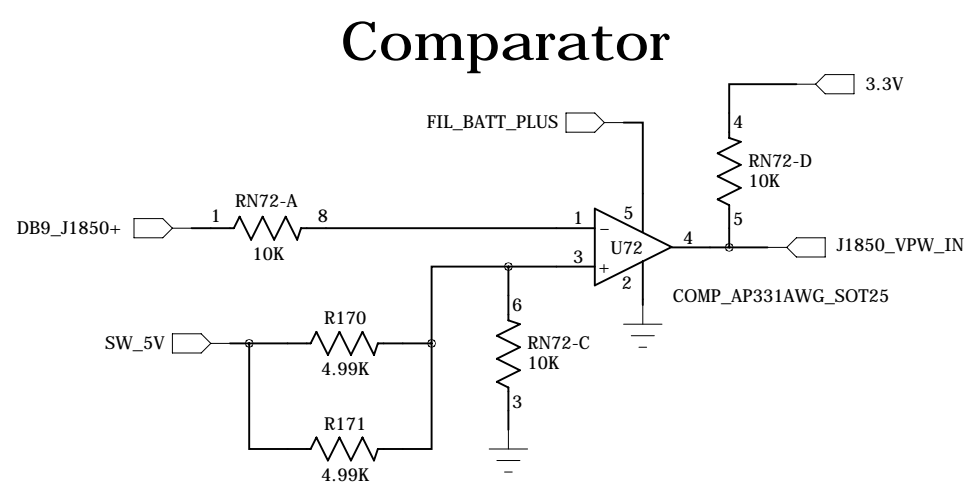
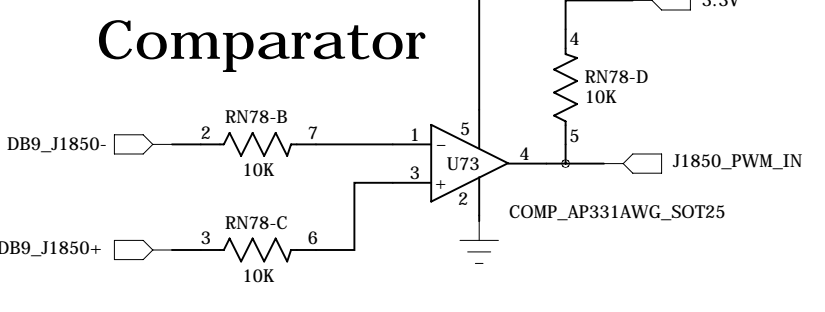
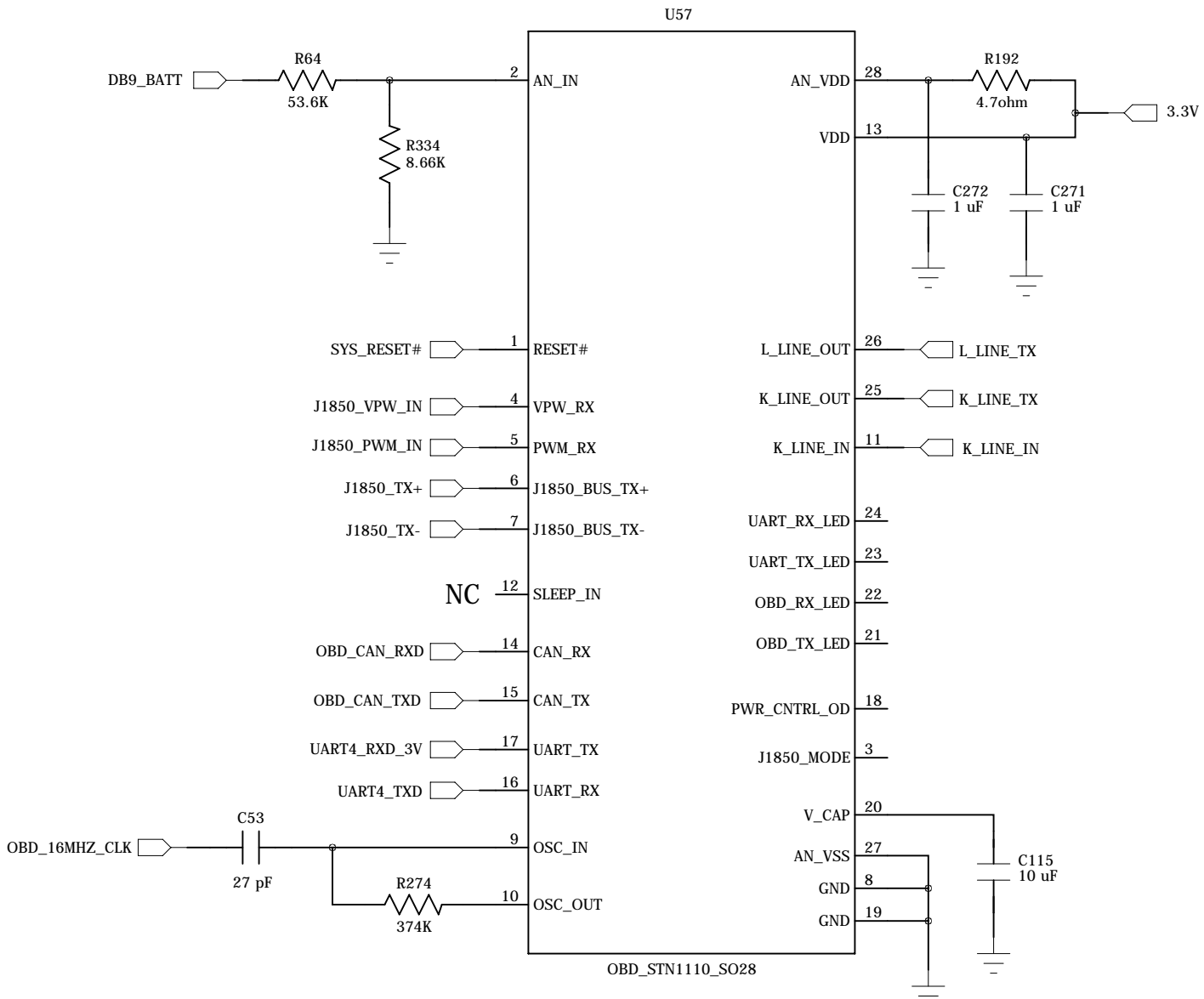
0-12.5V



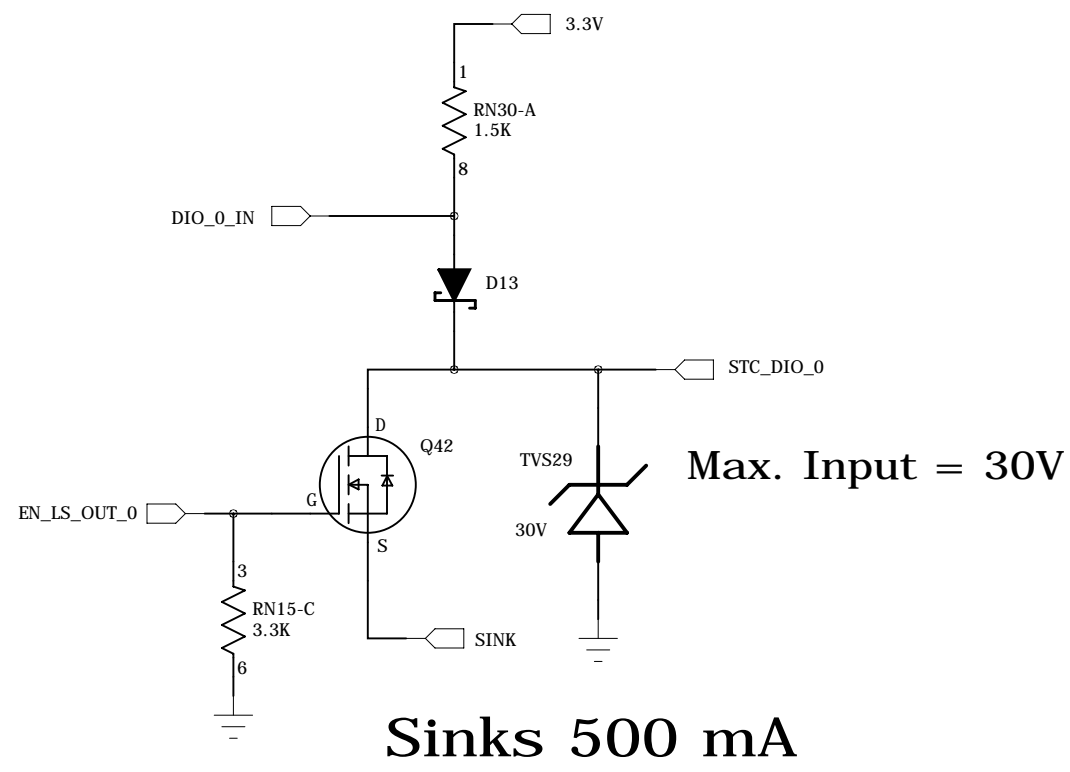
8-bit DAC



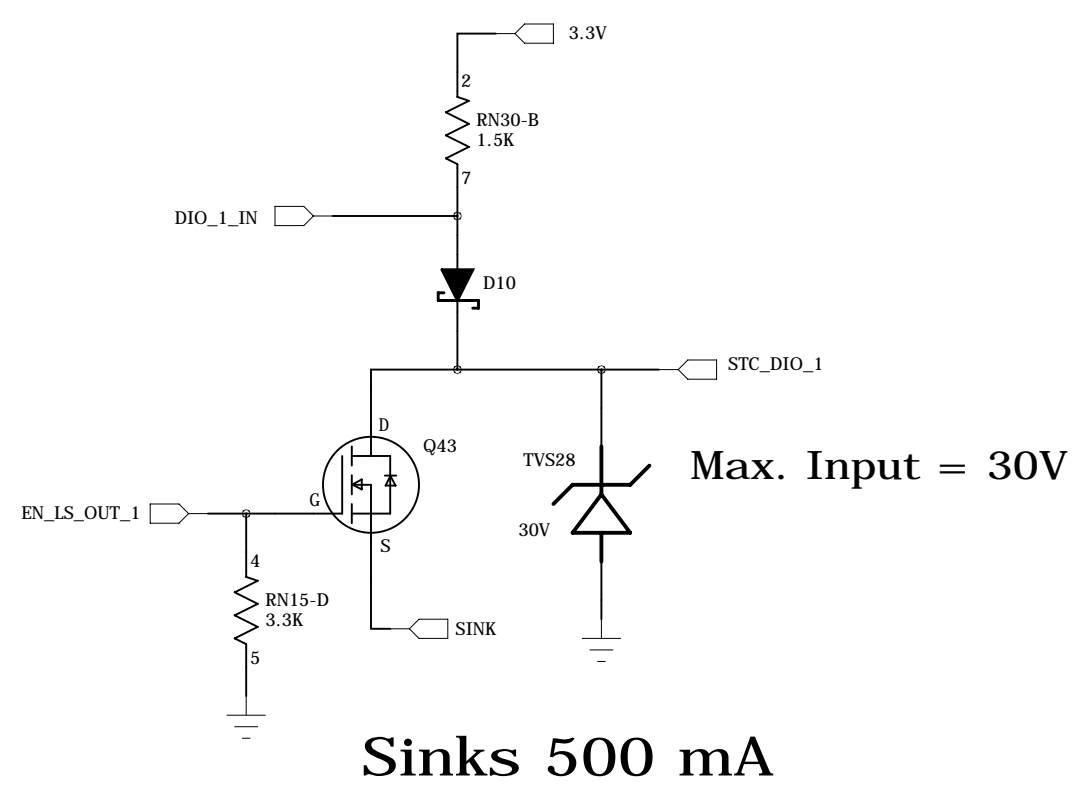
OBD Circuits



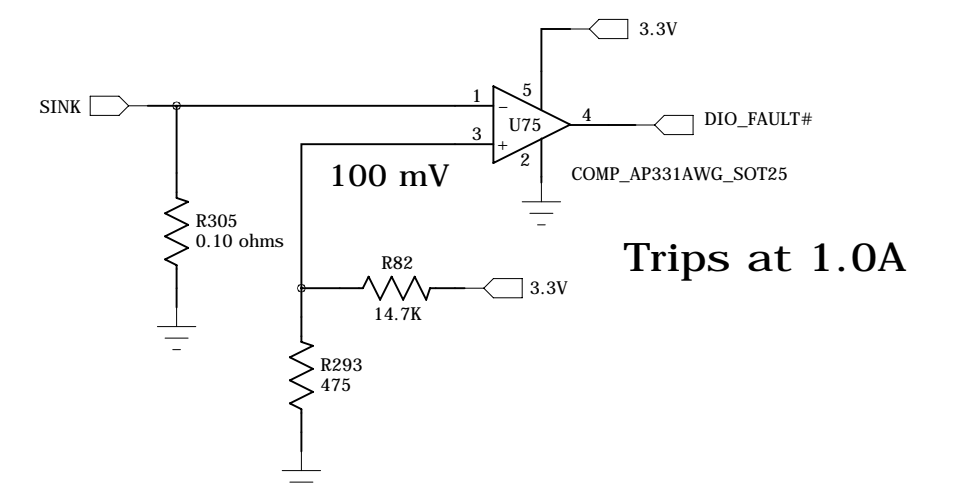
DIO_0



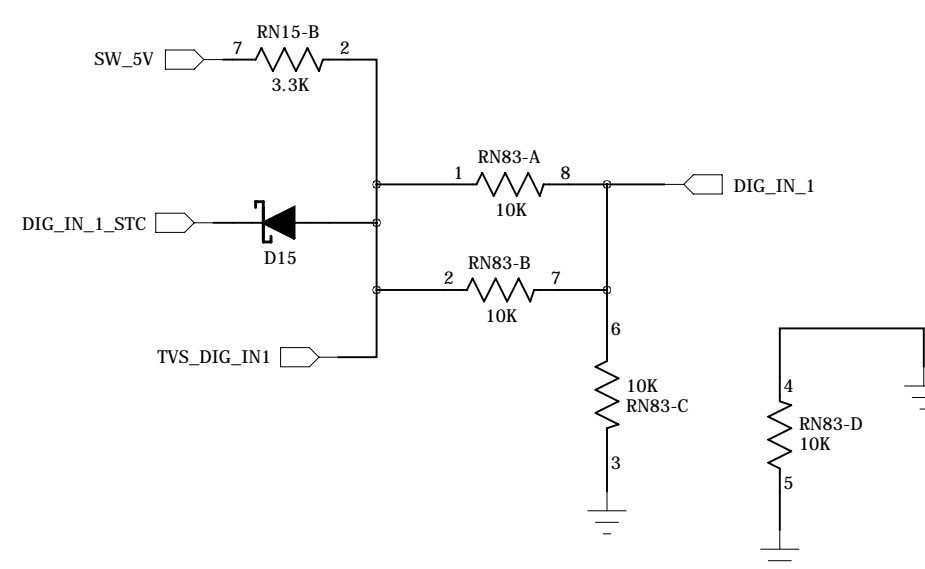
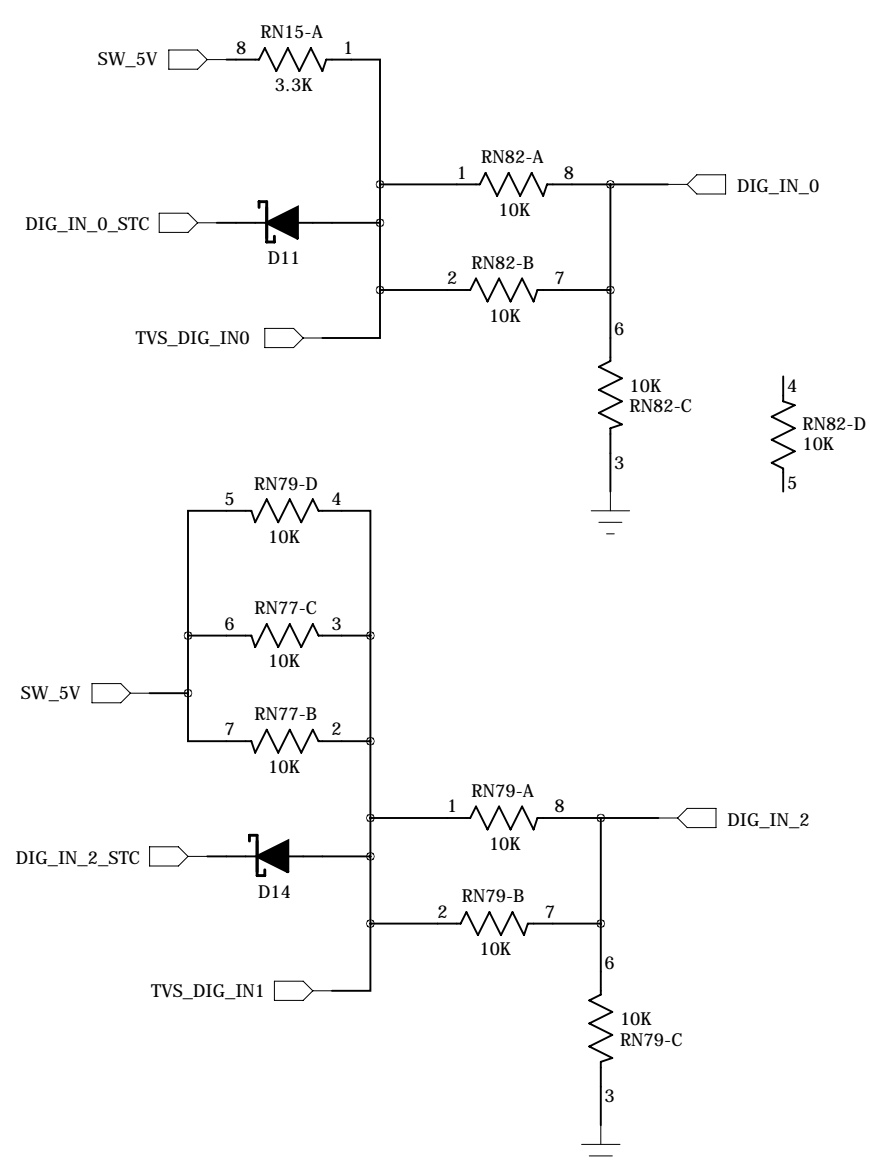
DIO_1



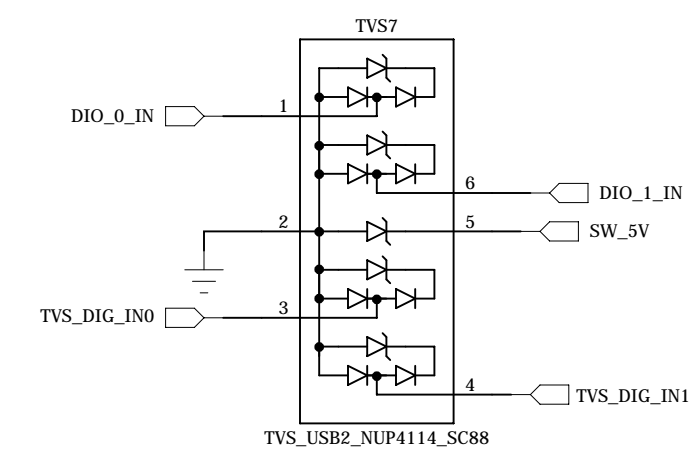
Comparator



Dig Inputs

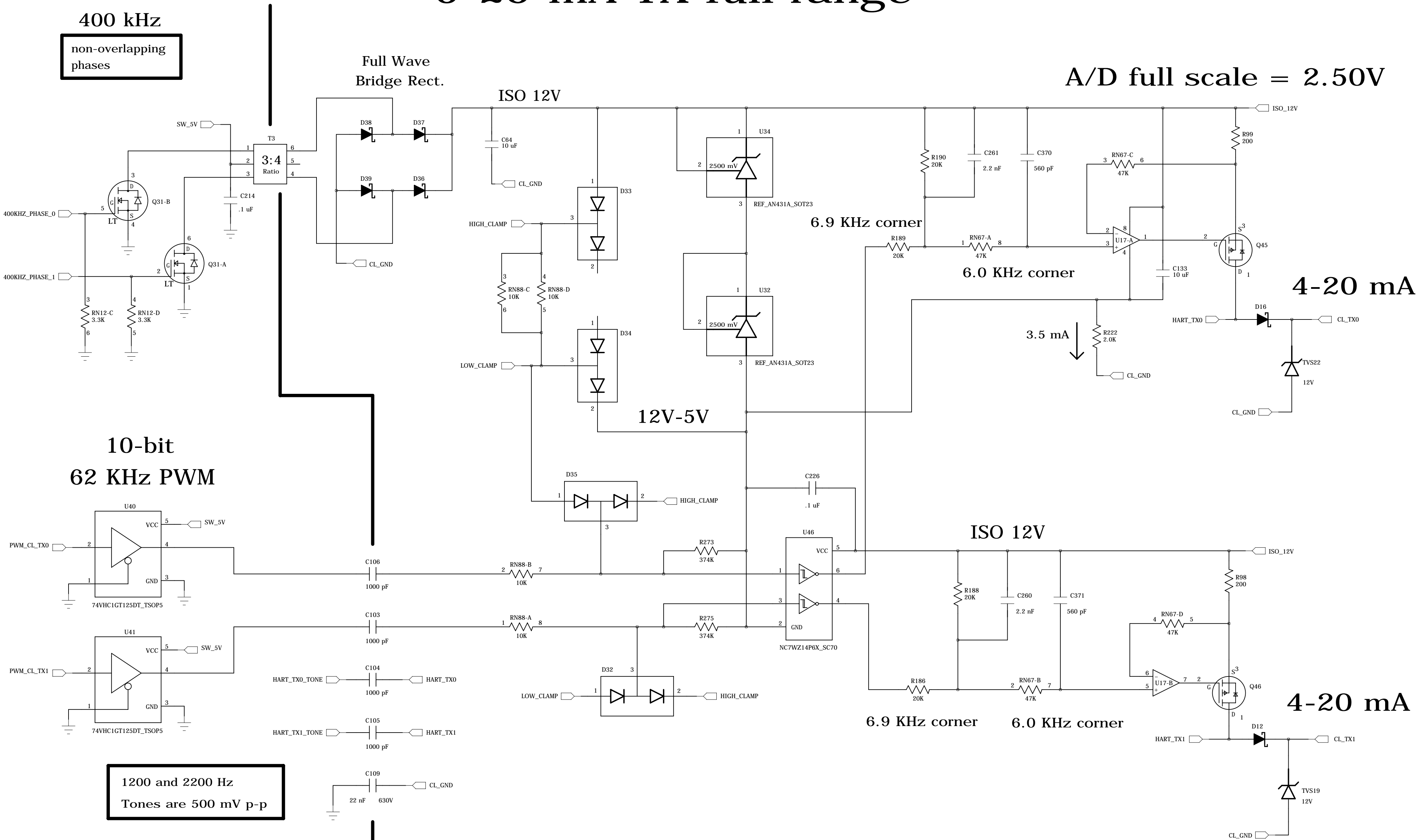


Dig IN TVS



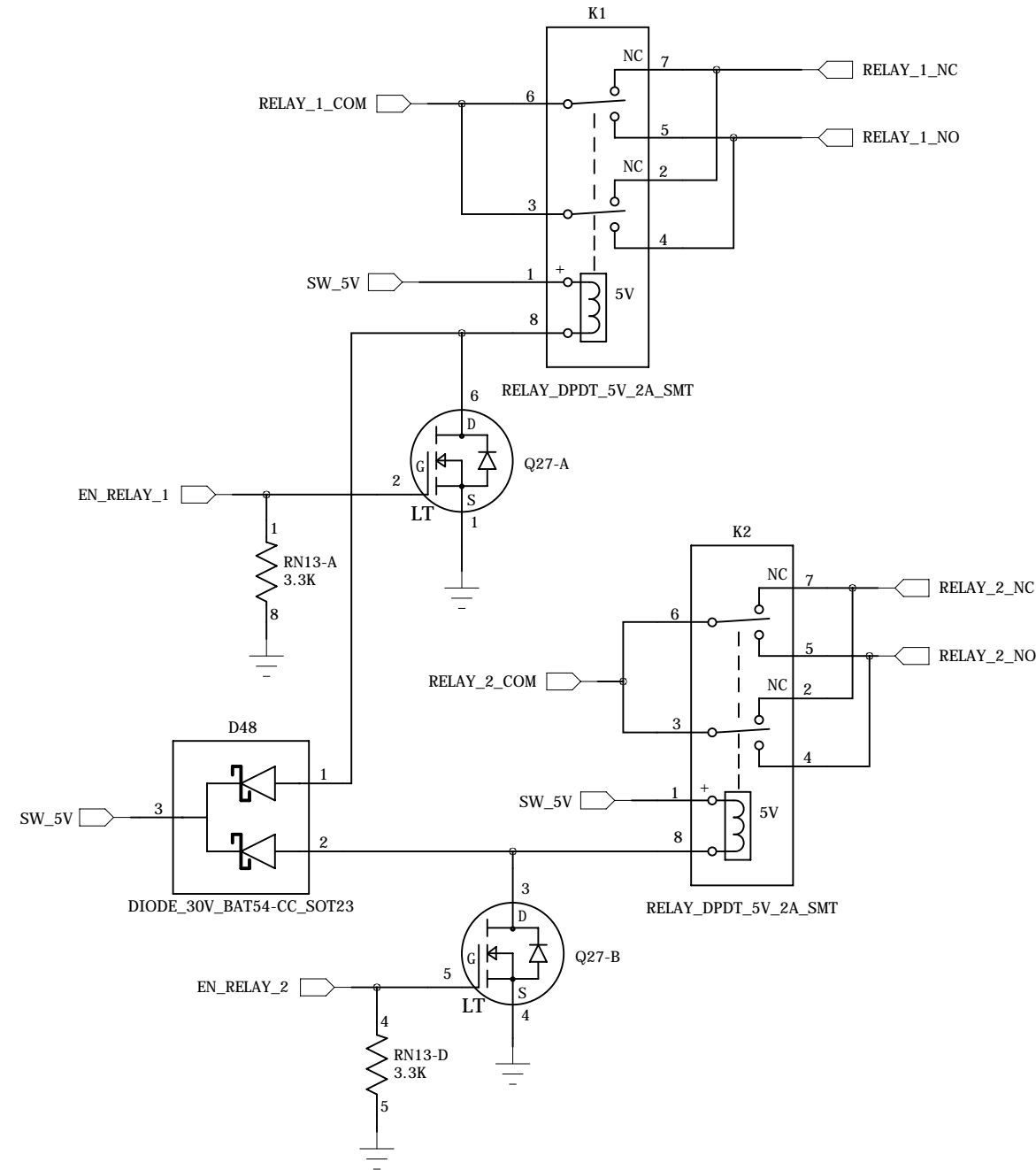
PWM --> 4-20 mA Current Loop Transmitters

0-25 mA TX full range

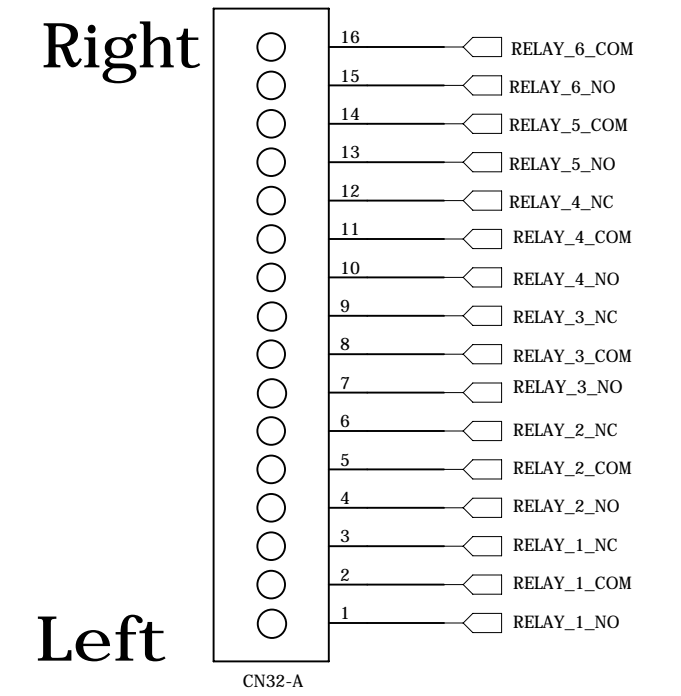


Relays

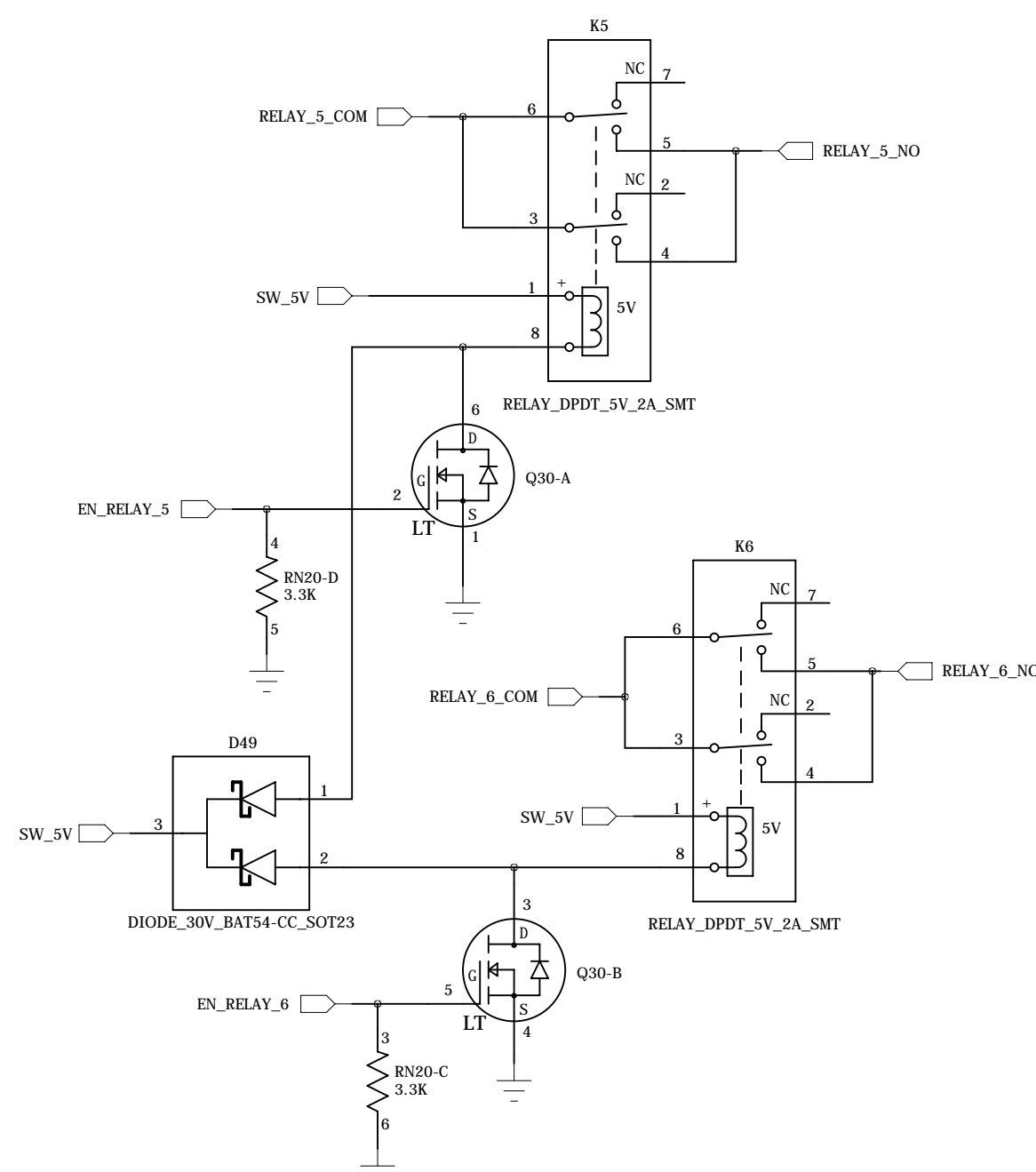
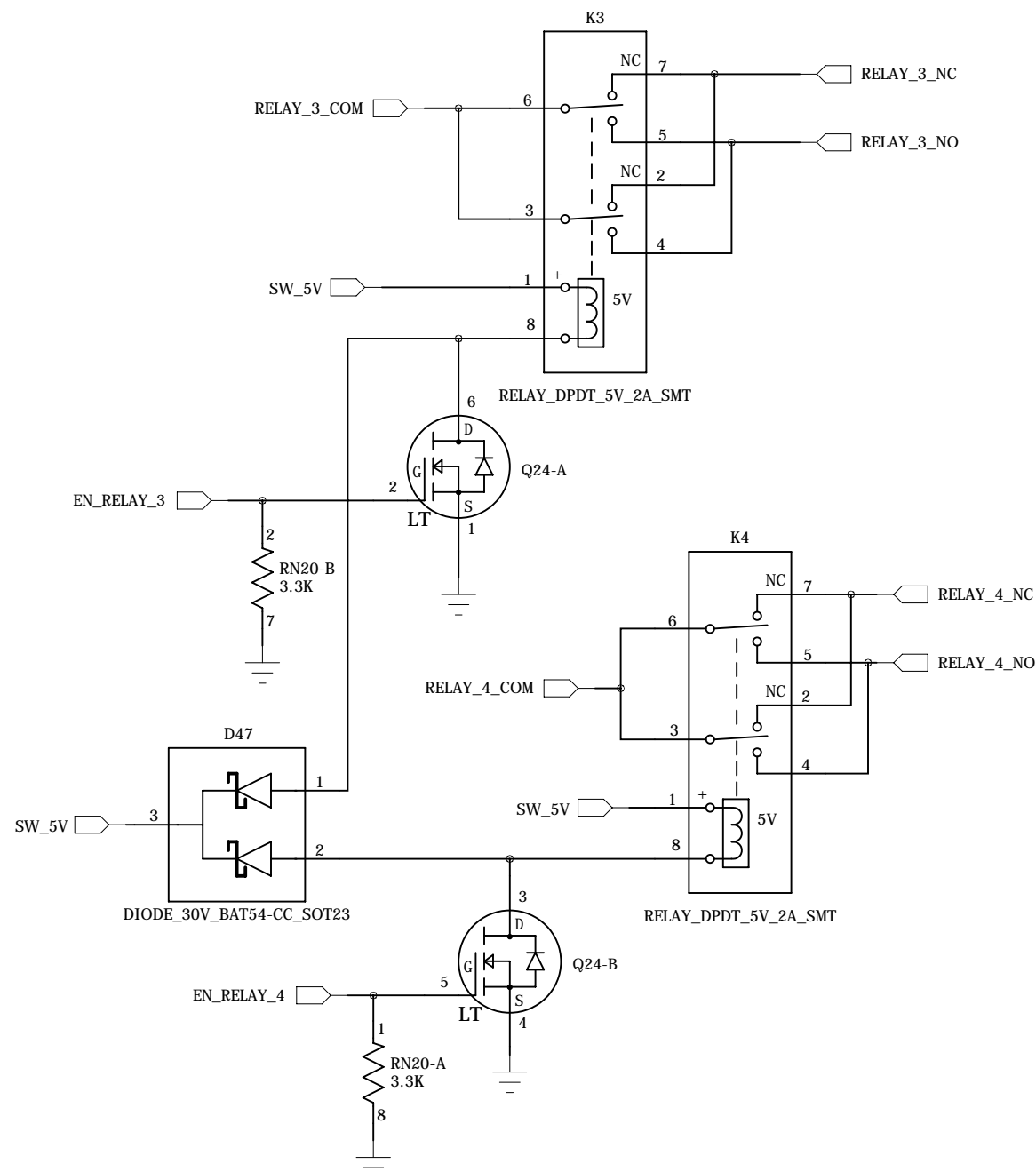
2 x 16 Screw Term. Positions



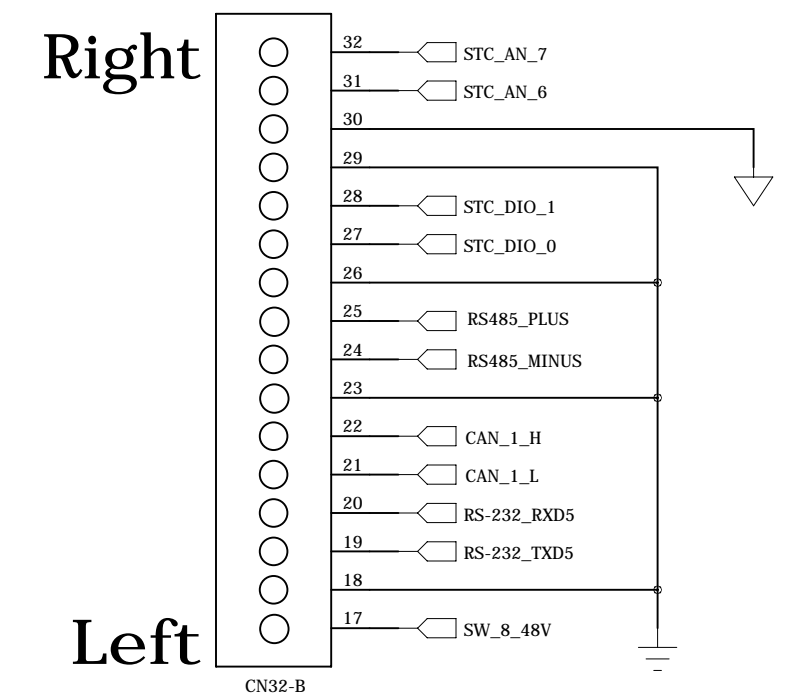
Top Row



Relays

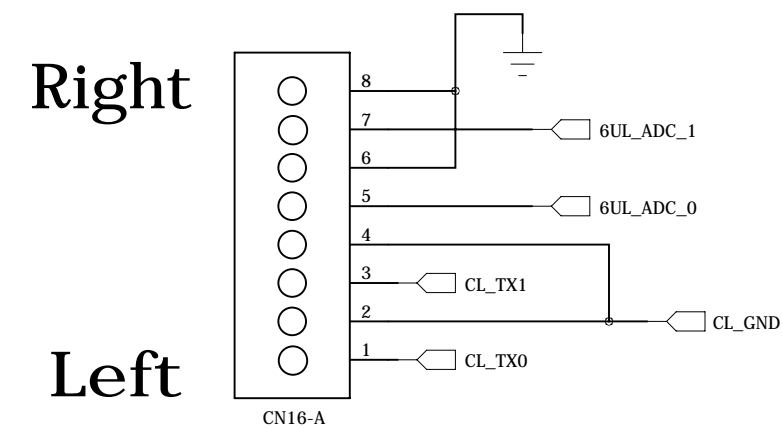


Bottom Row

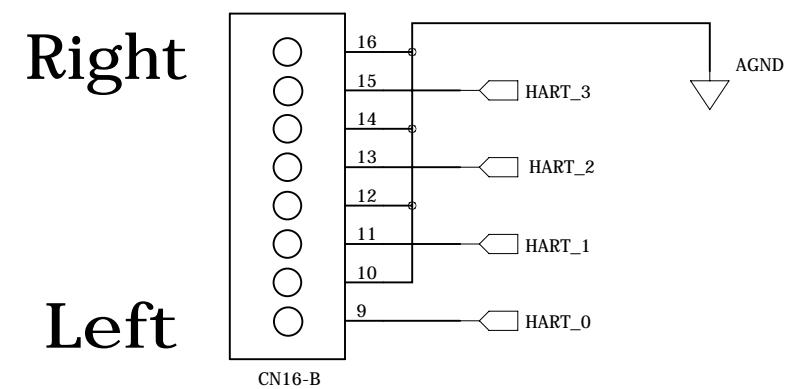


2 x 8 Screw Term.

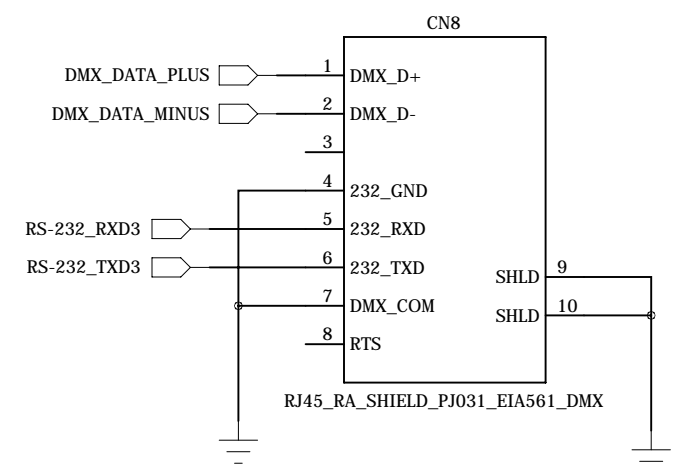
Top Row



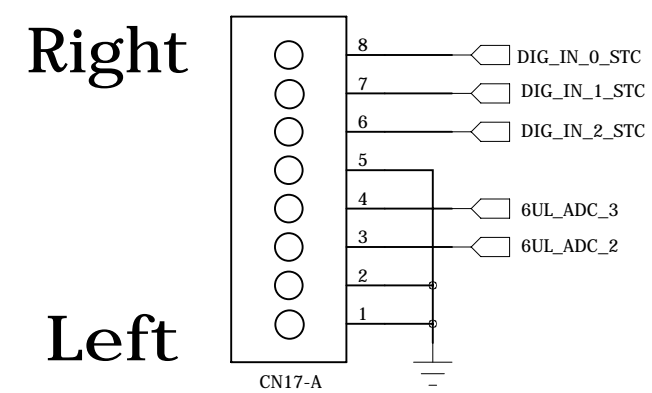
Bottom Row



DMX RJ45



Top Row



Bottom Row

