TS-7250-V2 Based on Marvell PXA166 or PXA168

Changes for Rev.A to B

Connected PC/104 "B9" (12V pin) to VIN

Connected PC/104 "B3" pin to 5V

Removed FB17

Changed Full-size SD card socket to new OST

Changed BGX50 TVS devices to new NUP4114

Changed M0 to SiLab uC

Added pull-down resistors on IRQ5 thru IRQ7

D6 not populated by default

Did not change to 153 ball eMMC - not tested yet

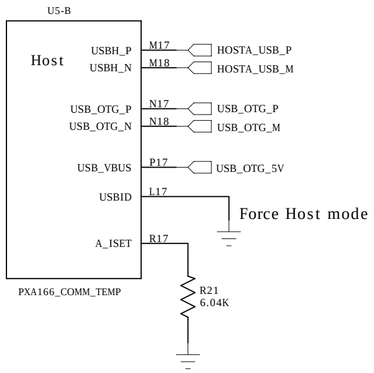
JP4# now readable on FPGA ball "M6"

Web Schematic: Some proprietary information has been withheld.

Technologic Systems		Date June 13, 2015
Title: TS-7250_V2 Marvell PXA166 or PXA168		
Rev: B	Designer	Sheet 0 of 16

PXA166 or PXA168

USB Ports

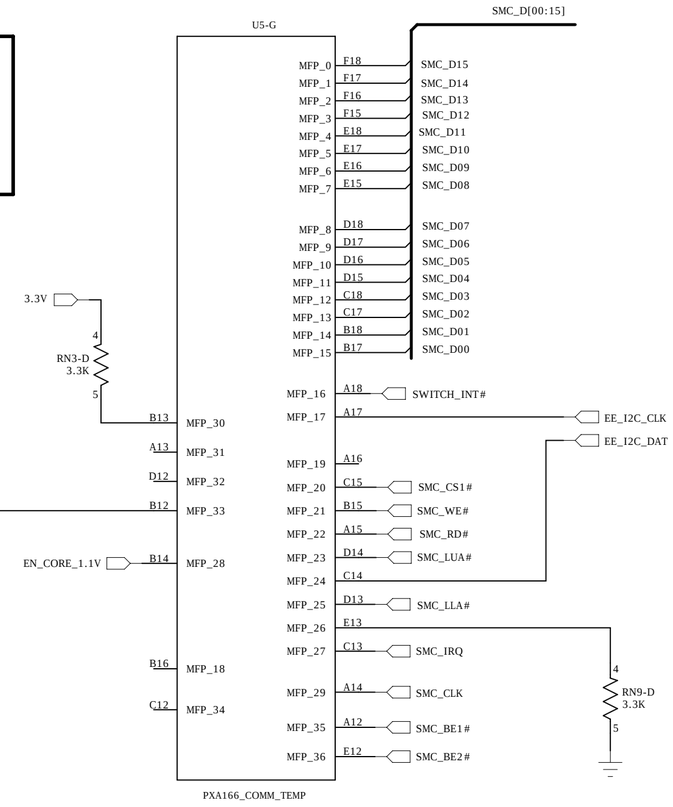


Board ID

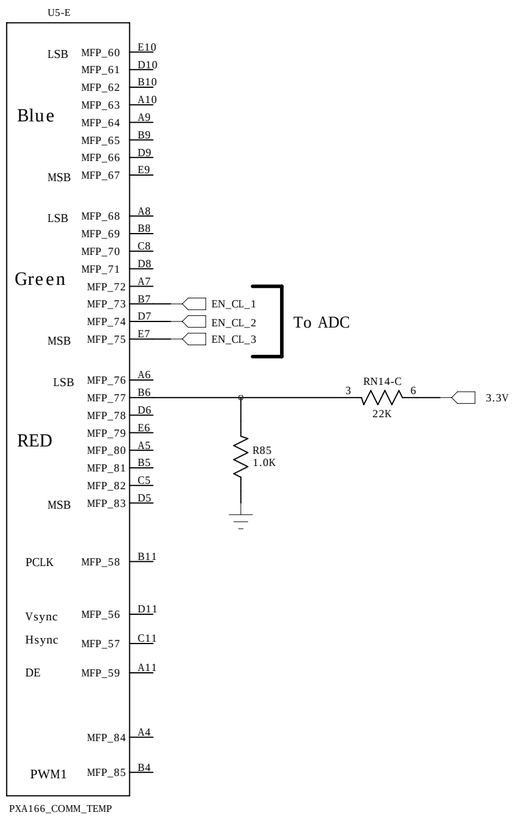
	MFP_26	MFP_30	MFP_33
TS-7250_V2	0	1	0
TS-7800_V2	1	1	1
TS-xxxx	0	0	0

Requires MFP to be Inputs

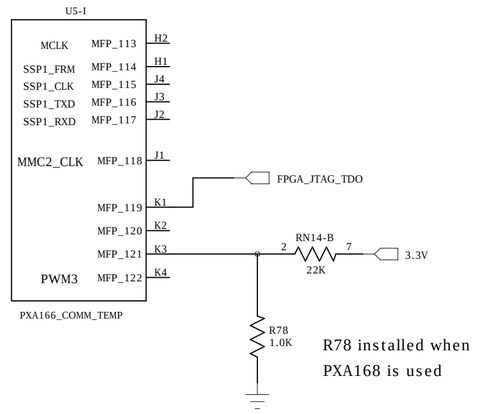
SMC Bus



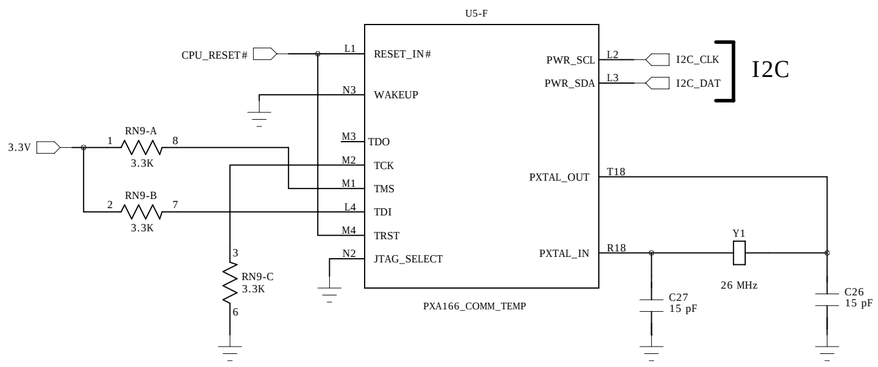
LCD



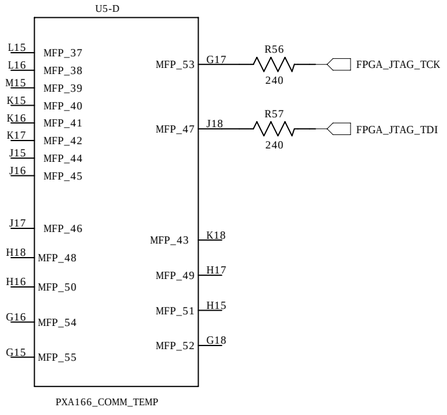
I2S



Control



Camera



U5 = PXA166 Commercial Temp

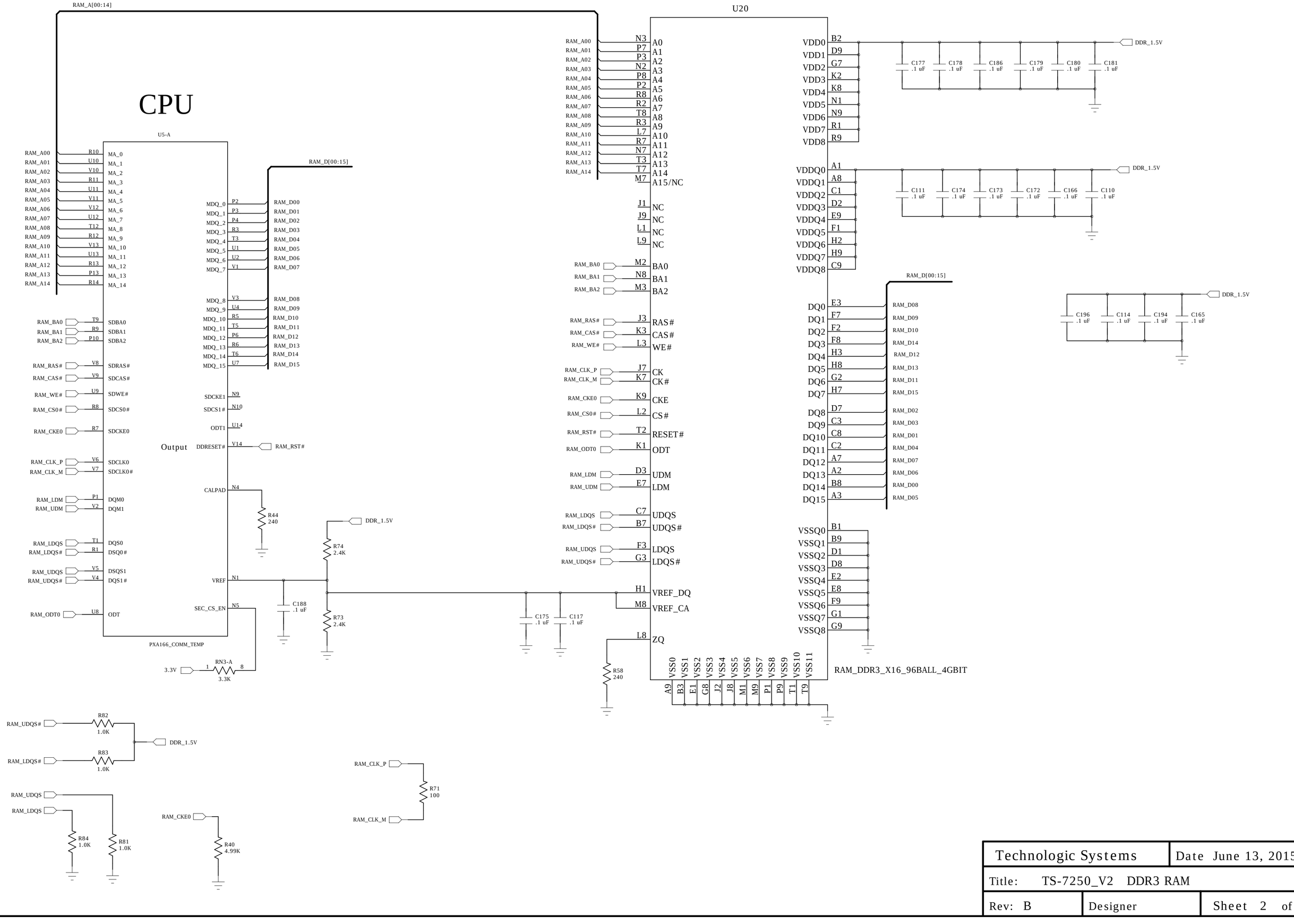
or = PXA168 Industrial Temp

Technologic Systems	Date June 13, 2015	
Title: TS-7250_V2 Marvell PXA166 or PXA168		
Rev: B	Designer	Sheet 1 of 16

DDR3 256Mx16 RAM

4 Gbit RAM chip

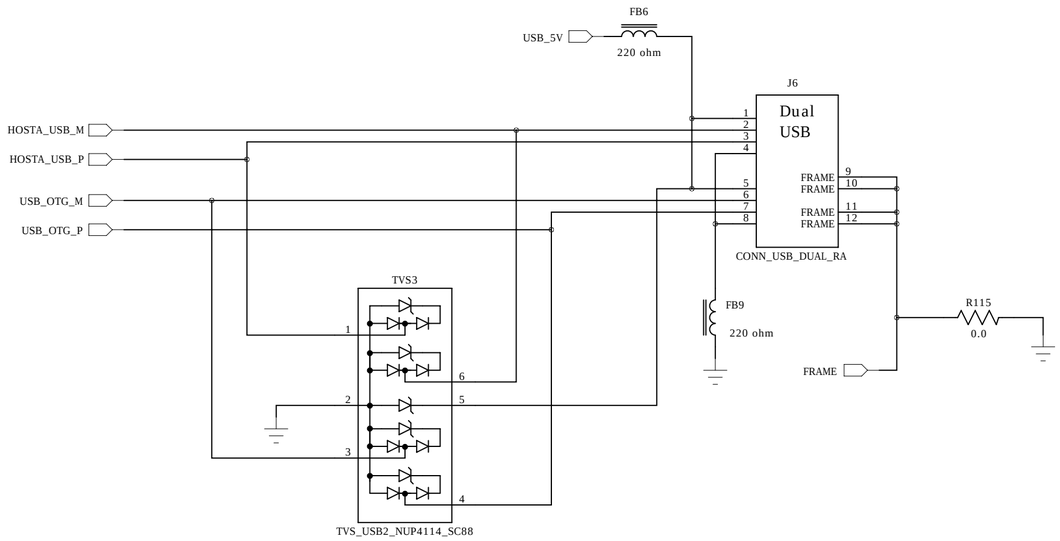
512 MB RAM



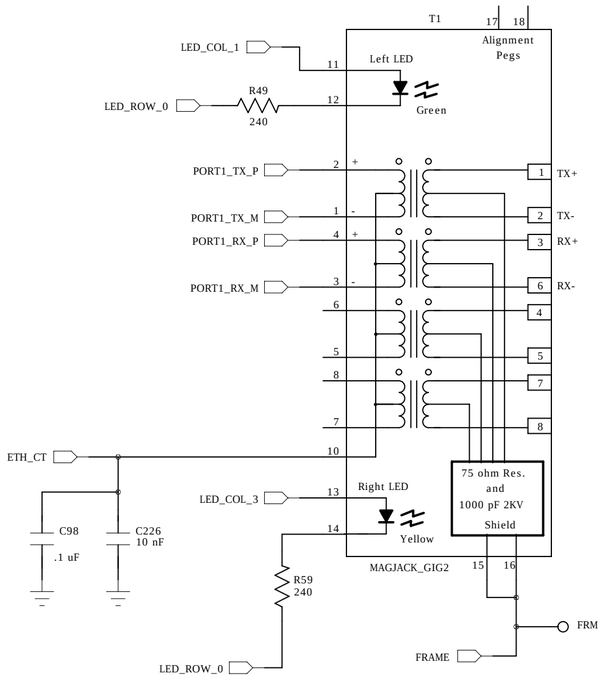
Technologic Systems	Date June 13, 2015	
Title: TS-7250_V2 DDR3 RAM		
Rev: B	Designer	Sheet 2 of 16

Off-Board Connectors

Dual Host USB Ports

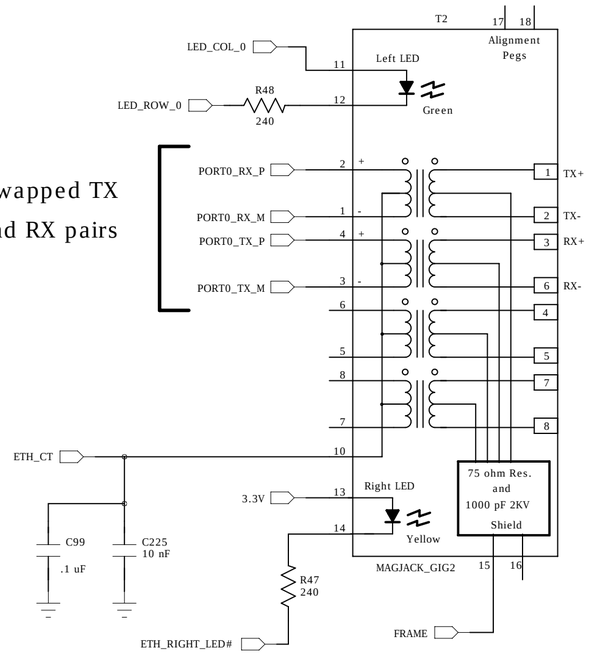


Primary MagJack



Second MagJack

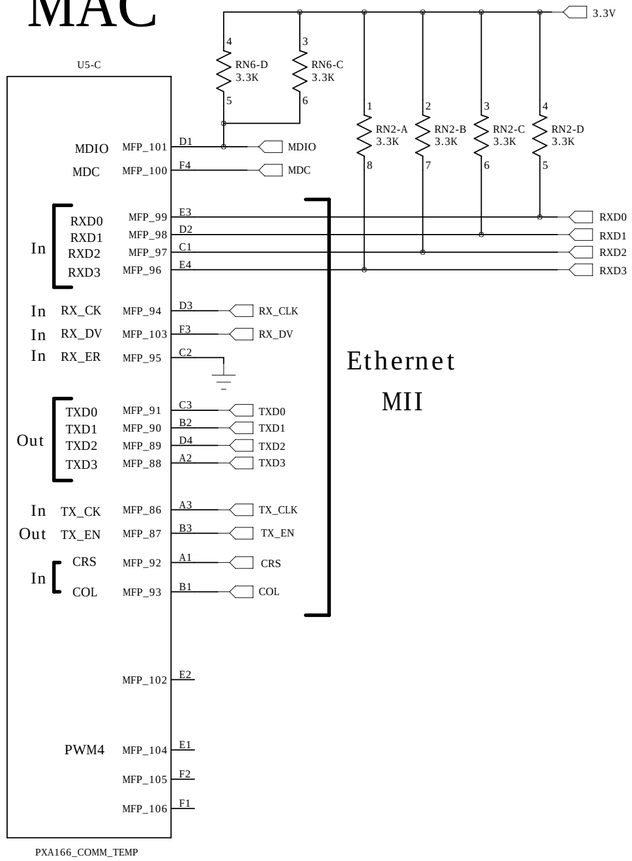
Swapped TX
and RX pairs

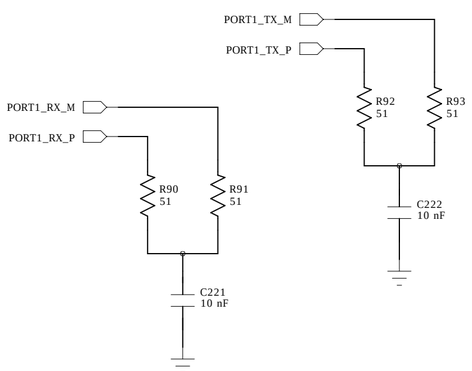


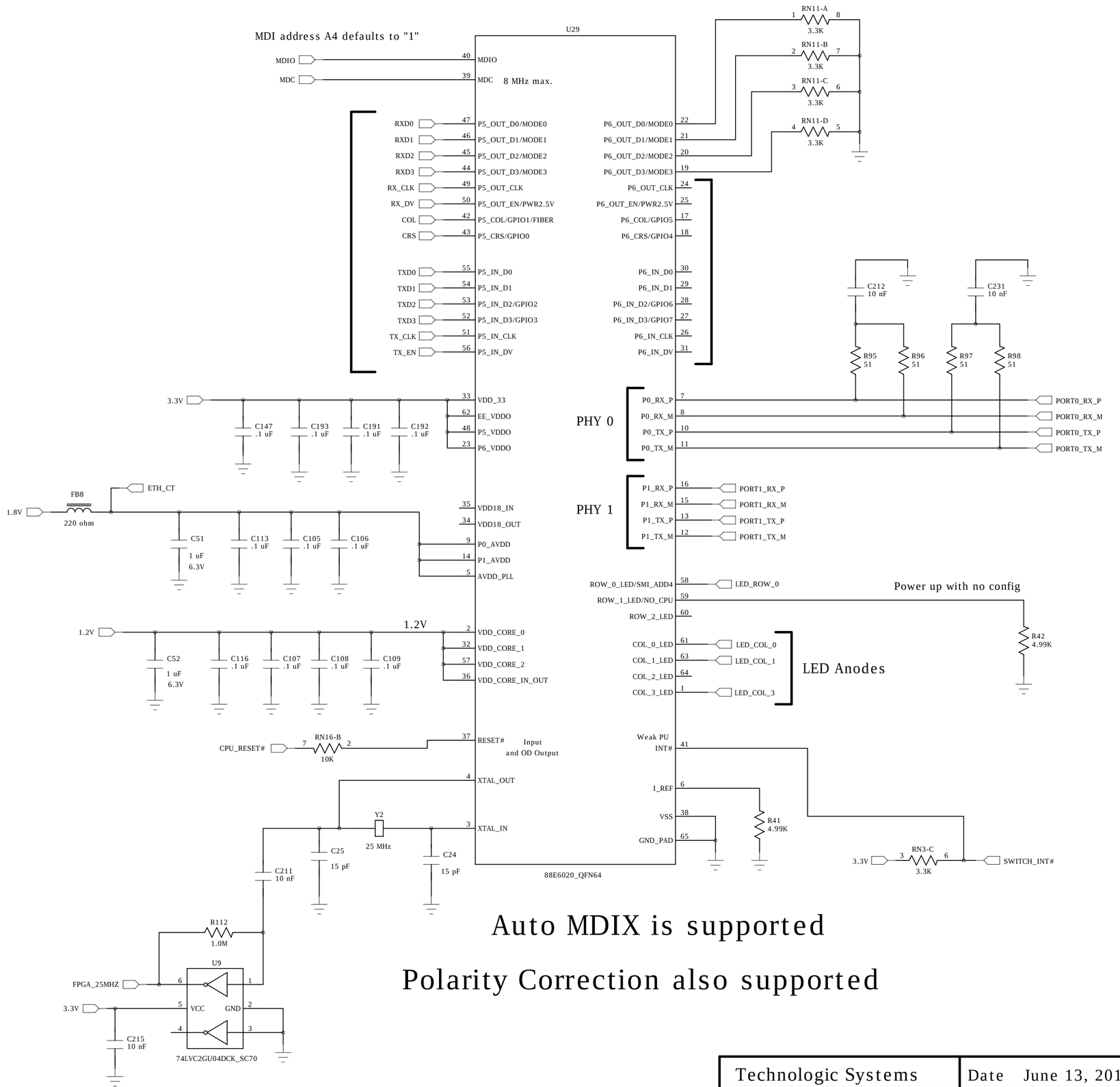
Technologic Systems		Date June 13, 2015
Title: TS-7250_V2 Ethernet Magjacks		
Rev: B	Designer	Sheet 3 of 16

10/100 Ethernet 4-Port Switch

CPU MAC





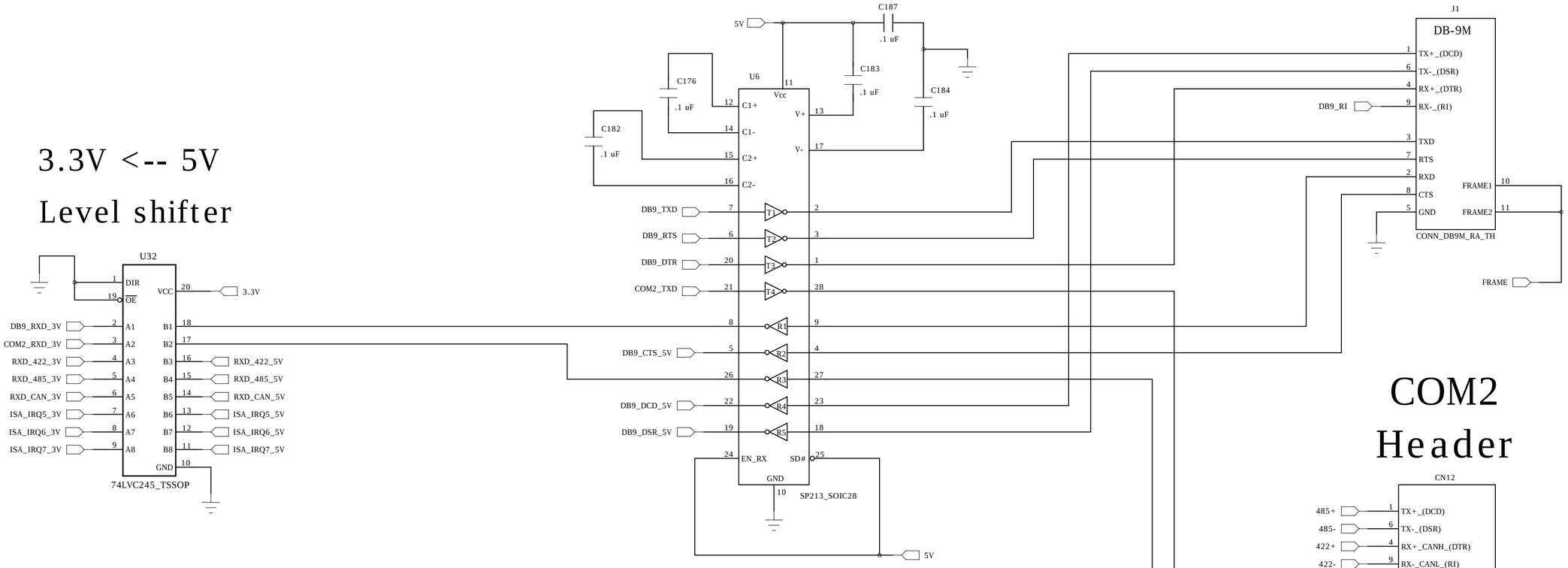


Auto MDIX is supported

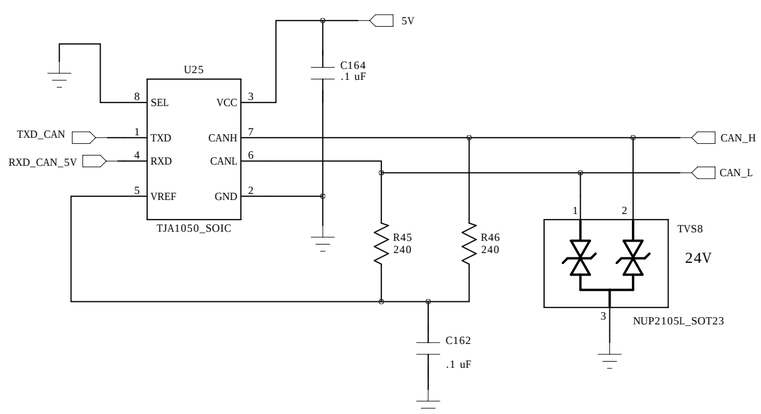
Polarity Correction also supported

Technologic Systems	Date June 13, 2015	
Title: TS-7250_V2 Ethernet Switch		
Rev: B	Designer RLM	Sheet 4 of 16

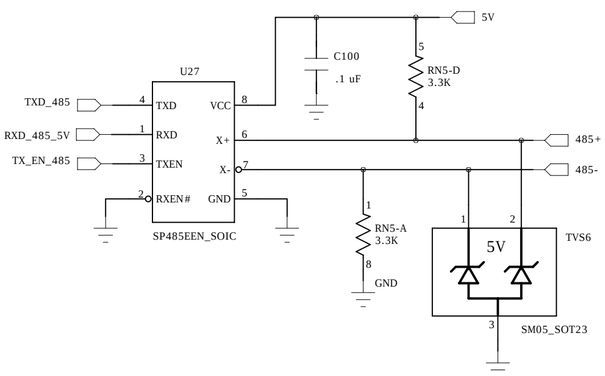
RS-232 Transceiver



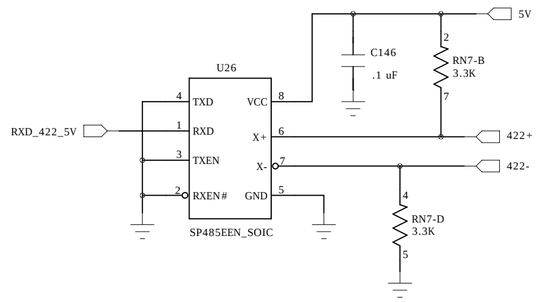
CAN Tranceiver



RS-485 Transceiver

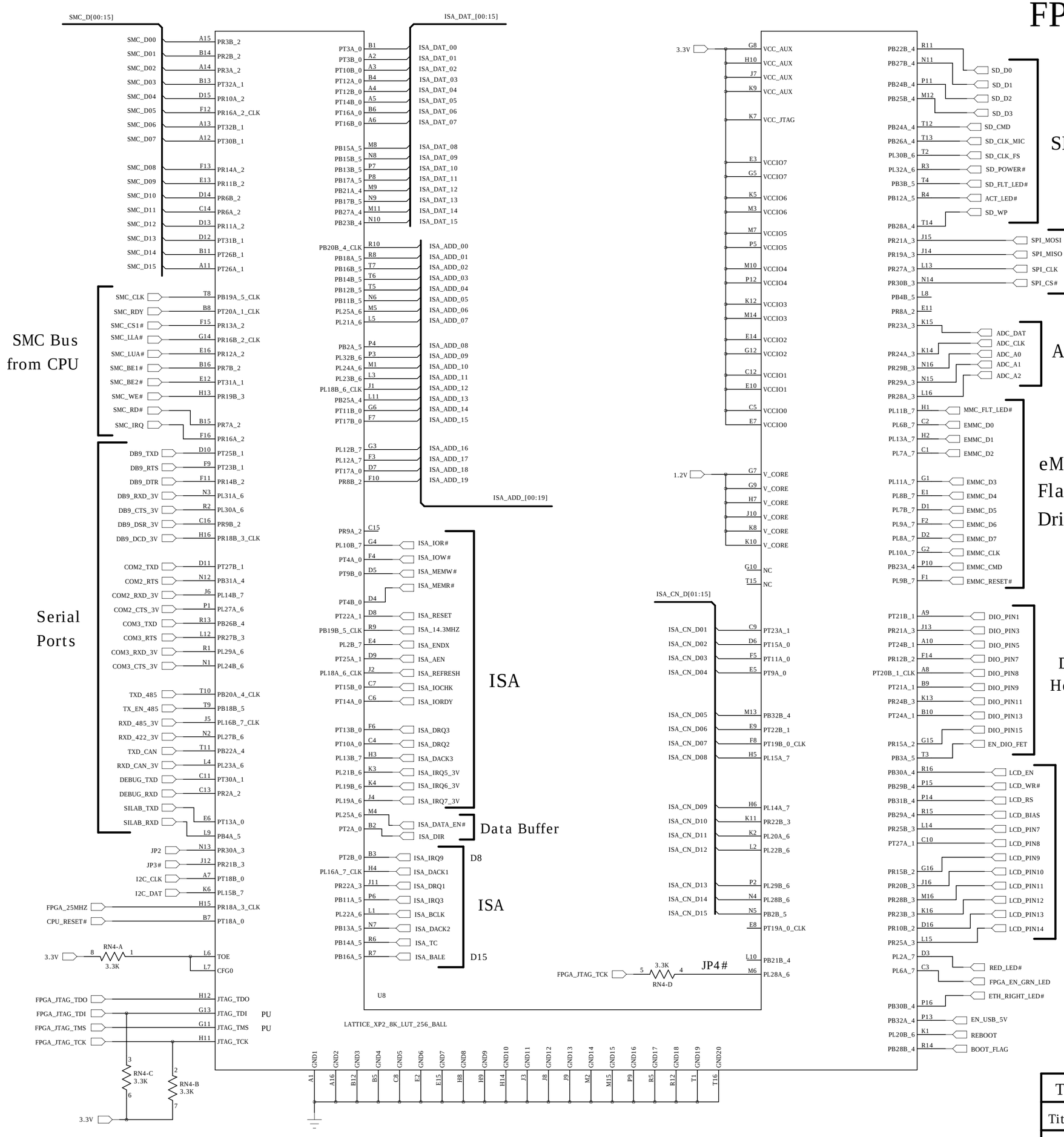


RS-422 Receiver



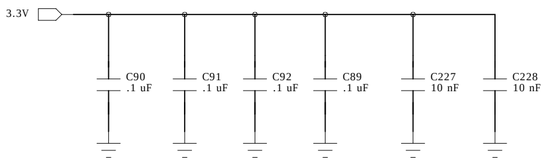
Technologic Systems	Date June 13, 2015	
Title: TS-7250_V2 COM Ports, CAN, RS-485		
Rev: B	Designer	Sheet 5 of 16

FPGA with 8K LUTs

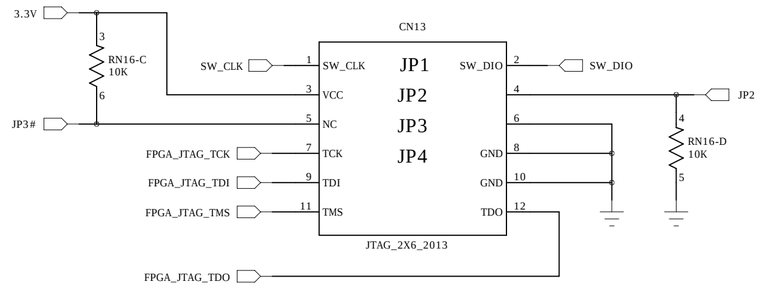


Technologic Systems	Date June 13, 2015	
Title: TS-7250_V2 FPGA		
Rev: B	Designer	Sheet 6 of 16

FPGA Caps



JTAG Header



Jumpers:

JP1 = User

JP2 = Console --> DB9

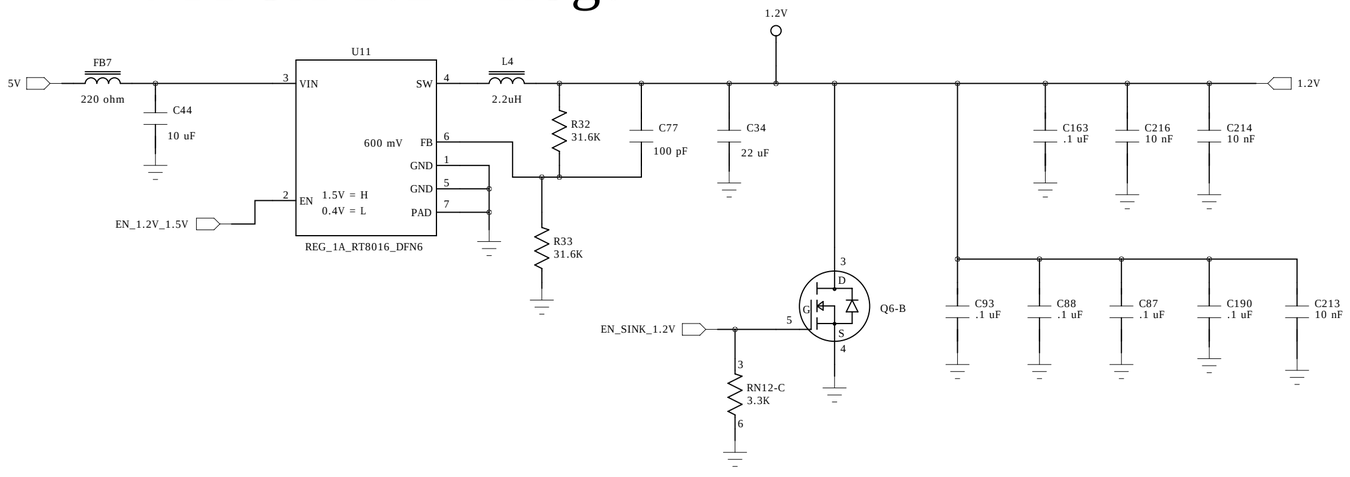
JP3 = SD Boot

JP4 = User

If JP4 installed

CPU can not reload FPGA

#4 FPGA 1.2V Reg.



TS-7250

Jumpers:

JP1 = Boot Serial

JP2 = Console Enable

JP3 = Write Enable Flash

JP4 = Stop @ Redboot

JP5 = TS_Test

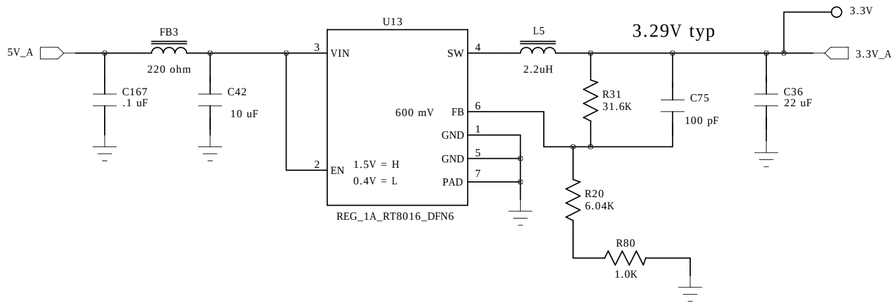
JP6 = Reserved

Technologic Systems	Date June 13, 2015	
Title: TS-7250_V2 FPGA PS, JTAG		
Rev: B	Designer	Sheet 7 of 16

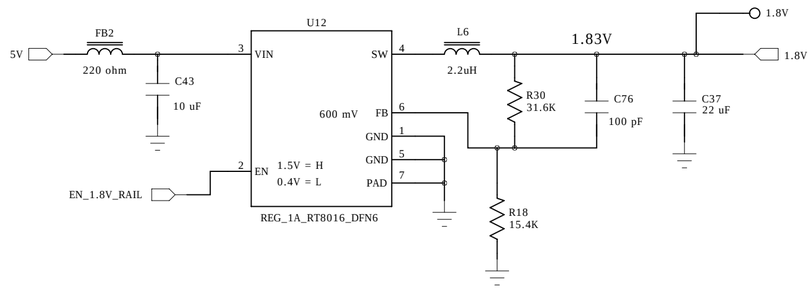
Power Supplies

#1 3.3V Power Supply

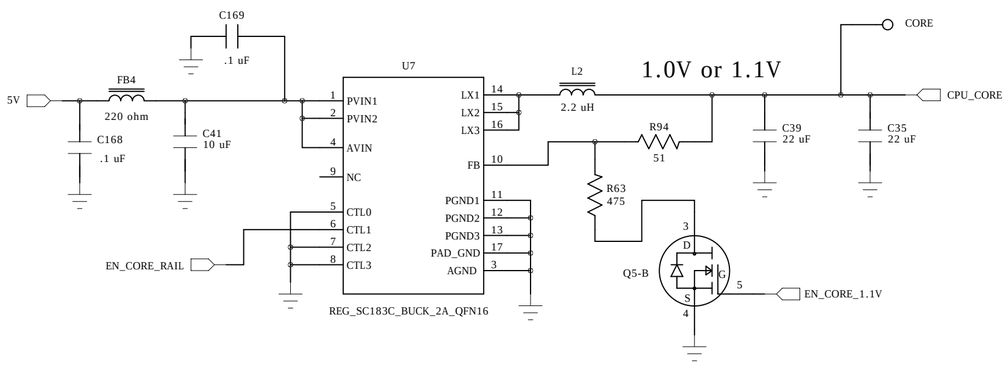
up to 1000 mA



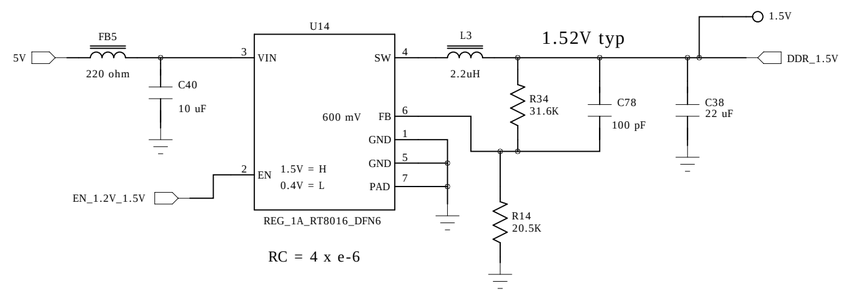
#2 1.8V Regulator



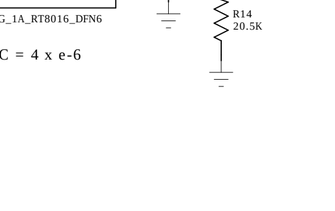
#3 CPU Core Supply



#4 DDR3 1.5V Reg.

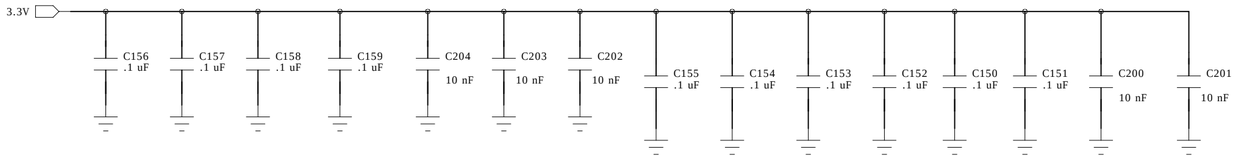


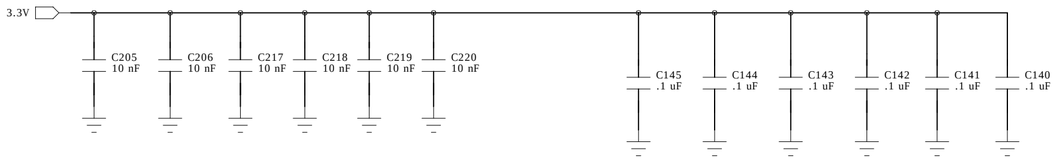
#5 CPU USB Power

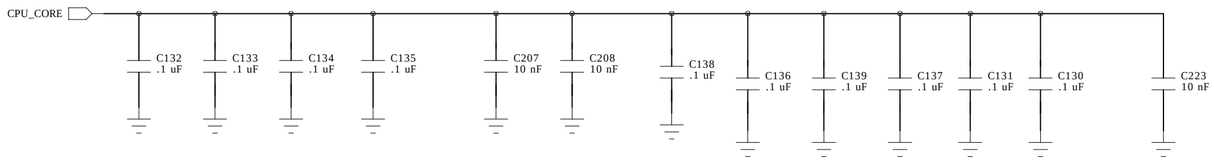


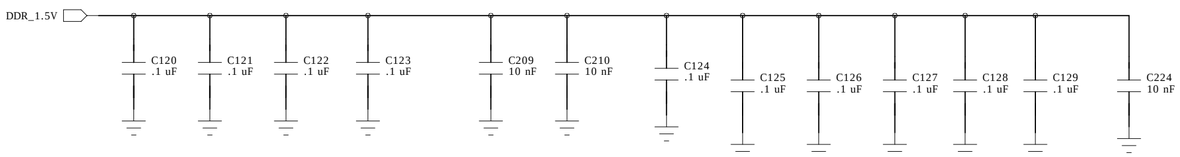
Technologic Systems	Date June 13, 2015	
Title: TS-7250_V2 Power Supplies		
Rev: B	Designer	Sheet 8 of 16

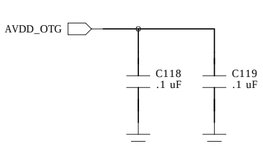
CPU Power



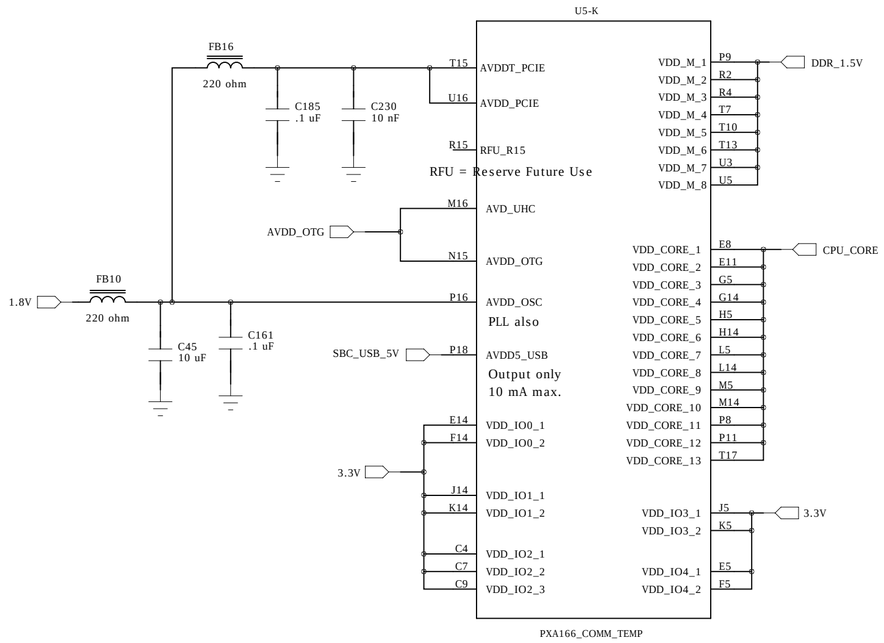






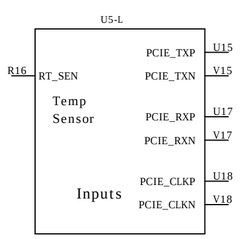


CPU

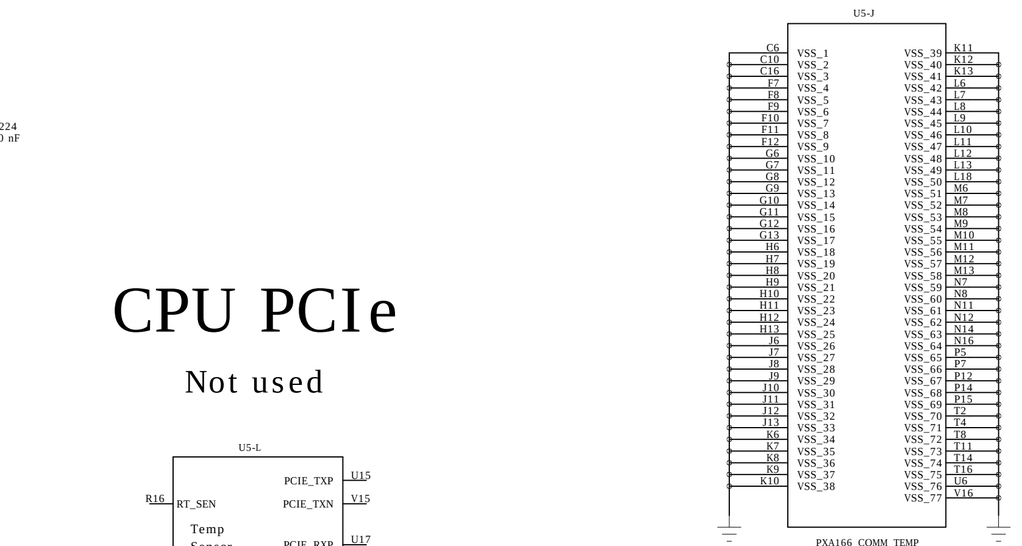


CPU PCIe

Not used



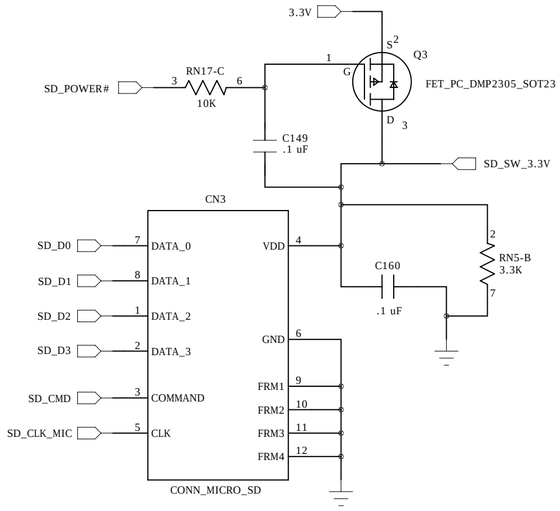
CPU



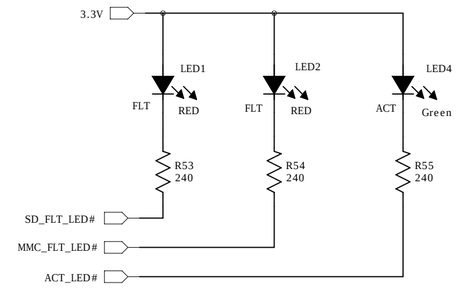
Technologic Systems	Date June 13, 2015	
Title: TS-7250_V2 CPU Power, Bypass caps		
Rev: B	Designer	Sheet 9 of 16

Flash Storage

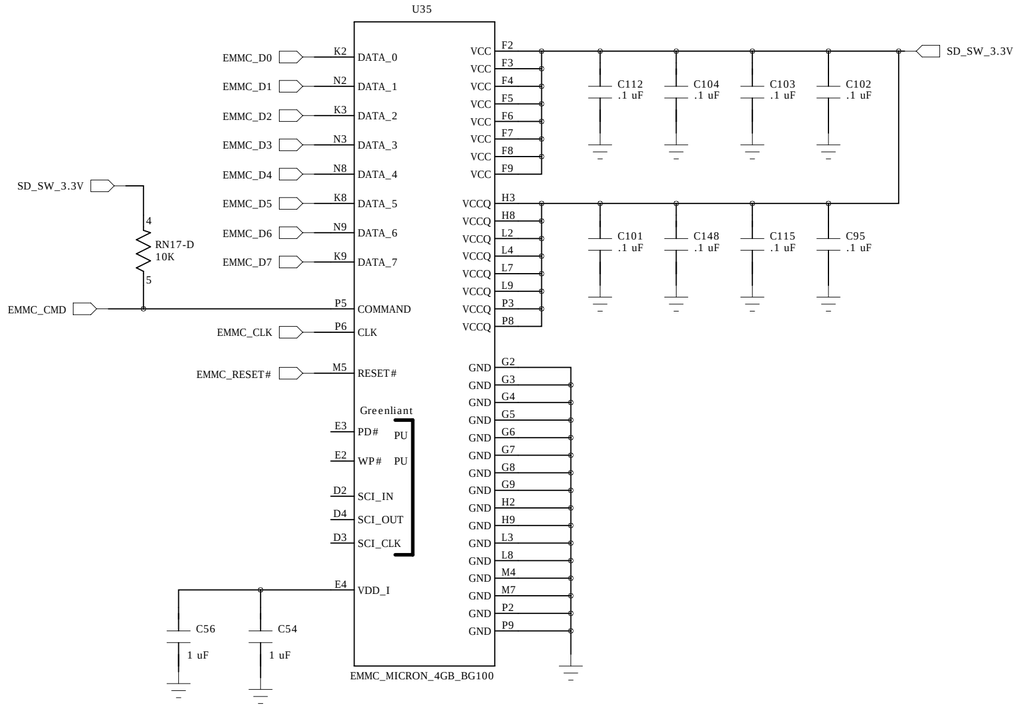
Micro SD Card Socket



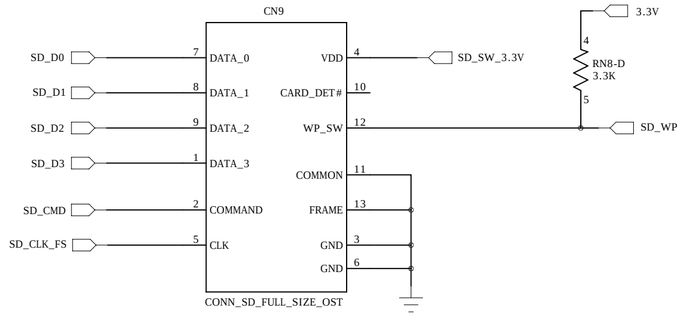
SD Card LEDs



eMMC 4GB

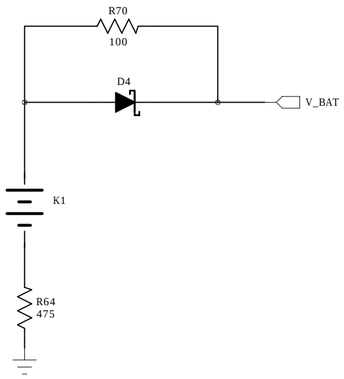


Full Size SD Socket

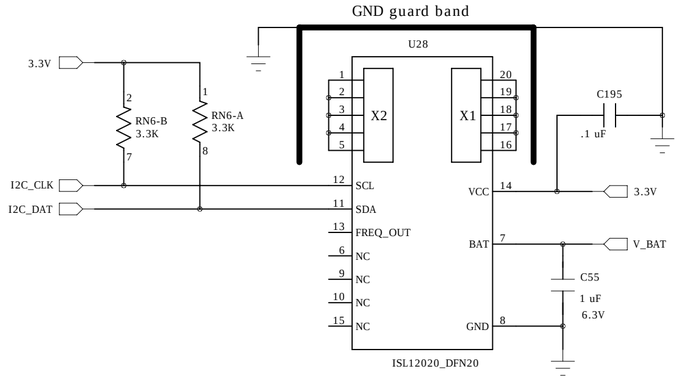


Technologic Systems		Date June 13, 2015
Title: TS-7250_V2 SD card, eMMC		
Rev: B	Designer	Sheet 10 of 16

RTC Battery

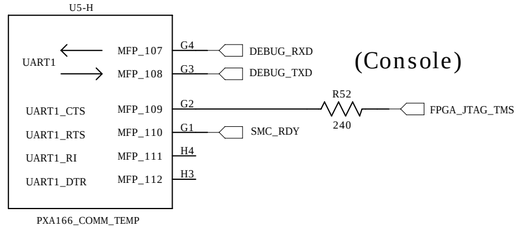


RTC and Temp. Sensor

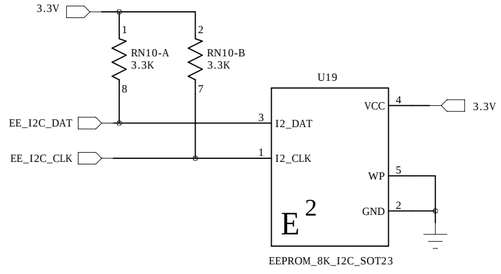


CPU

Debug UART



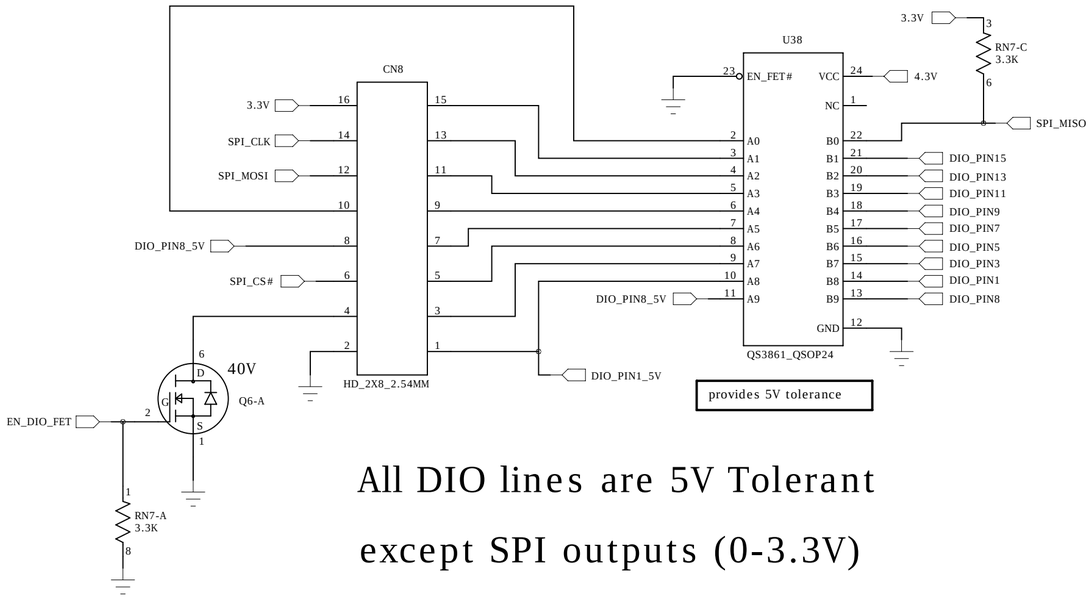
EEPROM 1 Kbyte



Technologic Systems		Date June 13, 2015
Title: TS-7250_V2 RTC, Battery, Boot Flag		
Rev: B	Designer	Sheet 11 of 16

DIO and LCD Headers

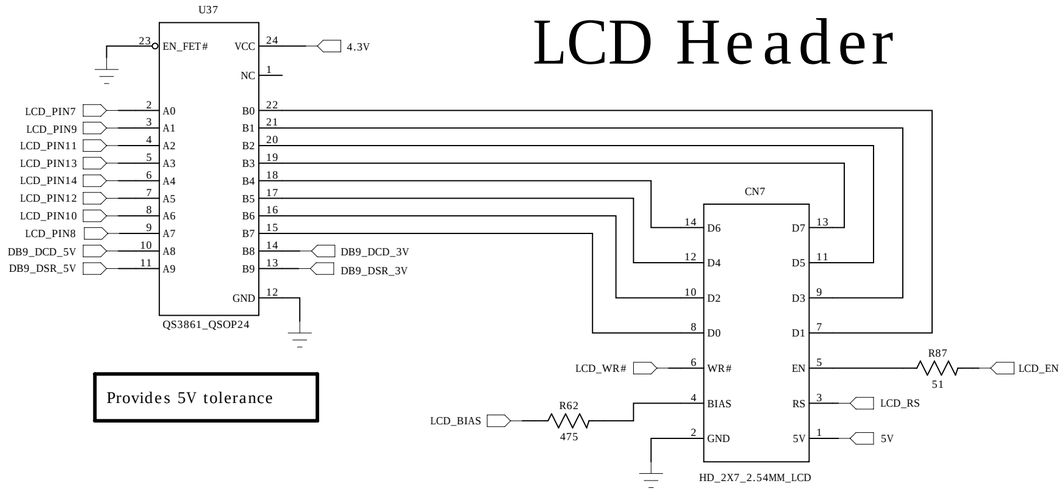
DIO Header



All DIO lines are 5V Tolerant

except SPI outputs (0-3.3V)

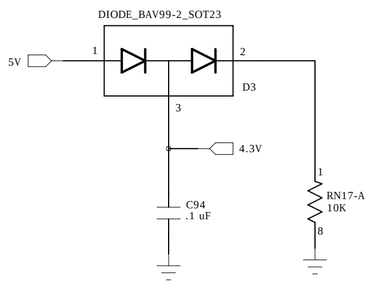
LCD Header



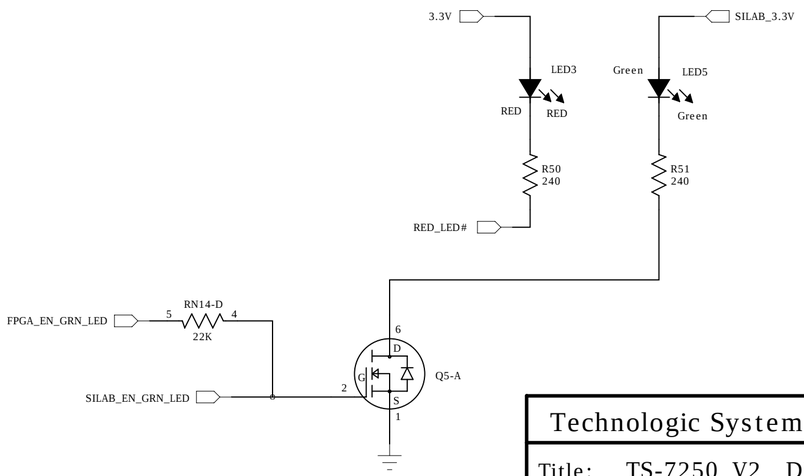
LCD Data lines are 5V tolerant

All LCD pins are bi-directional DIO

4.3V Supply



Red and Green LEDs

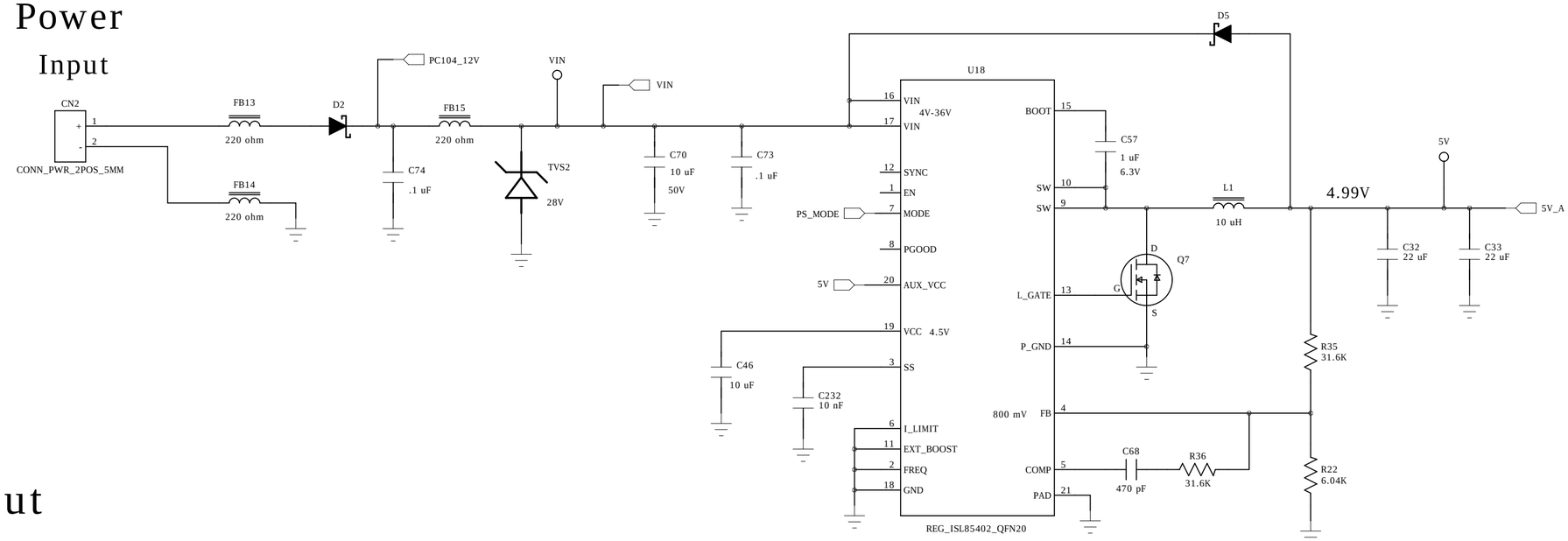


Technologic Systems		Date June 13, 2015
Title: TS-7250_V2 DIO and LCD Headers		
Rev: B	Designer	Sheet 12 of 16

5V Power Supply (2000 mA)

8V-28V

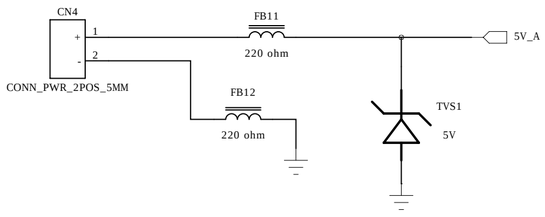
Power Input



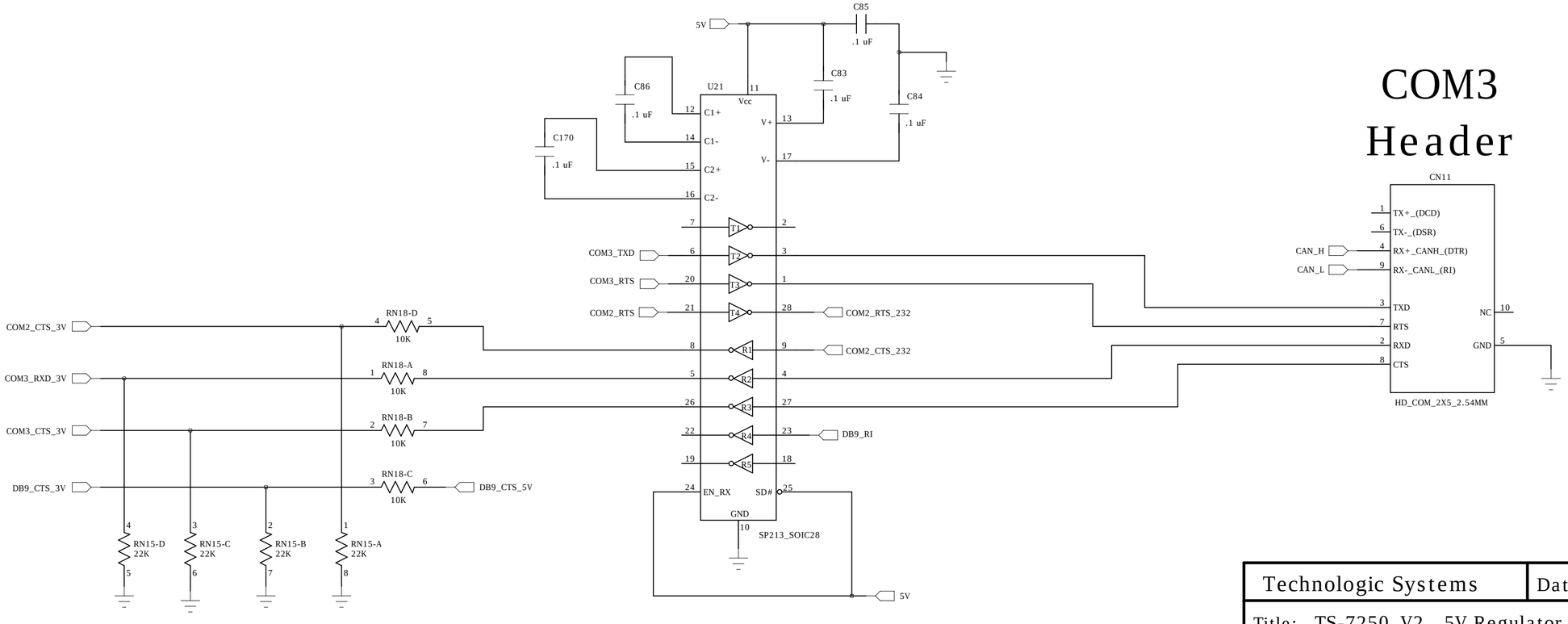
.063 hole

GND

5V Input



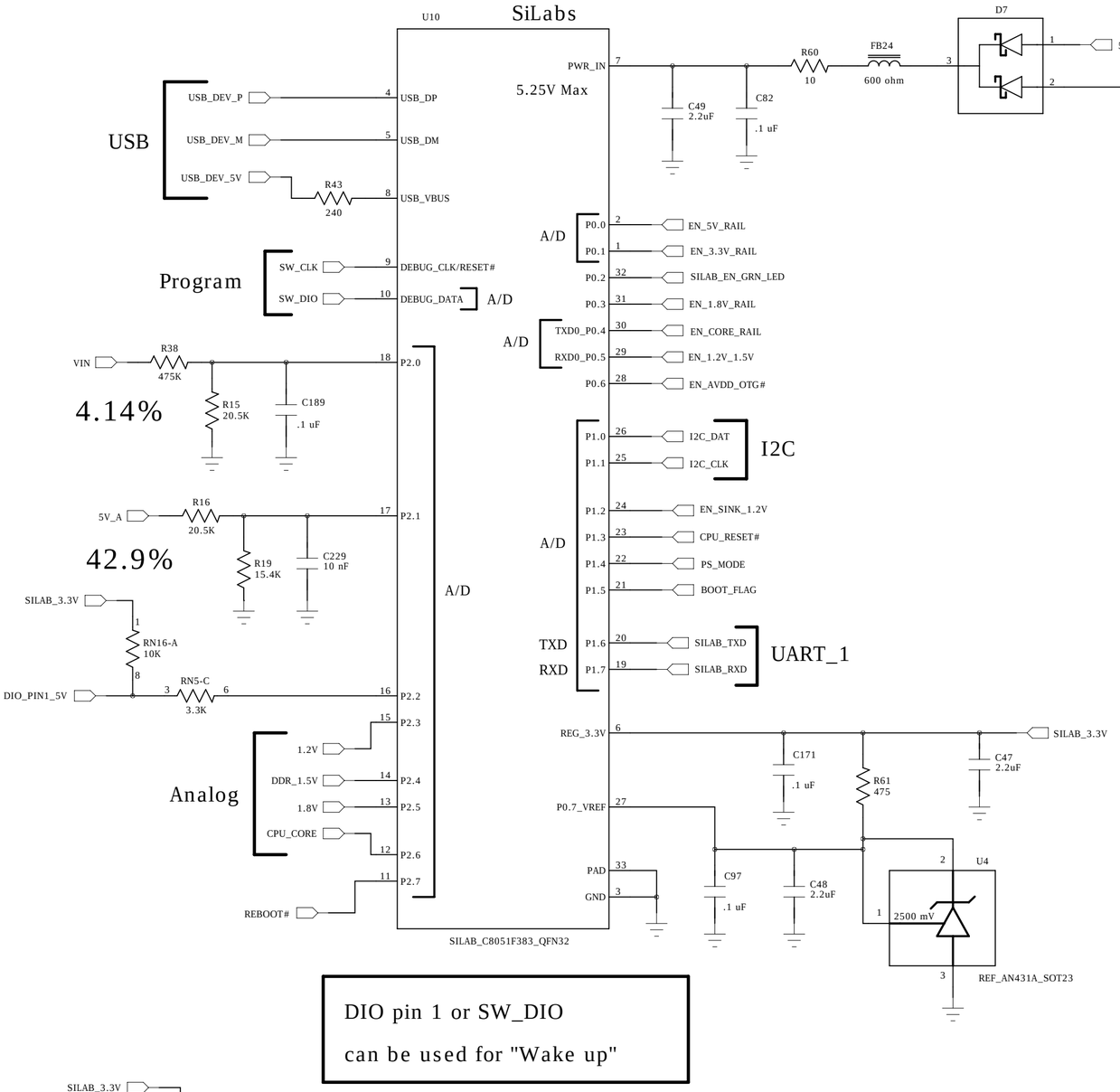
RS-232 Transceiver



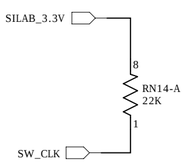
COM3 Header

Technologic Systems		Date June 13, 2015
Title: TS-7250_V2 5V Regulator		
Rev: B	Designer	Sheet 13 of 16

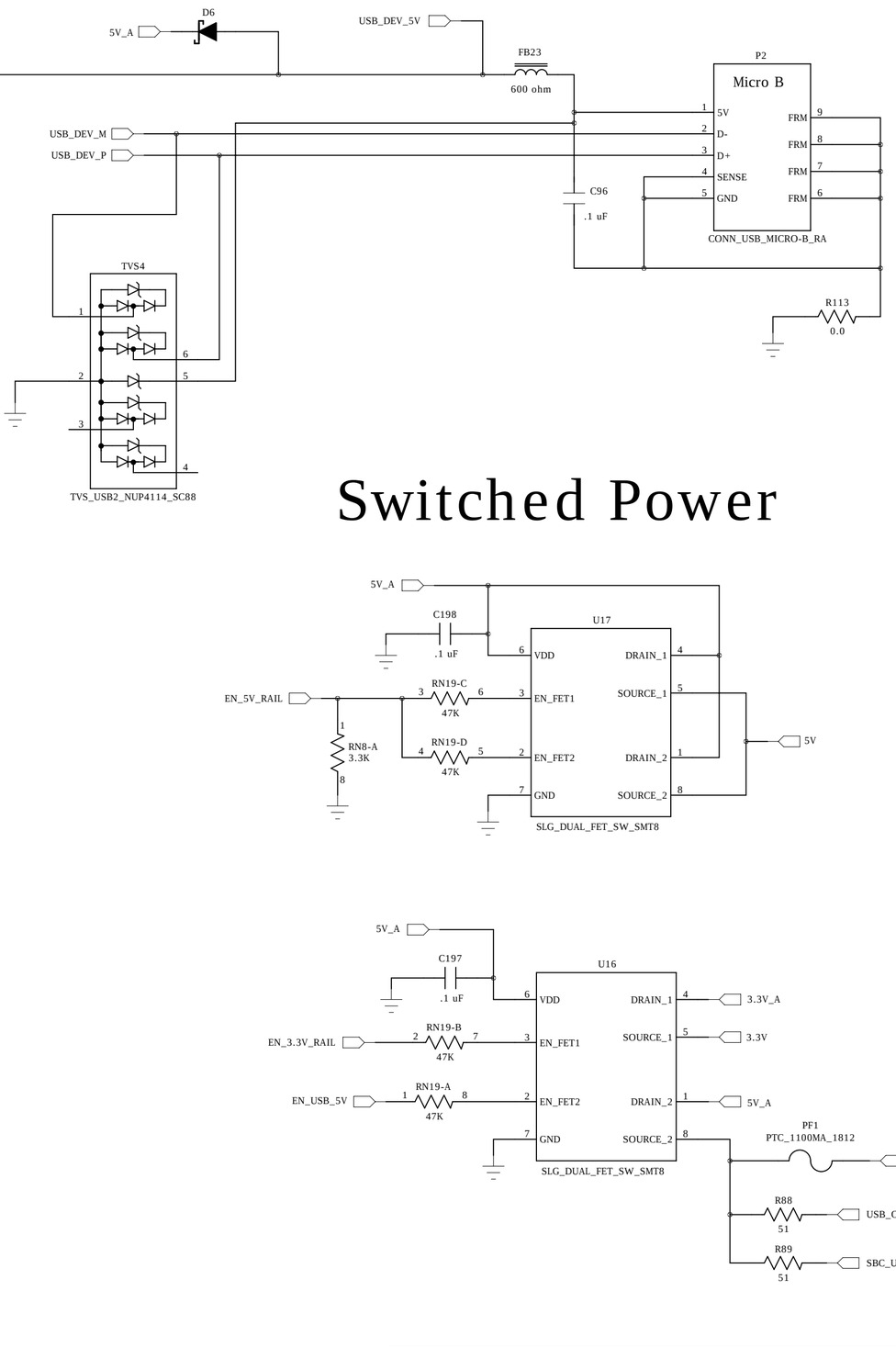
USB Device Port and SiLab uC



DIO pin 1 or SW_DIO
can be used for "Wake up"



USB Device Port



Switched Power

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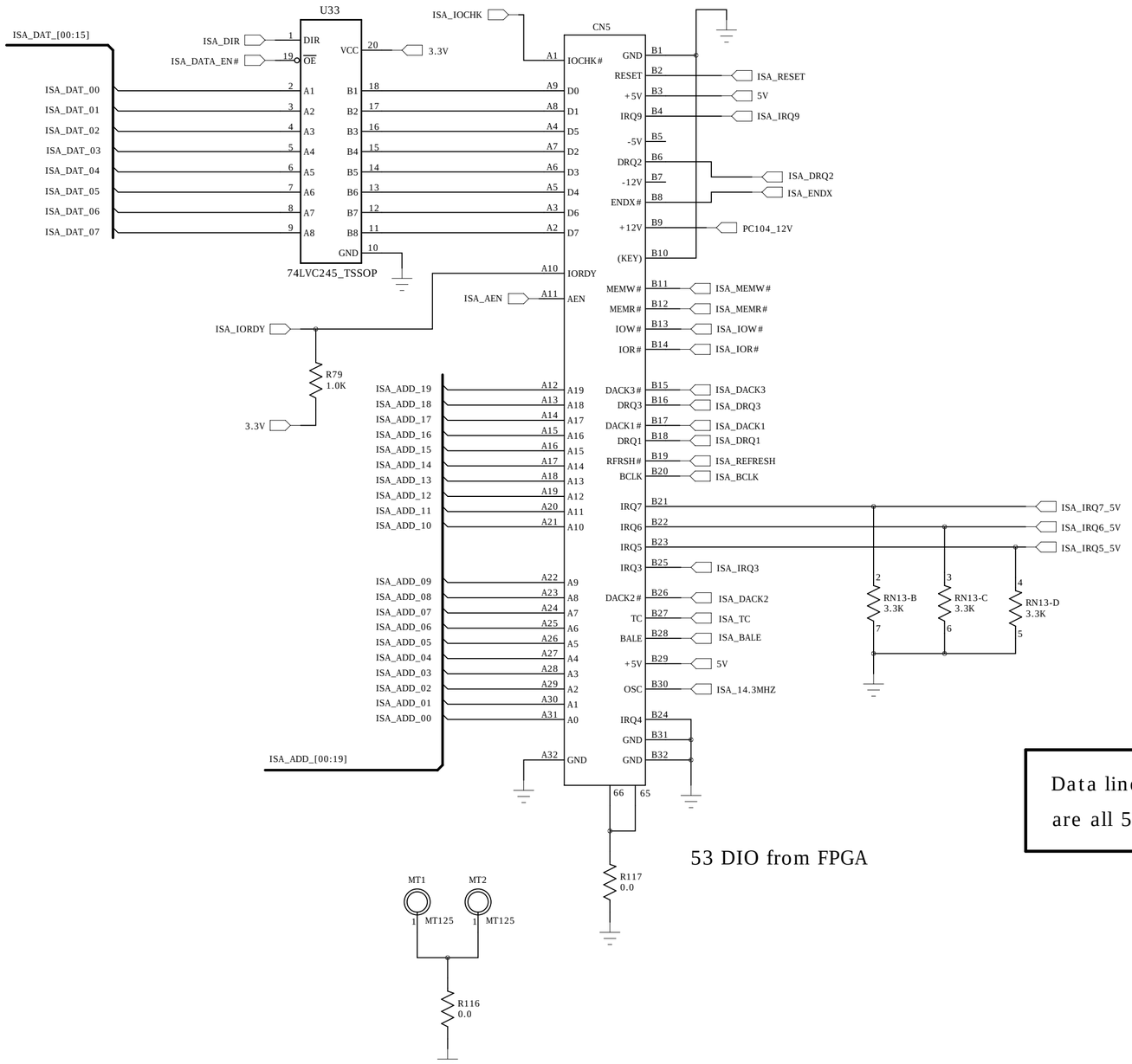
PC/104 Bus

CN5 has data pins wrong
Problem fixed in FPGA
Means data names wrong

PC/104

64-pin Connector

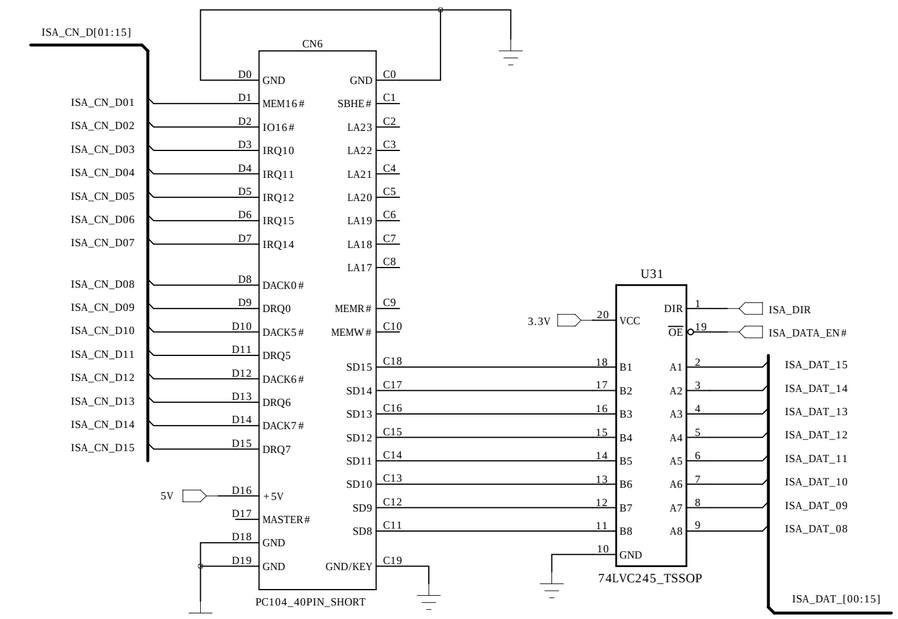


53 DIO from FPGA

Data lines and IRQ5-7
are all 5V tolerant

PC/104

40-pin Connector



23 DIO from FPGA

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0 to +30V Input range

or

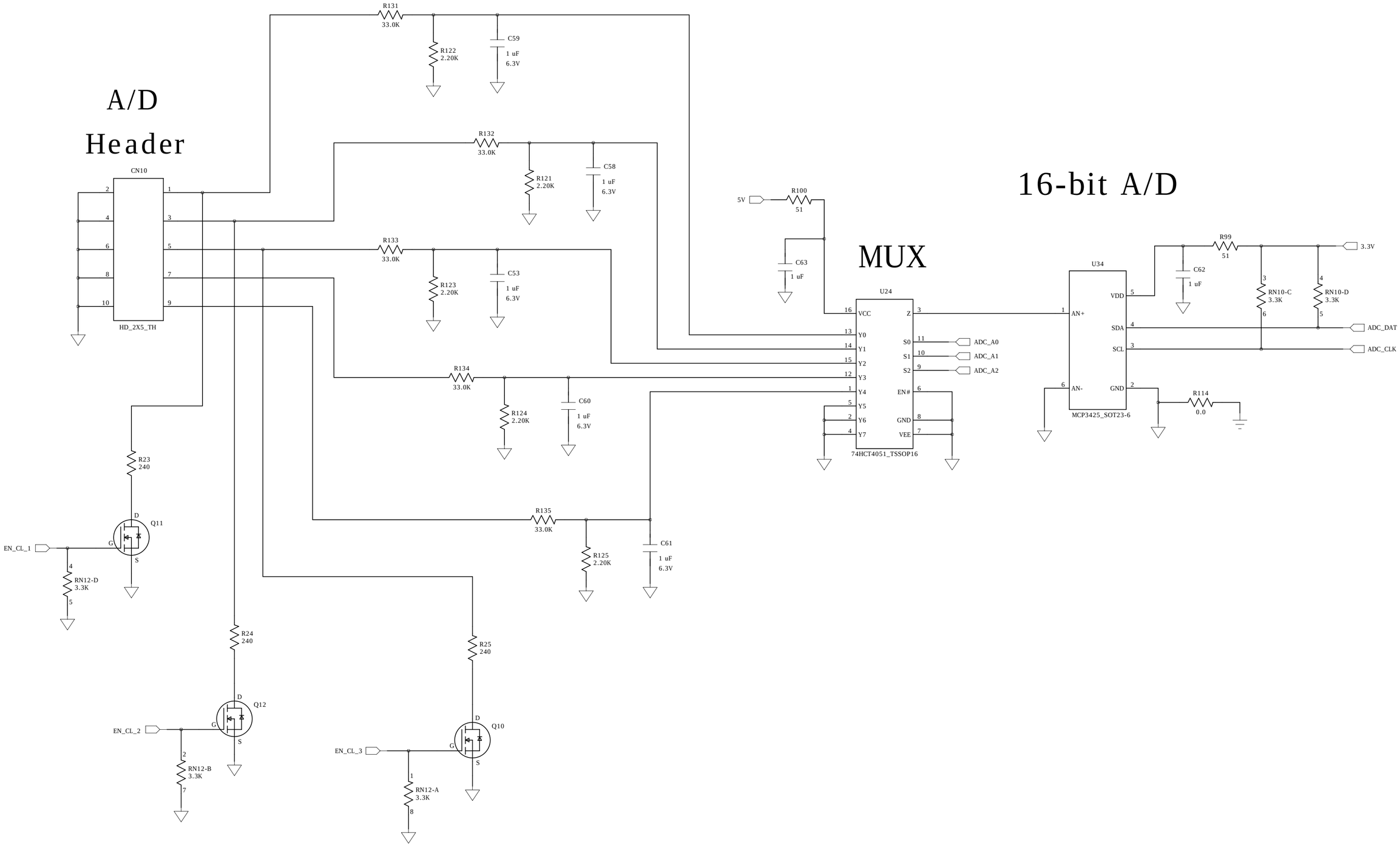
4-20 mA (3 channels)

Analog Inputs

A/D Header

MUX

16-bit A/D



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