**Rev.A Notes:**
- D6 and TVS6 not pop?
- R113 pop? (PS_MODE)
- R78 not pop for PXA166
- FB16 and FB17 not pop
- No stencil change!!

**Changes from Rev.P2**
- Change FB22 to 0 ohm (R69)
- Added PD on EN_SINK_1.2V
- U13 EN pin connected to 5V
- Model = TS-7250-V2 Rev.A

**Board ID**

<table>
<thead>
<tr>
<th>Model</th>
<th>MFP_26</th>
<th>MFP_30</th>
<th>MFP_33</th>
</tr>
</thead>
<tbody>
<tr>
<td>TS-7250_V2</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>TS-7800_V2</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>TS-xxxx</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Requires MFP to be Inputs

**USB Ports**

- **PXA166** 800 MHz - PXA168 1066 MHz

**I2S**

- R78 installed when PXA168 is used

**Control**

**Camera**

**SMC Bus**

**LCD**

**Display**

**U2** = PXA166 Commercial Temp

or = PXA168 Industrial Temp

**Title**: TS-7250_V2 Marvell PXA166 or PXA168

**Rev**: A

**Designer**: Sheet 1 of 16

**Date**: Nov. 19, 2013
Off-Board Connectors

Dual Host USB Ports

Primary MagJack

Second MagJack

Swapped TX and RX pairs
10/100 Ethernet 4-Port Switch

Defaults to MII PHY mode with 3.3V Levels

Auto MDIX is supported
Polarity Correction also supported

Ports 1-4 are MII PHY mode with 3.3V levels

Power up with no config
Pull-downs default P6 to port disabled mode

All Port 6 pins have PU or PD bias

MII address A6 defaults to "1"

Pins 34 and 35 are NC if using external 1.2V and 1.8V power reg.
**FPGA Caps**

**JTAG Header**

**Jumpers:**
- JP1 = ??
- JP2 = SD Boot
- JP3 = Console --> DB9
- JP4 = User

If JP4 installed
CPU cannot reload FPGA

**# 4 FPGA 1.2V Reg.**

**TS-7250**

**Jumpers:**
- JP1 = Boot Serial
- JP2 = Console Enable
- JP3 = Wire Enable Flash
- JP4 = Stop @ Redboot
- JP5 = TS_Test
- JP6 = Reboot

Page 37 of Data Sheet (Hot Socketing)
FPGA Power Supplies can be sequenced in any order but must be monotonic.
All I/O lines are tri-stated during power cycling.
Title: TS-7250_V2 Power Supplies

Rev: A
Designer

Sheet 8 of 16

# 1 3.3V Power Supply  up to 1000 mA

# 2 1.8V Regulator

# 3 CPU Core Supply

# 4 DDR3 1.5V Reg.

# 5 CPU USB Power
CPU Power

TC-1

CPU

CPU

CPU PCIe

PXA168 PCIe rails must be connected to AN_1.8V

Not used

PCIe not supported on PXA166

CPU

Technologic Systems  Date Nov. 19, 2013
Title:  TS-7250_V2 CPU Power, Bypass caps
Rev: A  Designer  Sheet 9 of 16
RTC Battery

RTC and Temp. Sensor

CPU

Debug UART

EEPROM 1 Kbyte
DIO and LCD Headers

DIO Header

All DIO lines are 5V Tolerant except SPI outputs (0-3.3V)

LCD Header

LCD Data lines are 5V tolerant

Red and Green LEDs

4.3V Supply
5V Power Supply (2000 mA)

Power Input

8V-28V

Mode (pin 7) is 0.8V when open with 12V applied to VIN

RS-232 Transceiver

COM3 Header
USB Device Port and Cortex M0

Pins 2 and 3 must be high at Pwr up

DIO pin 1. SW_CLK or SW_DIO can be used for M0 "Wake up"

To test JP1, set SW_DIO low for 2 us read SW_CLK then tri-state SW_DIO

Covertx M0

USB Device Port

Power Sequencer

Wait until 5V_A rail > 4.2V for 80 ms, then start sequencing

Delay:
1 - Enable 5V Rail
5 ms
2 - Enable 3.3V Rail
5 ms
3 - Enable 1.8V Rail
5 ms
4 - Enable Core Rail
5 ms
5 - Enable 1.2V and 1.5V
5 ms
6 - Enable AVDD_OTG Rail
80 ms
7 - Deassert CPU_RESET#

EN_SINK_1.2V is always complement of EN_1.2V_1.5V

If 5V_A < 4.0V, Deassert all Enables

Rise time of both outputs measured at ~1V/us
PC/104 Bus

PC/104
64-pin Connector

PC/104
40-pin Connector

Data lines and IRQ5-7 are all 5V tolerant
0 to +30V Input range
or
4-20 mA (3 channels)