1.2V Regulator

- Measured 57 mA/thm
- 1 ohm resistor, with FPGA 2K Look-up Table meaning
- 730 µs time constant

1.8V Switching Regulator

- 1.5 MHz freq, 50 mA quiescent
- 800mV Vout (1+ Drop/PD) > 90% off at 100-400 mA load
- 1000 mA max load

Technologic Systems

- Title: TS-7350 Power Supplies, Ethernet
- Date: March 15, 2008
- Rev: Designer RLM
- Sheet 3 of 7
RS-232 Transceiver

COM1 DB9M

JTAG 16-pin Header

RS-485 Drivers

DIO Header

24-pin Header

24 + 16 = 40-pin Header

- 4 ADC
- Latch
- GND
- 6 Latched Outputs (OUT0-OUT5)
- 7 Buffered Inputs (IN0-IN6)
- 1 SPI, 16-bit

UART0 and UART1 are in the EPM302 CPU chip
UART2 thru UART9 are X-UARTs in the FPGA
UART0 drives TTL levels to the JTAG header (TxD and RxD only)
UART1 drives COM1 TxD and RxD (RTS, CTS, DTR, DCD are from FPGA)
UART2 drives COM2 (TxD and RxD only)
UART1 and UART4 drive RS-485 ports
UART5 and UART6 drive COM1 handshakes
UART7 and UART8 drive PC104 bus (TTL levels)
UART9 drives DIO header (TTL levels)

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Date: March 15, 2008

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Title: TS-7350 COM Ports DIO JTAG Headers
Warning:
All IRqs and data lines
D0-D7 are 5V tolerant
all other signals must
use 3.3V levels
IRQ3 must be 3.3V levels
33 lines directly into FPGA
plus 10 more (D0-D7 and IOB, IOW)
that can be used with no IRC option
plus 6 more from I/O (A14-A19)
Hysteretic Switching Power Supply

5V @ (2.5 Amps)

5-28V Power In

5V @ 220 ohm @100 MHz
50 milliohm DC

Mura t a GRM 31CR71H225K
2.2 uF @ 50V 10%

Vout = 1.24V * [(20K / Rbot) + 1]
7 uA shutdown 300 uA quiescent
35V max operating
Floating "Enable" = 0V

When Vin ≥ 4.9V
FET gate at 35 mV

2.2 uF @ 30V 10%
Metrix GRM1CR71H225K
0.10 @ 2K Reel Dip-chip

Floating knee at 28-32V
for 1 mA of current
14 Amps @ 42V

Technologic Systems

Title: TS-7350 5V Power Supply

Date: March 15, 2008

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