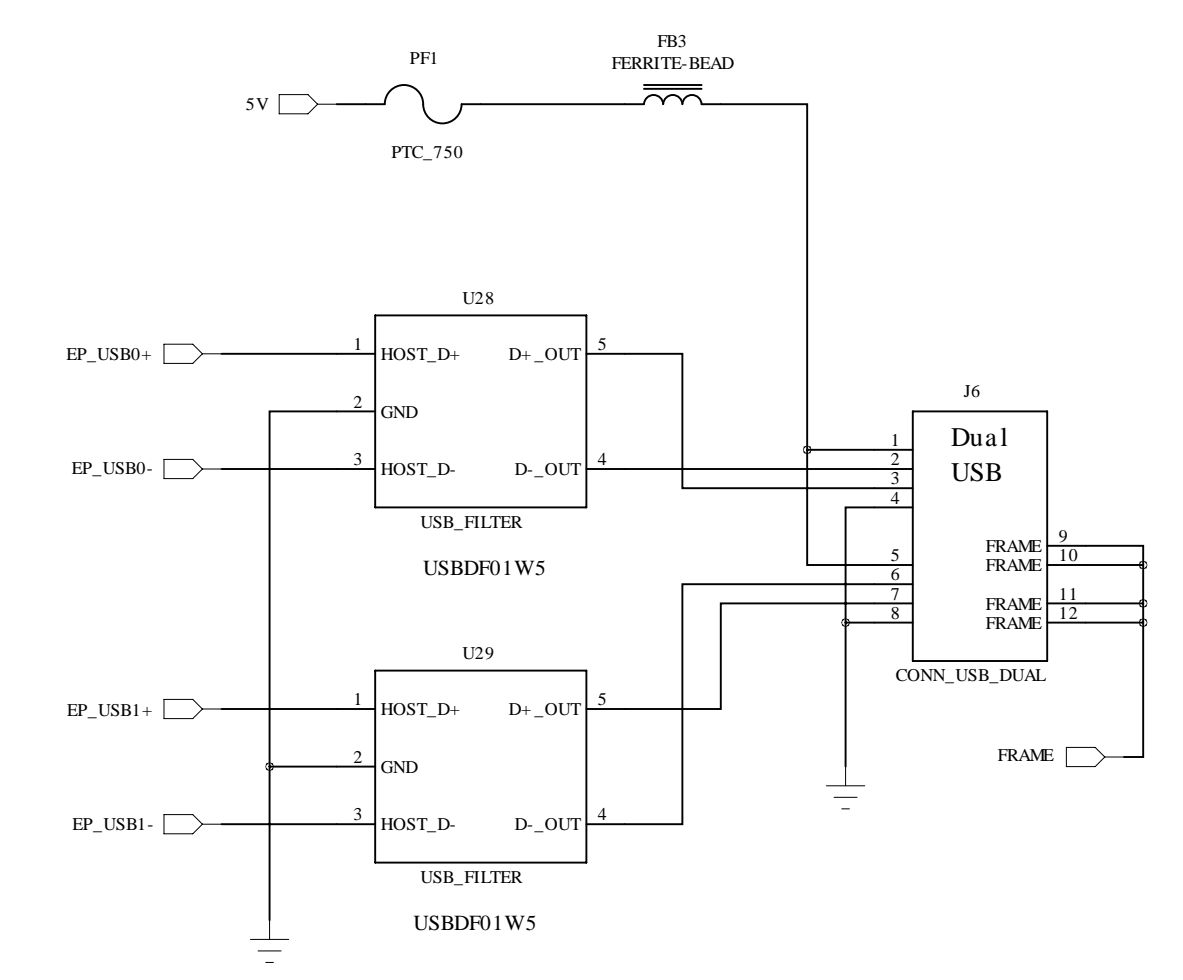


USB Ports

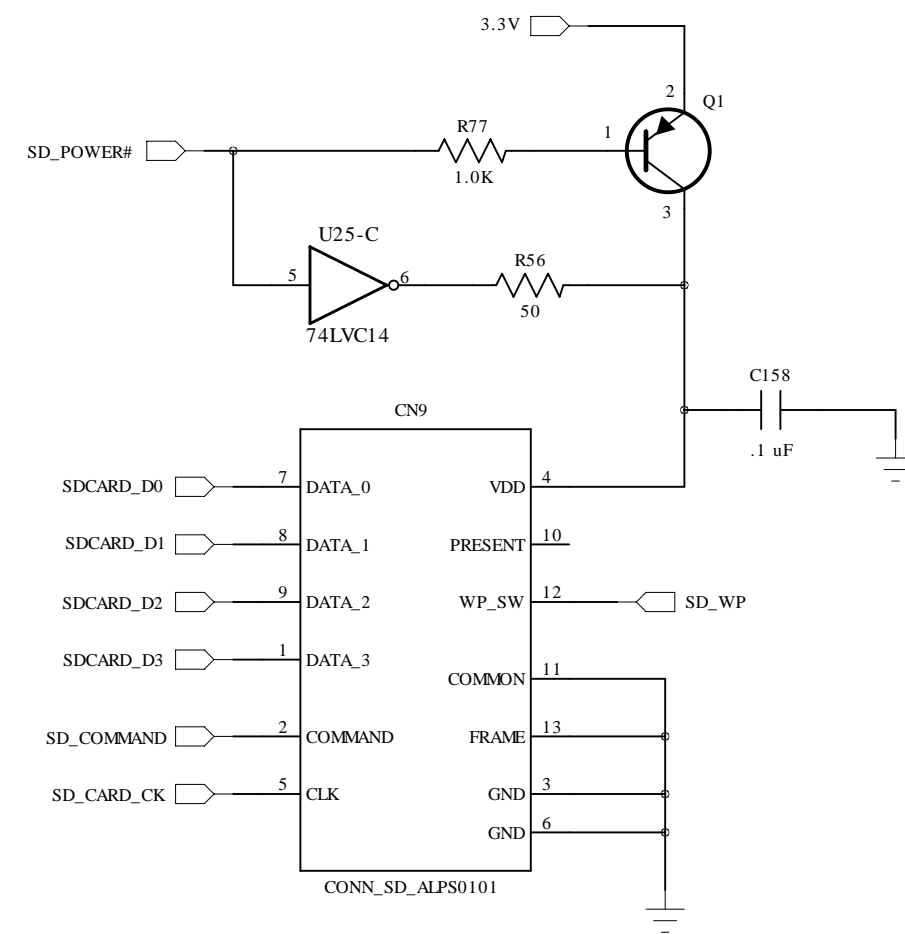


CS7# low = 16-bit Boot

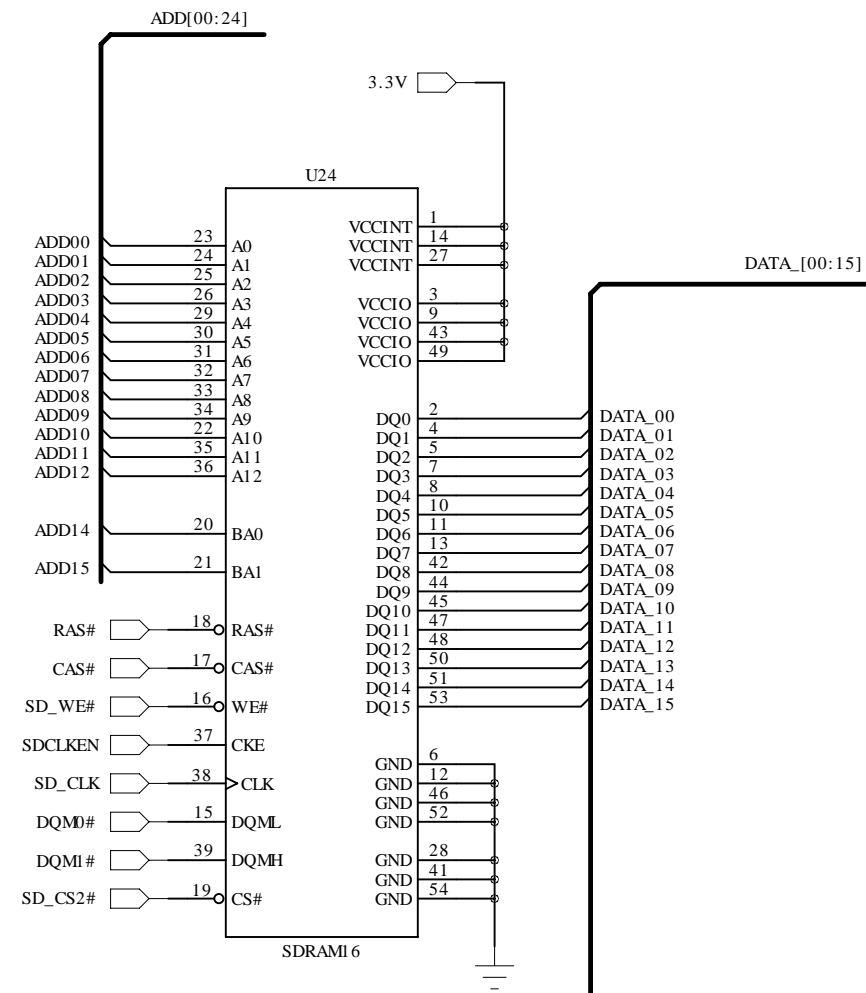
EE_CLK low @reset
= Boot External

Technologic Systems	Date	March 15, 2008
Title: TS-7350 EP9302 CPU, USB		
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		Sheet 1 of 7

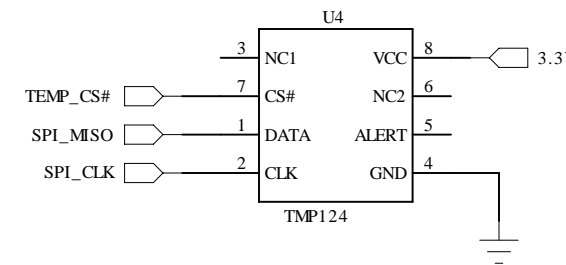
SD Card Socket



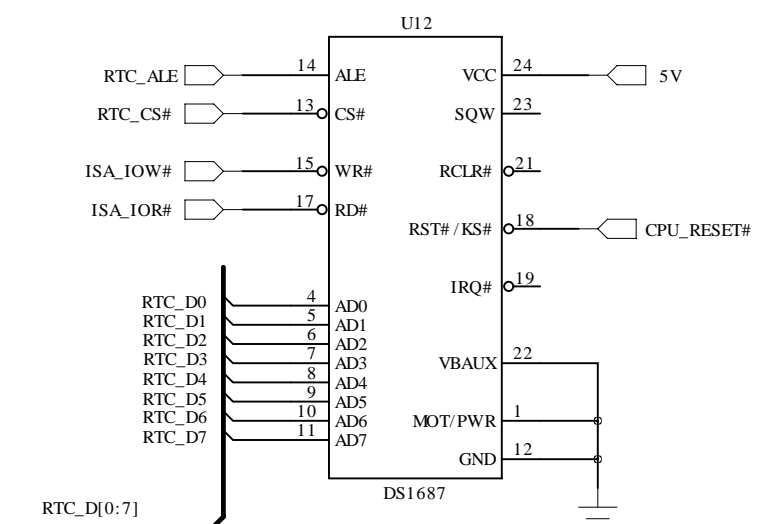
SDRAM



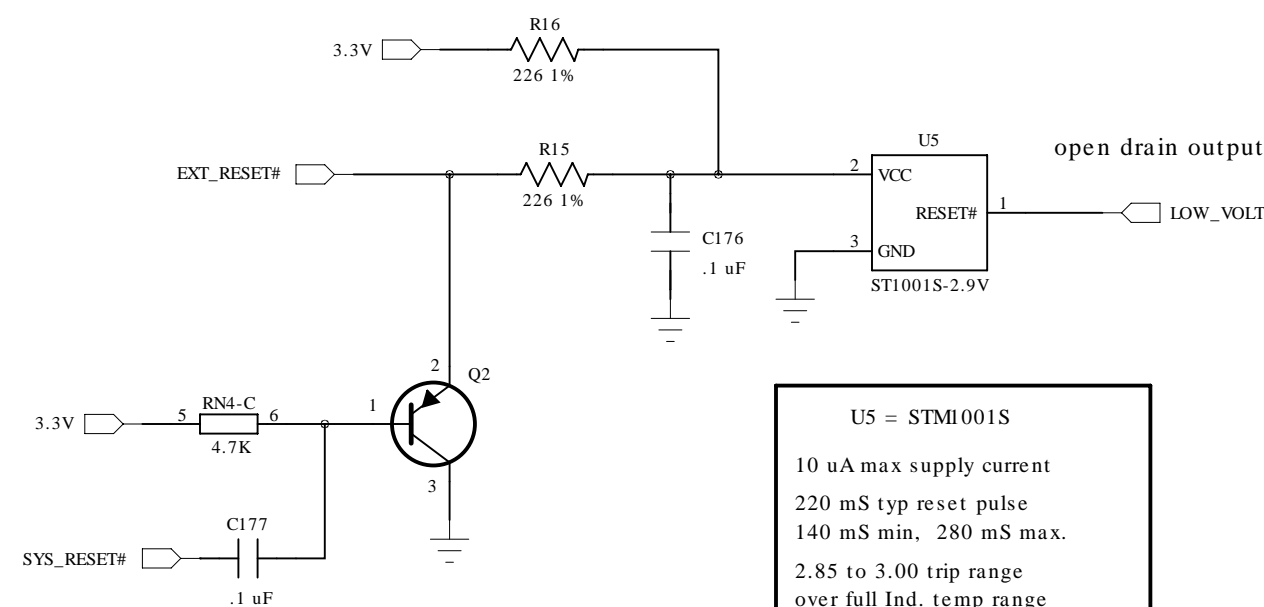
Temp Sensor



Battery-Backed Real Time Clock

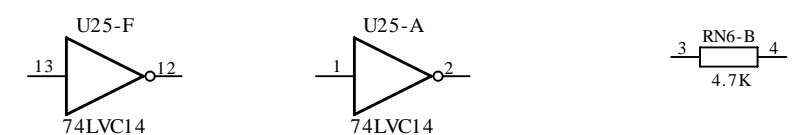
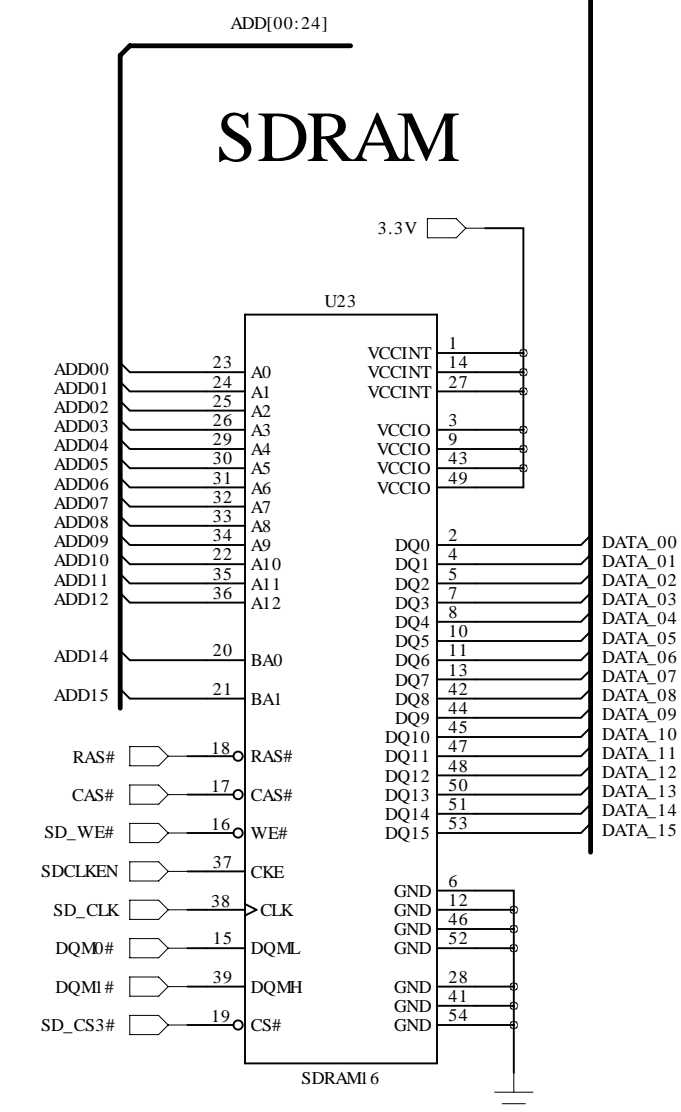


Power On Reset



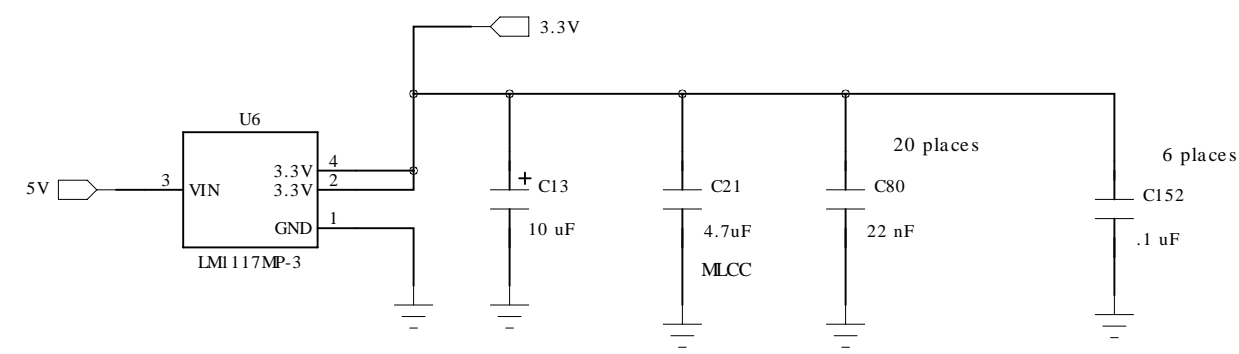
U5 = ST1001S
 10 uA max supply current
 220 mS typ reset pulse
 140 mS min, 280 mS max.
 2.85 to 3.00 trip range
 over full Ind. temp range
 guaranteed output low
 down to 1V Vcc
 but can only sink 1.2 mA

SDRAM

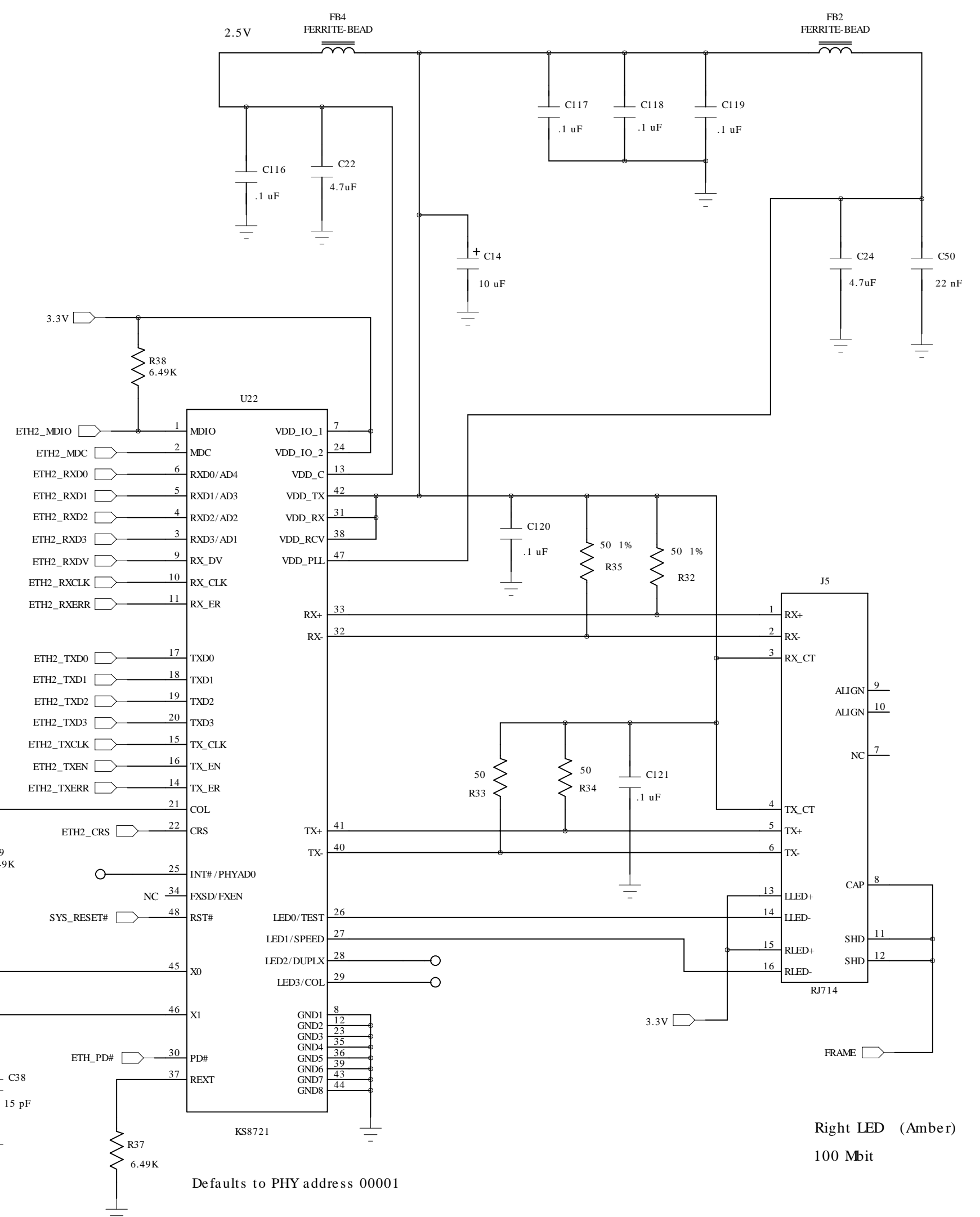


Technologic Systems	Date	March 15, 2008
Title:	TS-7350 SDRAM, Flash, RTC, POR	
Rev:	Designer	RLM
	Sheet	2 of 7

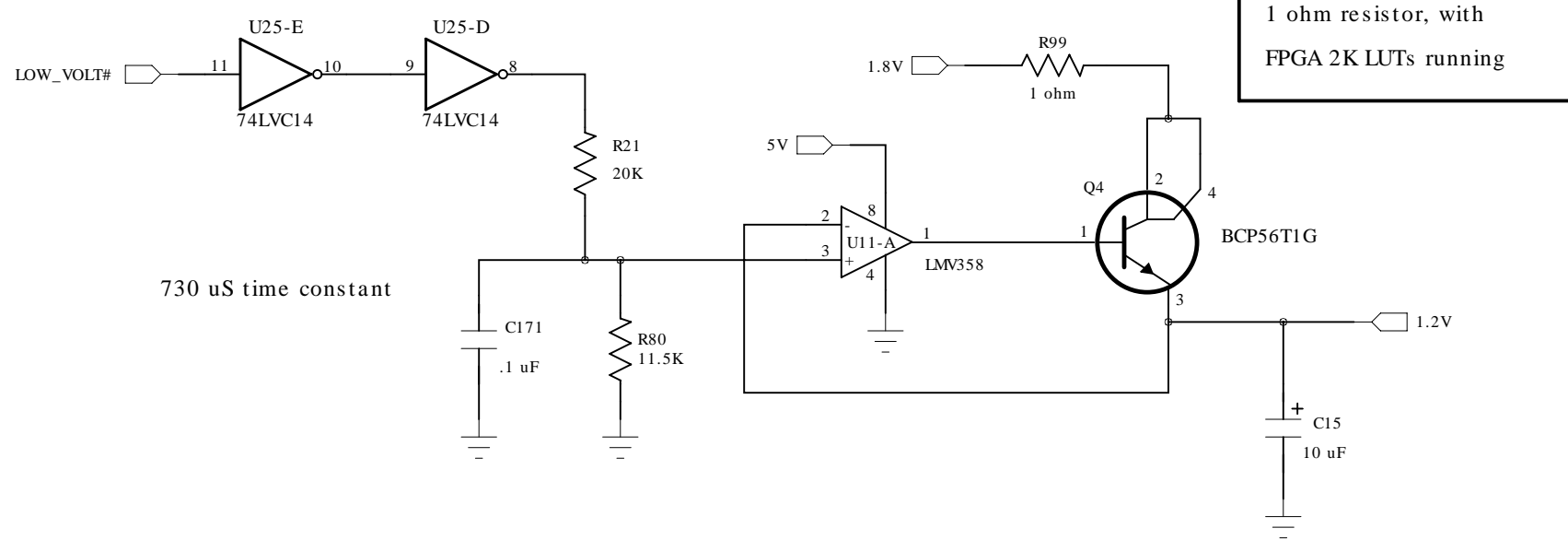
3.3V Regulator



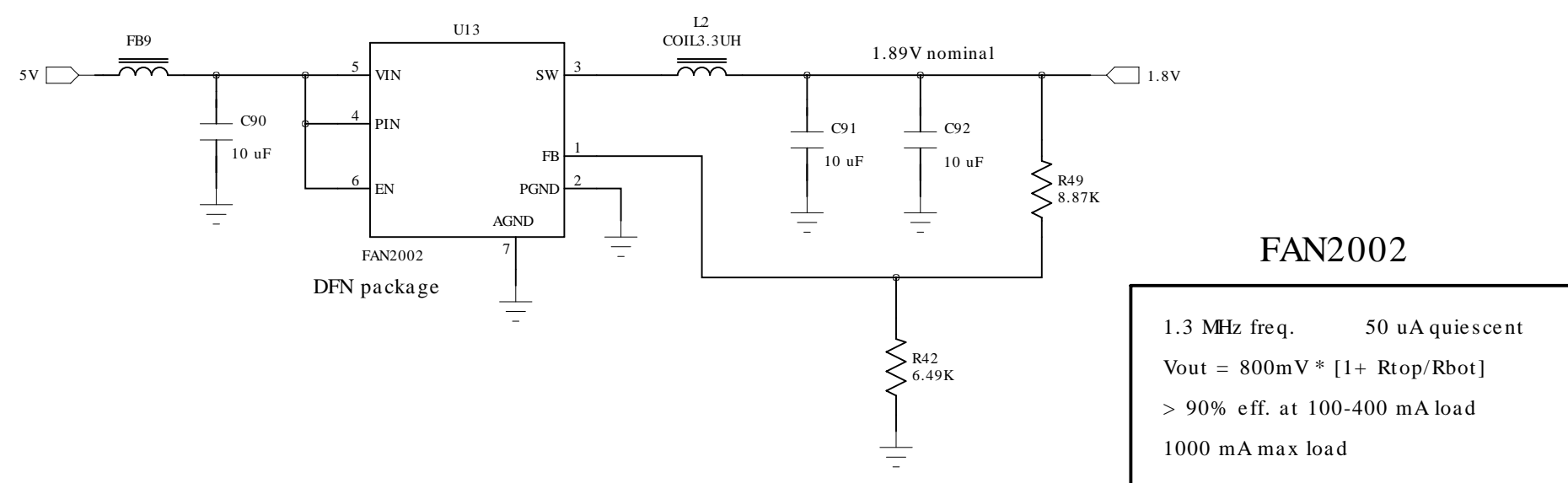
10/100 Ethernet



1.2V Regulator



1.8V Switching Regulator

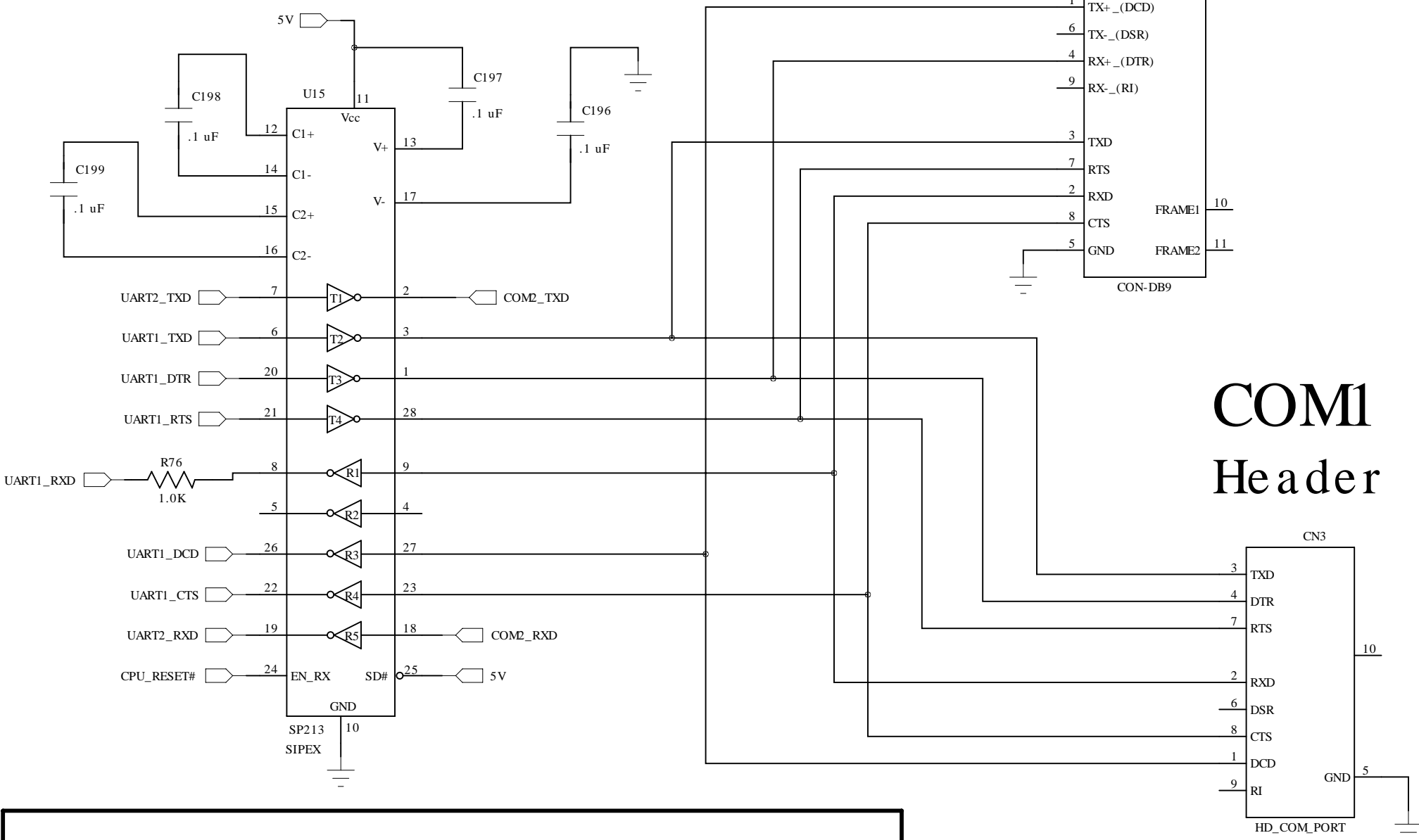


Right LED (Amber)
100 Mbit

Left LED (Green)
Link / Activity

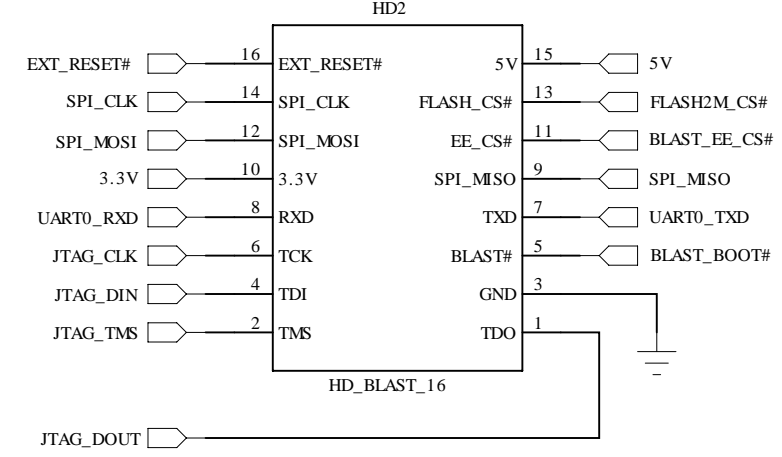
Technologic Systems		Date	March 15, 2008
Title: TS-7350 Power Supplies, Ethernet			
Rev:	Designer	RLM	Sheet 3 of 7

RS-232 Transceiver

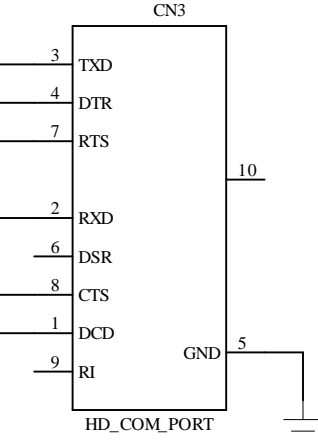


COM1 DB9M

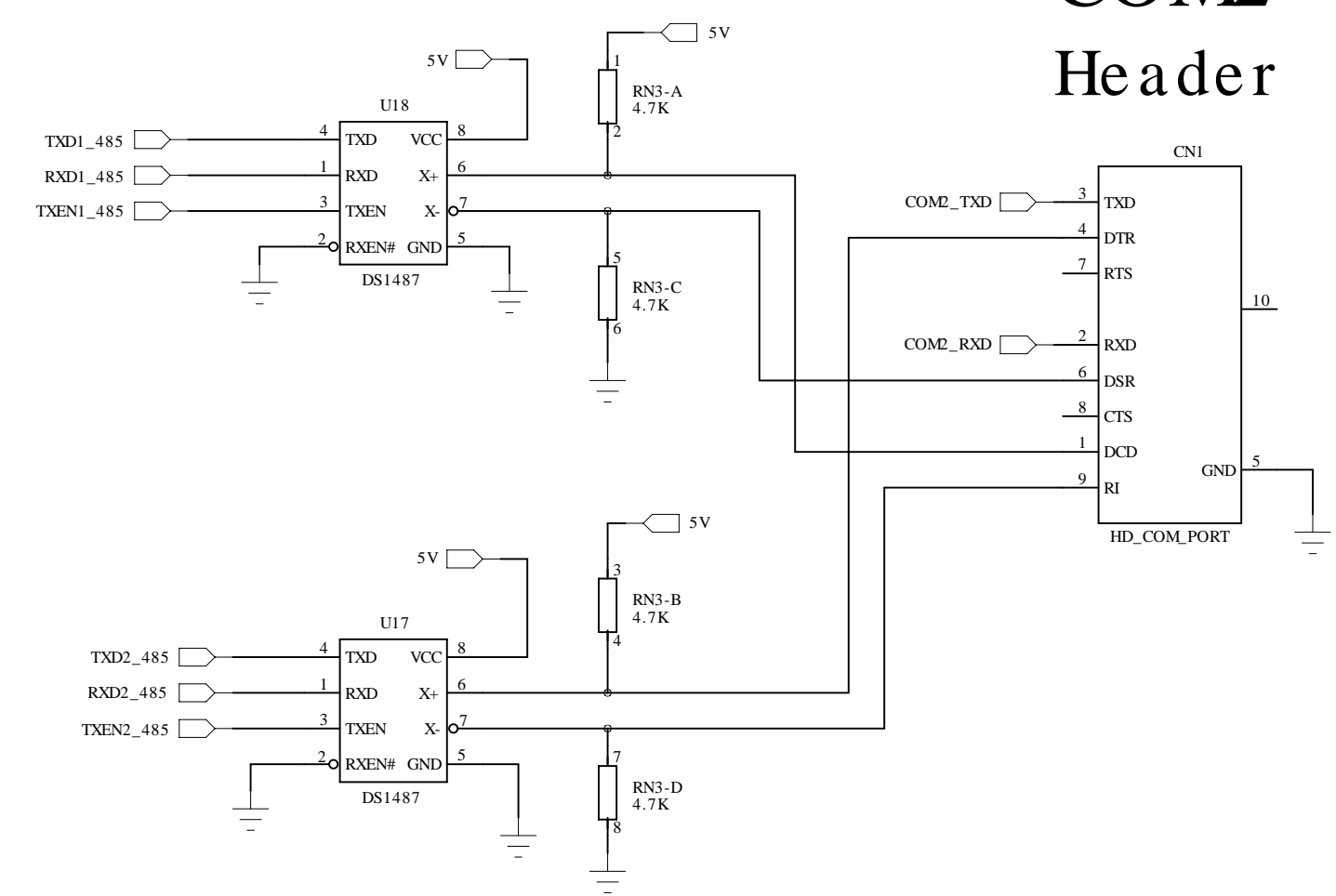
JTAG 16-pin Header



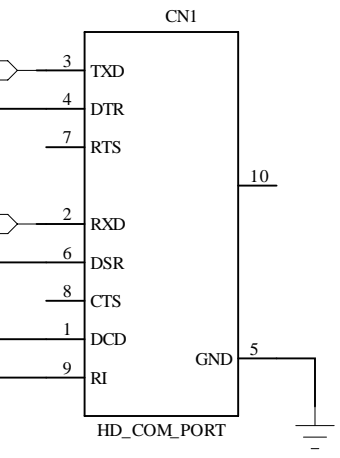
COM1 Header



RS-485 Drivers

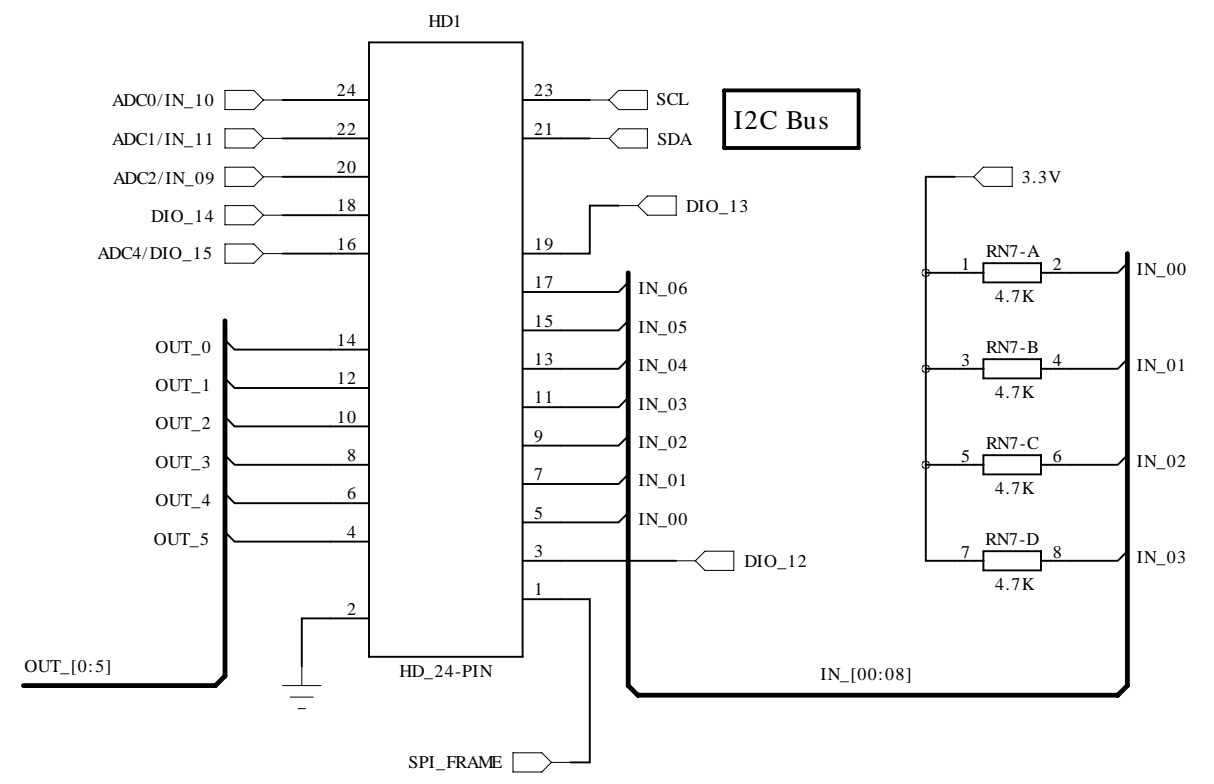


COM2 Header



UART0 and UART1 are in the EP9302 CPU chip
 UART2 thru UART9 are X-UARTs in the FPGA
 UART0 drives TTL levels to the JTAG header (TXD and RXD only)
 UART1 drives COM1 TXD and RXD (RTS, CTS, DTR, DCD are from FPGA)
 UART2 drives COM2 (TXD and RXD only)
 UART3 and UART4 drive RS-485 ports
 UART5 and UART6 drive COM1 handshakes
 UART7 and UART8 drive PC/104 bus (TTL levels)
 UART9 drives DIO header (TTL levels)

DIO Header



24-pin Header

24 + 16 = 40-pin Header

- 4 ADC
- ADC lines in parallel with IN_09, IN_10, IN11, DIO15
- 2 I2C
- 1 GND
- 6 Latched Outputs (OUT0-OUT5)
- 7 Buffered Inputs (IN0-IN6)
- 3 DIO_12, DIO_13, DIO_14
- 1 SPI_FRAME

Lattice XP2 FPGA

8 MB Video SDRAM

XP2-5 has:
 5K LUTs 2 PLLs
 9 blocks of 1Kx18 Block RAM
 12 18x18 Multipliers
 146 I/O with 208 pin package
 "instant ON" = about 1.5 mS
 input PLL clock = 10 MHz min

Make sure these signals are on CLK inputs:
 SDRAM_CLK
 FPGA_25MHz

PROGRAM#, DONE, and INIT# are dedicated configuration pins when CFG0 is low. When CFG0 is high they are "general purpose I/O"
 Page 4 of TN1141

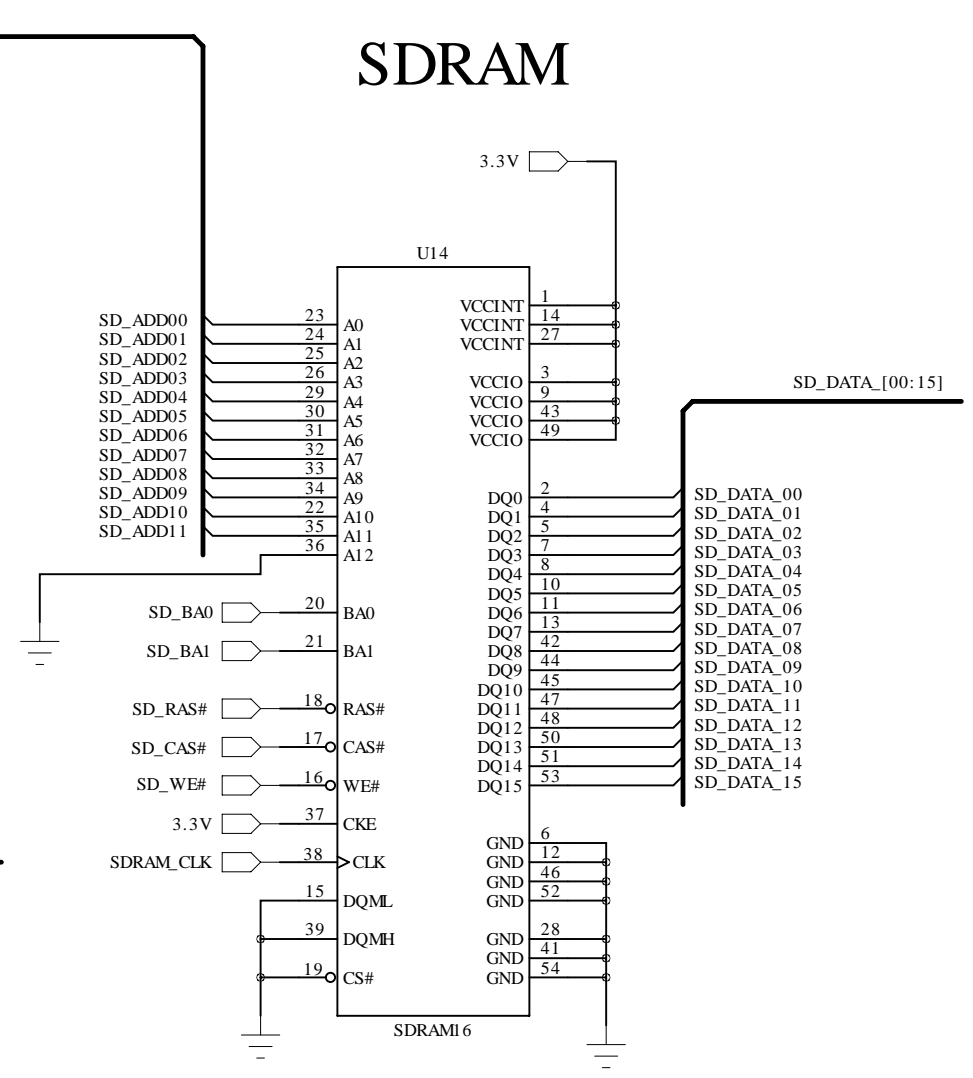
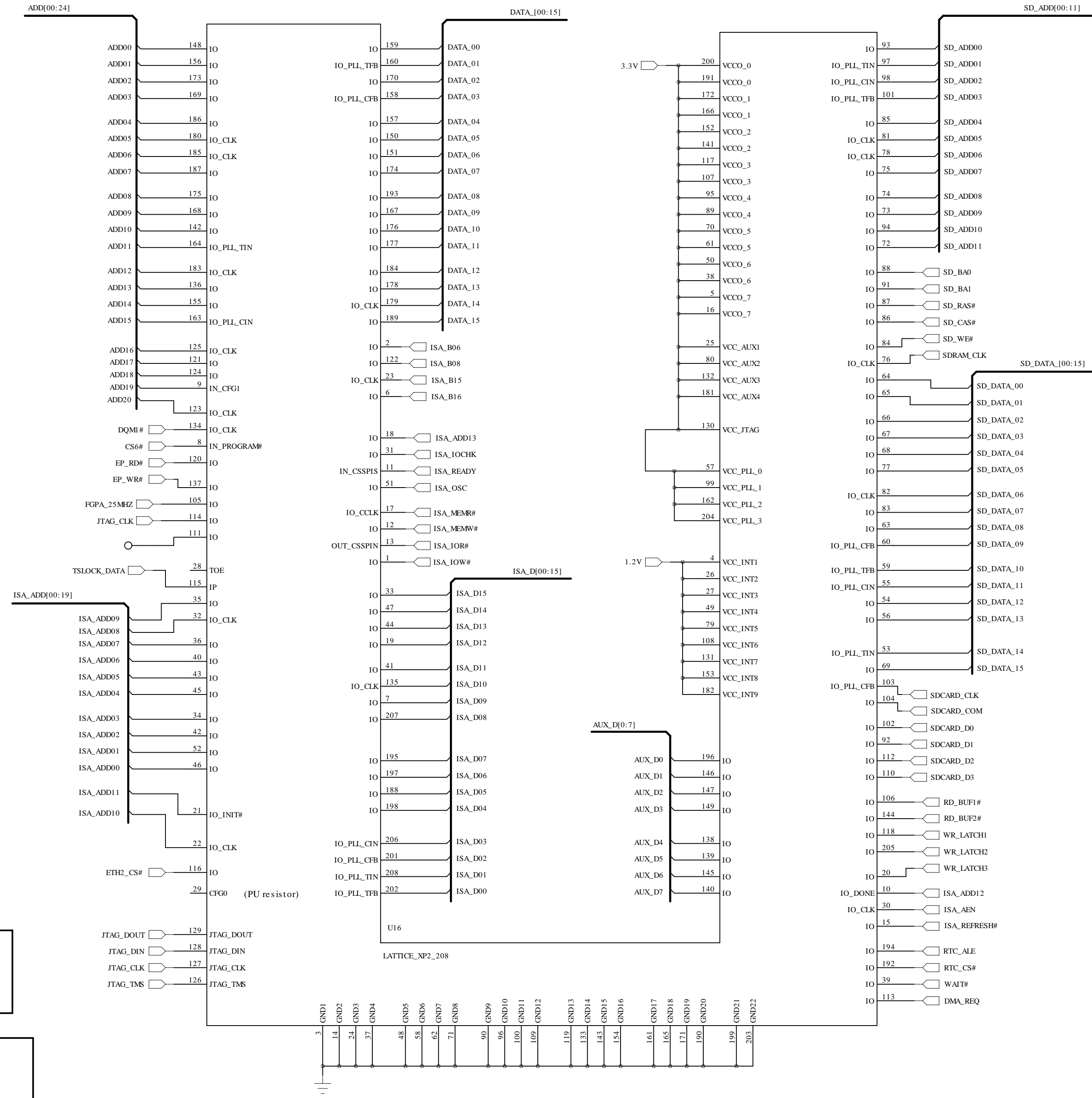
During JTAG Flash programming the PROGRAM# pin should be high else it can inhibit Flash --> SRAM
 DONE likewise must be high
 These do have weak PU resistors

When CFG0 = 1 then always uses SDM
 SDM = Self Download Mode
 SDM uses on-chip Flash --> SRAM
 CFG0 PU resistor uses VCC core (1.2V)

TAG Memory is 79 bytes of Flash (XP2-5)
 Always available thru JTAG port
 can not be Write or Read protected
 perfect for: MAC, birth date, Revision #
 TAG memory can be accessed from fabric

Set CONFIG_MODE to NONE
 This allows all pins to be used

Pull-up and pull-down resistors are 6 to 30K ohms



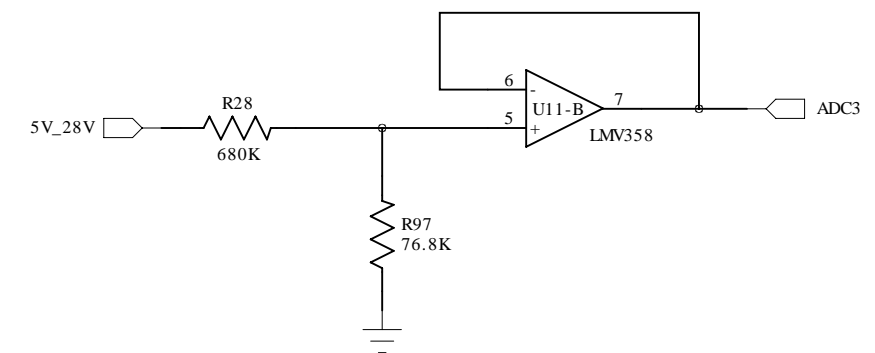
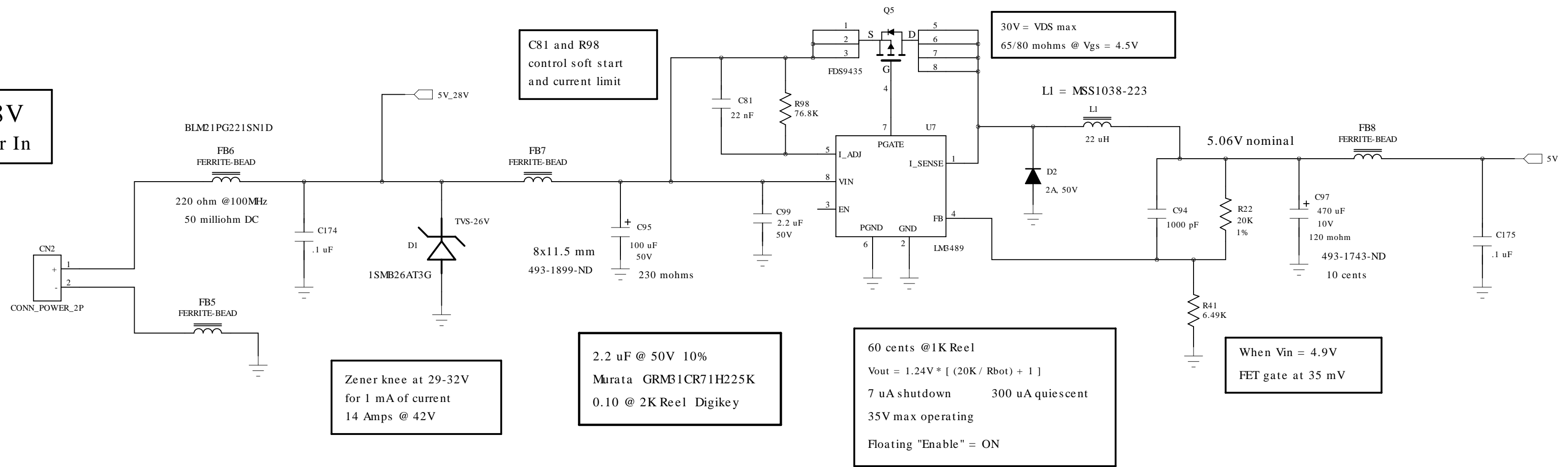
CPU_RESET is the same as PWR_RST# (as in TS-7xxx)
 In previous products, it was the OR of LOW_VOLT# and the WatchDog time-out

Page 37 of Data Sheet (Hot Socketing)
 Power Supplies can be sequenced in any order but must be monotonic
 All I/O lines are tri-stated during power cycling

Hysteretic Switching Power Supply

5V @ (2.5 Amps)

5-28V
Power In



Technologic Systems	Date	March 15, 2008
Title: TS-7350 5V Power Supply		
Rev:	Designer	Sheet 7 of 7