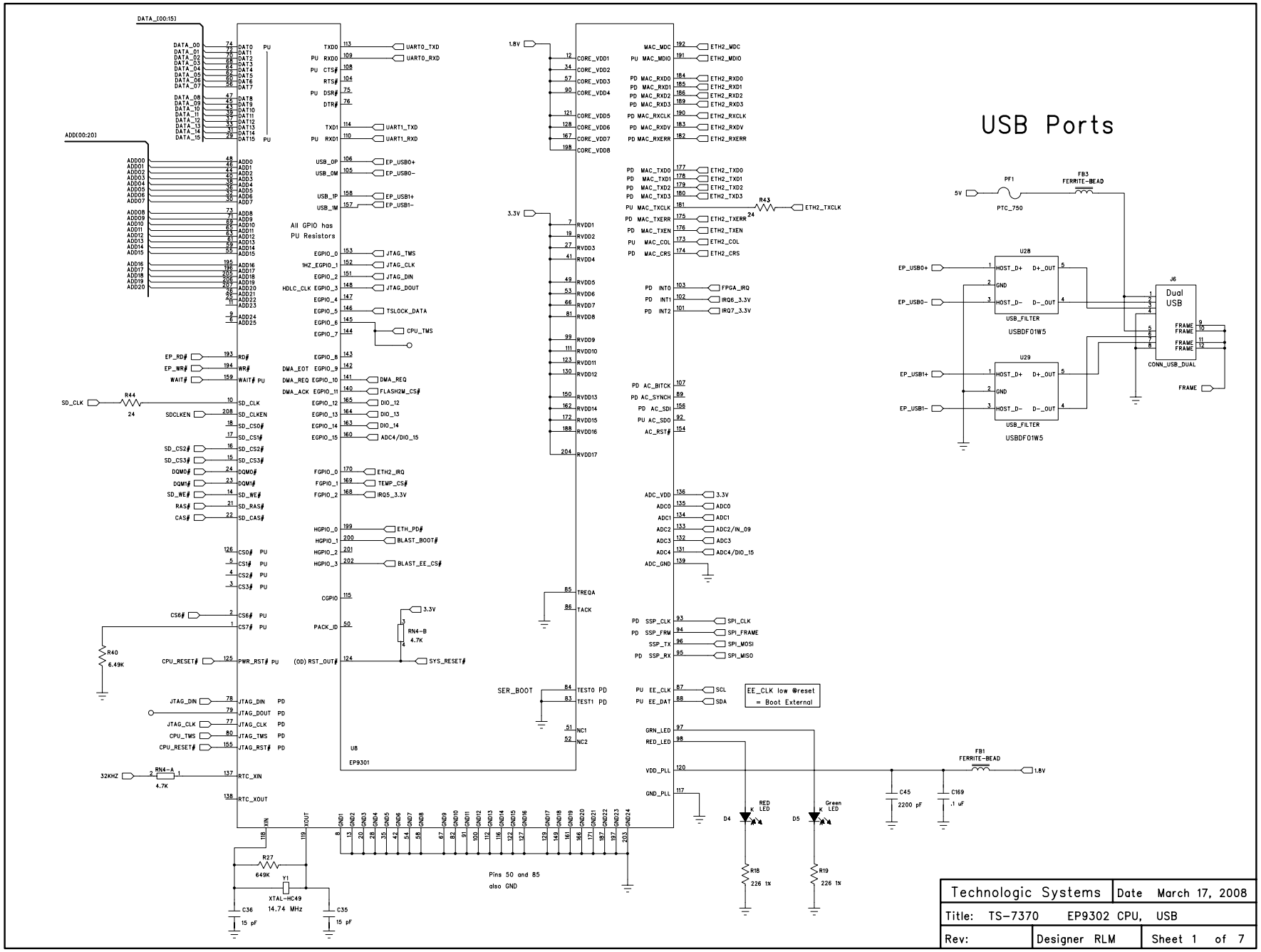
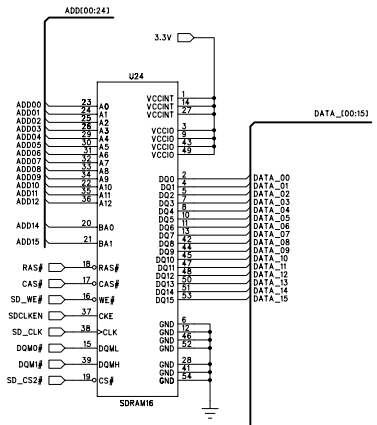
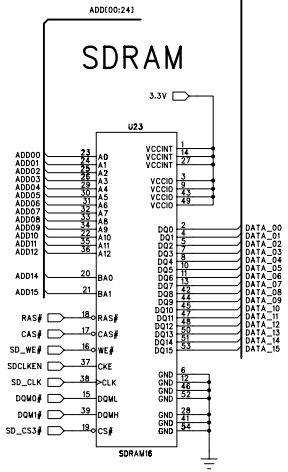

USB Ports
All GPIO has PU Resistors
Pins 50 and 85 also GND
EE_CLK low @reset = Boot External
U8
EP9301
U28
U29
USBDF01W5
CONN_USB_DUAL
Technologic Systems
Date March 17, 2008
Title: TS-7370 EP9302 CPU, USB
Rev:
Designer RLM
Sheet 1 of 7

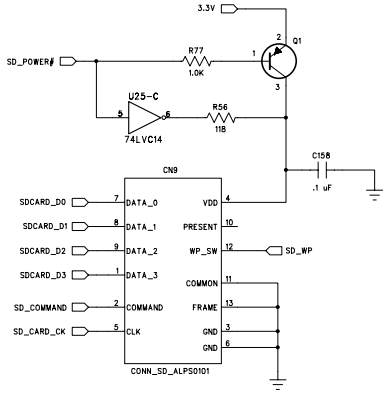
SDRAM

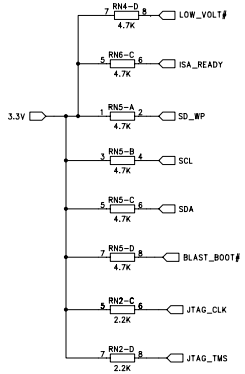


SDRAM

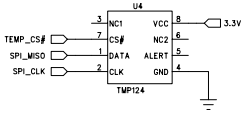


SD Card Socket

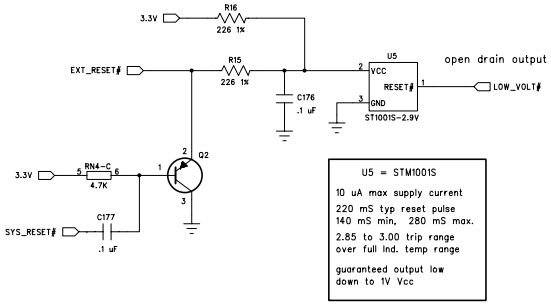




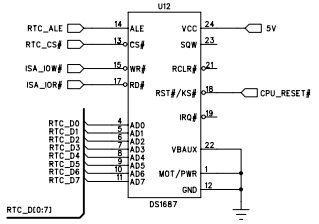
Temp Sensor



Power On Reset

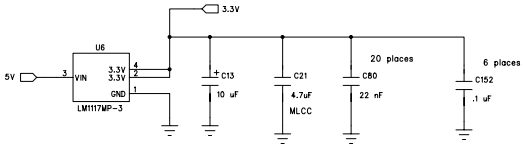


Battery-Backed Real Time Clock

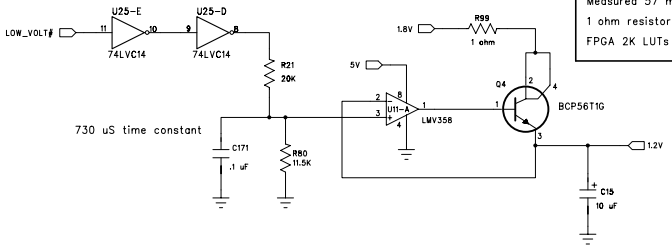


Technologic Systems	Date March 17, 2008	
Title: TS-7370 SDRAM, Flash, RTC, POR		
Rev:	Designer RLM	Sheet 2 of 7

3.3V Regulator

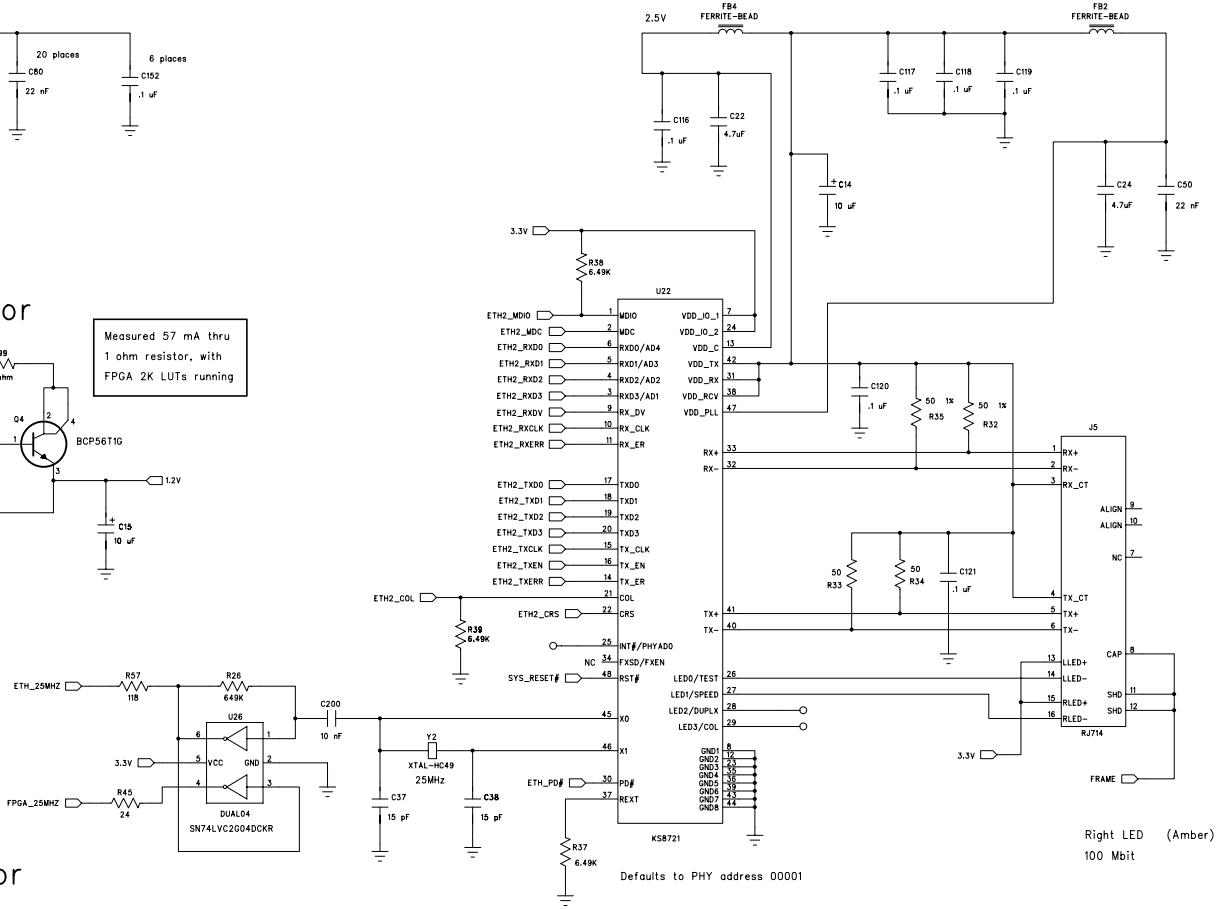


1.2V Regulator



Measured 57 mA thru
1 ohm resistor, with
FPGA 2K LUTs running

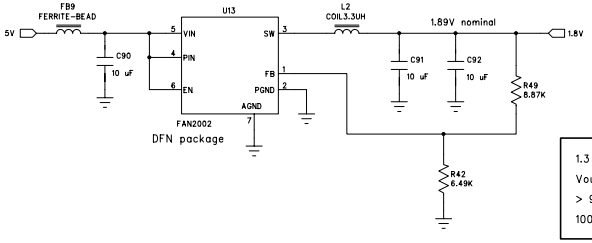
10/100 Ethernet



Right LED (Amber)
100 Mbit

Left LED (Green)
Link / Activity

1.8V Switching Regulator

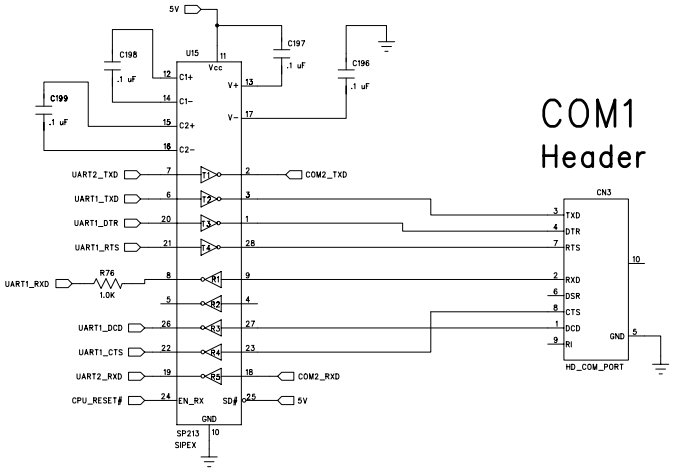


FAN2002

1.3 MHz freq. 50 uA quiescent
Vout = 800mV * (1+ Rtop/Rbot)
> 90% eff. at 100-400 mA load
1000 mA max load

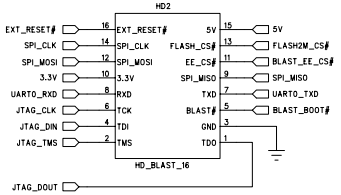
Technologic Systems		Date March 17, 2008
Title: TS-7370 Power Supplies, Ethernet		
Rev:	Designer RLM	Sheet 3 of 7

RS-232 Transceiver



COM1 Header

JTAG Header

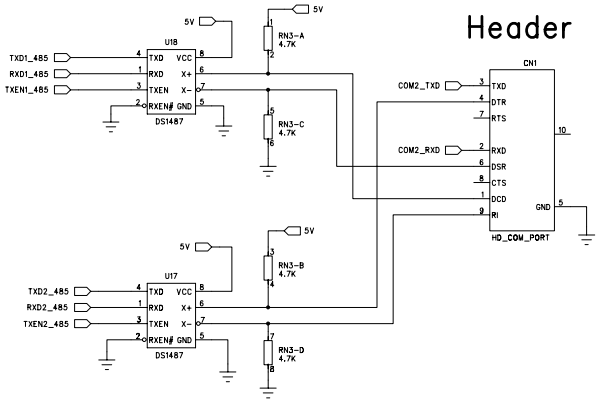


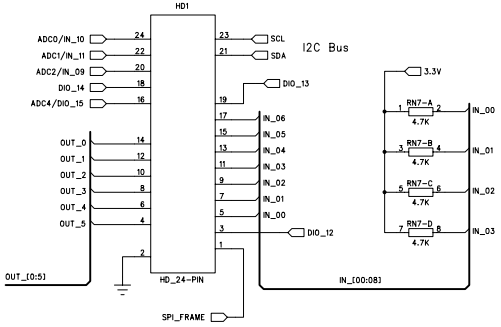
BLAST_EE_CS# is not used for booting -- FPGA Boot code has capability to boot from 2MB Serial Flash directly

Logic "0" on "BLAST_BOOT#" signal indicates Boot using TS-9444 2MB Flash

RS-485 Drivers

COM2 Header



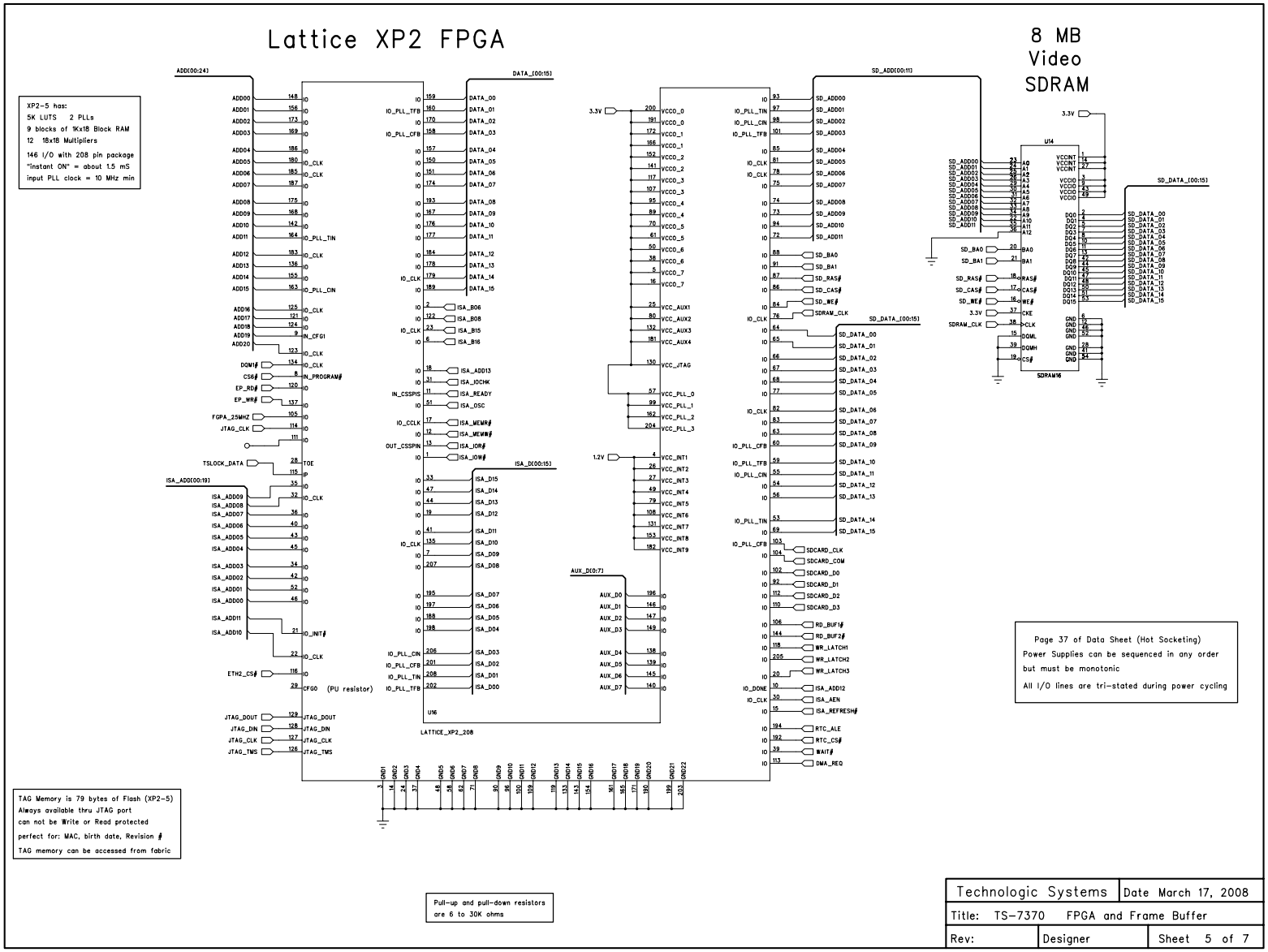


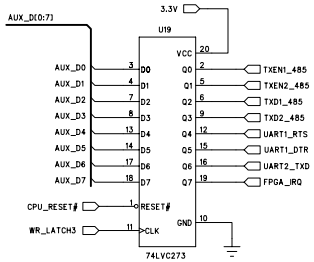
24-pin Header

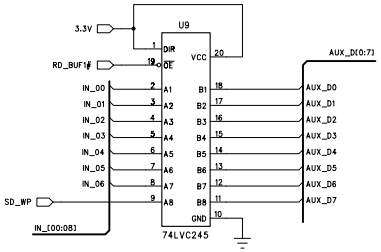
24 + 16 = 40-pin Header

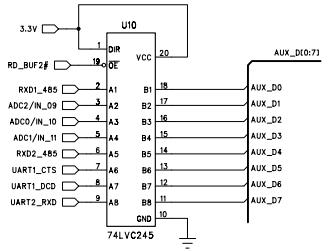
- 4 ADC
  ADC lines in parallel with IN_09, IN_10, IN11, DIO15
- 2 I2C
- 1 GND
- 6 Latched Outputs (OUT0-OUT5)
- 7 Buffered Inputs (IN0-IN6)
- 3 DIO_12, DIO_13, DIO_14
- 1 SPI_FRAME

Technologic Systems		Date March 17, 2008
Title: TS-7370 COM Ports DIO JTAG Headers		
Rev:	Designer	Sheet 4 of 7

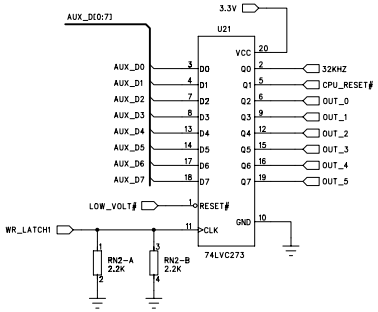

Lattice XP2 FPGA
8 MB Video SDRAM
XP2-5 has:
5K LUTS 2 PLLs
9 blocks of 1Kx18 Block RAM
12 18x18 Multipliers
146 I/O with 208 pin package
"Instant ON" = about 1.5 mS
input PLL clock = 10 MHz min
ADD[00:24]
DATA_[00:15]
SD_ADD[00:11]
SD_DATA_[00:15]
ISA_ADD[00:19]
ISA_D[00:15]
AUX_D[0:7]
LATTICE_XP2_208
SDRAM16
TAG Memory is 79 bytes of Flash (XP2-5)
Always available thru JTAG port
can not be Write or Read protected
perfect for: MAC, birth date, Revision #
TAG memory can be accessed from fabric
Pull-up and pull-down resistors are 6 to 30K ohms
Page 37 of Data Sheet (Hot Socketing)
Power Supplies can be sequenced in any order but must be monotonic
All I/O lines are tri-stated during power cycling
Technologic Systems
Date March 17, 2008
Title: TS-7370 FPGA and Frame Buffer
Rev:
Designer
Sheet 5 of 7

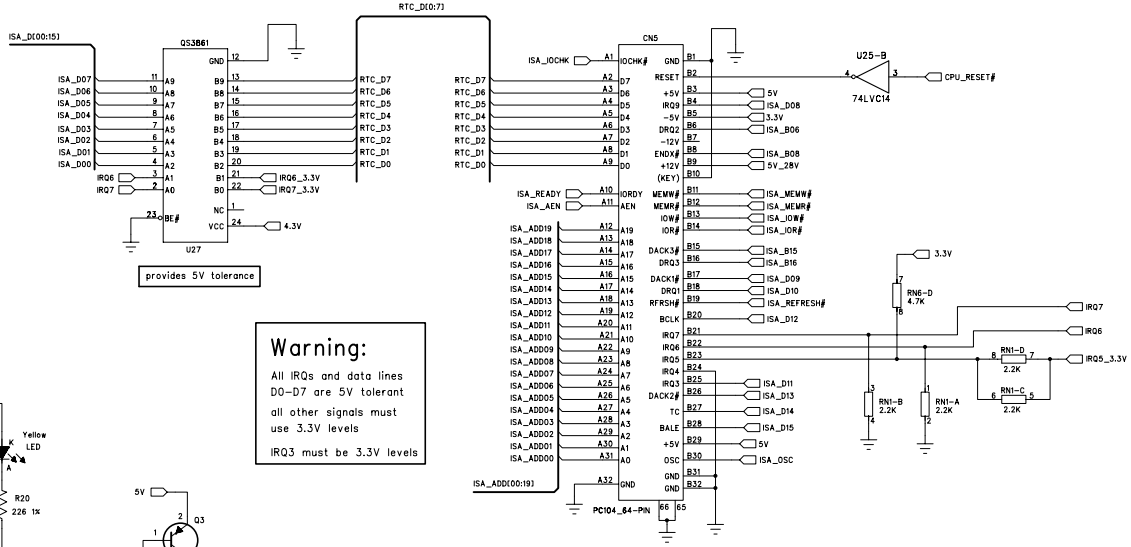


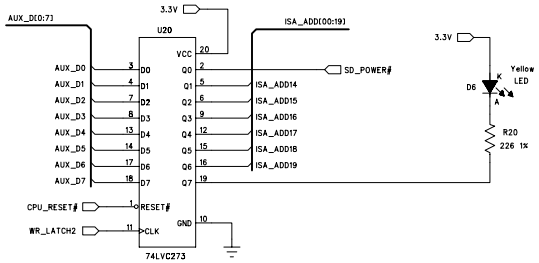


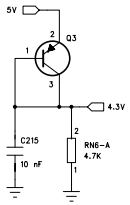


PC/104 64-pin Connector









Warning:

All IRQs and data lines D0–D7 are 5V tolerant

all other signals must use 3.3V levels

IRQ3 must be 3.3V levels

33 lines directly into FPGA

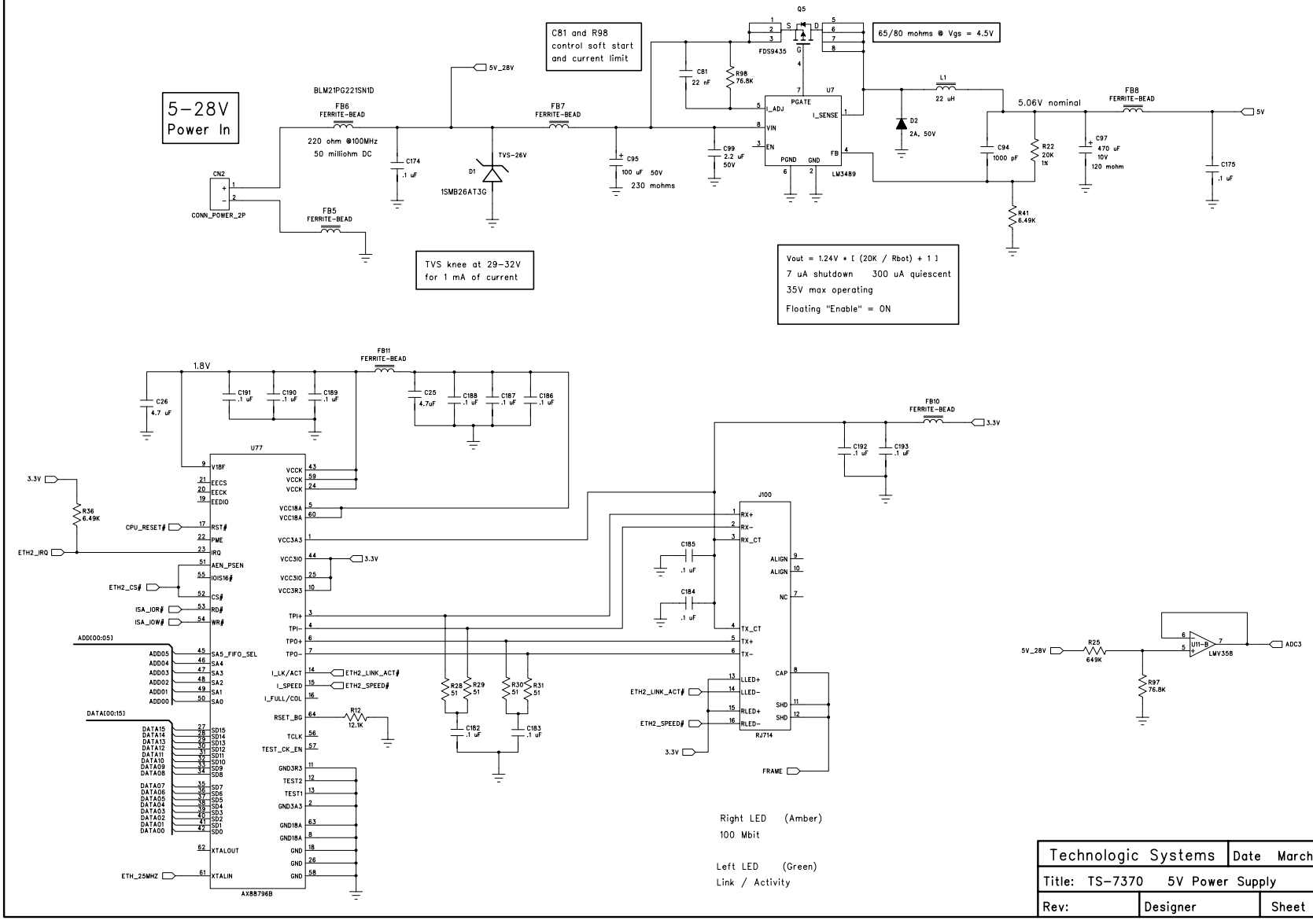
plus 10 more (D0–D7 and IOR, IOW) that can be used with no RTC option

plus 6 more from latch (A14–A19)

Technologic Systems		Date March 17, 2008
Title: TS-7370 PC/104 AUX Bus		
Rev:	Designer	Sheet 6 of 7

Hysteretic Switching Power Supply

5V @ (2.5 Amps)



Technologic Systems	Date March 17, 2008	
Title: TS-7370 5V Power Supply		
Rev:	Designer	Sheet 7 of 7