DIO after booting but can be switched after power up (or reset). Console always is enabled

CPU_RESET# is deasserted after active pull-ups on TS-7500.

MODE1 and MODE2 states are latched when FPGA is deselected.

MODE1 and MODE2 have 4k resistor pullups on TS-7500.

MODE0 and MODE1 always are active.

DIO bus default to DIO. May be switched to SPI function.

LED0 shows both activity and link.

44-Pin DIO Header (Bottom)

FPGA with 5000 LUTs

MODE1 and MODE2 states are latched when FPGA is deselected.

MODE1 and MODE2 have 4k resistor pullups on TS-7500.

DIO bus default to DIO. May be switched to SPI function.

LED0 shows both activity and link.

Power Supplies can be sequenced in any order but must be monotonic.

All I/O lines are tri-stated during power cycling.
The DDR clock differential pair is the most critical trace on the entire board.

The data lines in each byte lane can be swapped on the RAM chip for optimal layout.

Example: D0 and D9 can be swapped, but not D7 and D8.

The trace length of each data line (in a single byte lane) and the respective Q0 and DM signals must be matched to within 2.5 mm.

Address and Command signals can be grouped together, but must be isolated from data and M0, M1, M2 signals (by at least 5 mm).

Or run them on different layer.