### 512 Mbyte NAND Flash

#### DDR1 SDRAM

**DDR RAM Notes**

- The DDR clock differential pair is the most critical trace on the entire board.
- The data lines in each byte lane can be swapped on the RAM chip for optimal layout.
  - Example: D0 and D1 can be swapped, but not D7 and D8.
- The trace length of each data line (in a single byte lane) and the respective Qs and DM signals must be matched to within 2.5 mm.
- Address and Command signals can be grouped together, but must be isolated from data and M_SHQ and M_SM signals (by at least 3 mm).
- Or run them on different layers.

### 64 Mbyte DDR1 SDRAM

#### RTC

**RTC**

- 12 pF

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**NAND Flash**

- 512 Mbyte
- 64 Mbyte

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**DDR1 SDRAM Notes**

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- Or run them on different layers.
3.3V Regulator

1.2V Regulator

1.8V Regulator

2.5V Regulator