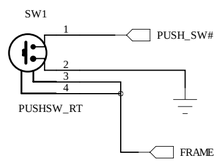
TS-7552

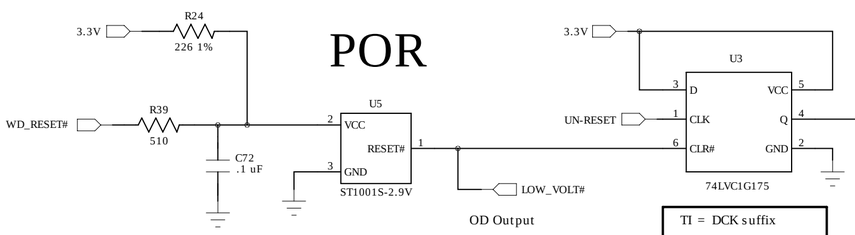
with 5 USB Ports

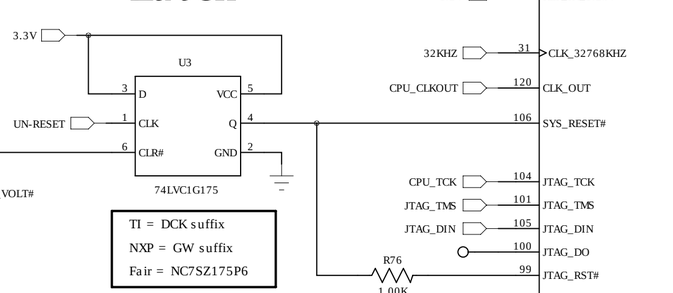
Push Switch

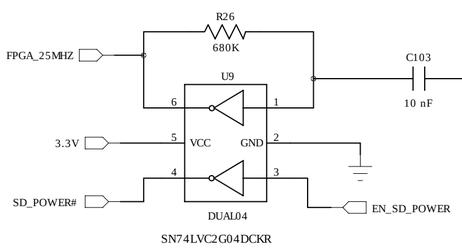


Reset Latch

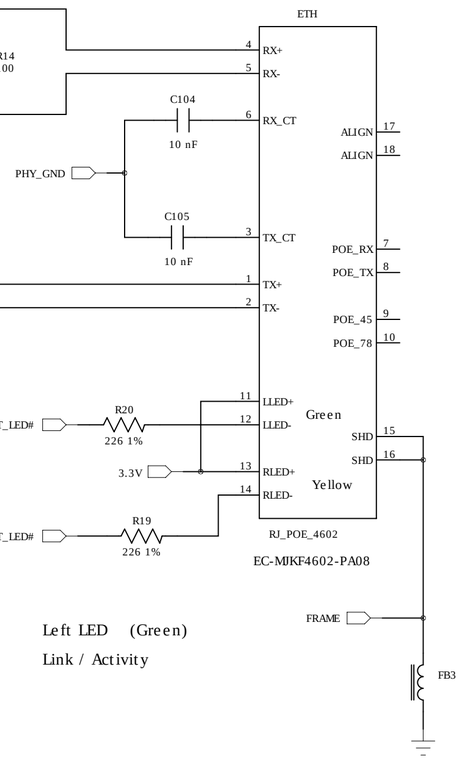
POR







10/100 Ethernet

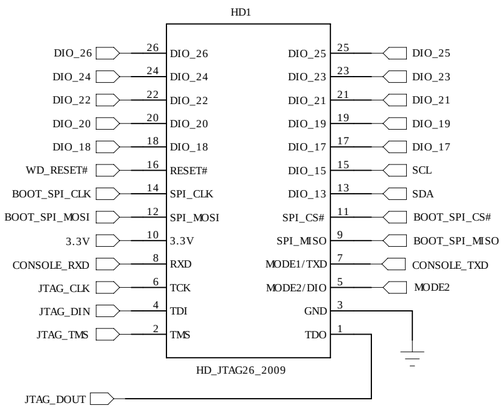


Strap Options

CLK_OUT	ICE mode (default high)
SPI_MOSI	Low = Little Indian
RAM_CKE	High = SPI Boot

Technologic Systems	Date Jan. 17, 2010	
Title: TS-7552 CPU, Ethernet, POR		
Rev:	Designer	Sheet 1 of 7

JTAG 26-pin Header



Mode 1	Mode 2	Boots from
1	1	NAND Flash
1	0	SD Card
0	1	Off-board Flash
0	0	Off-board Flash

MODE1 and MODE2 states are latched when CPU_RESET# is deasserted

Console always is enabled

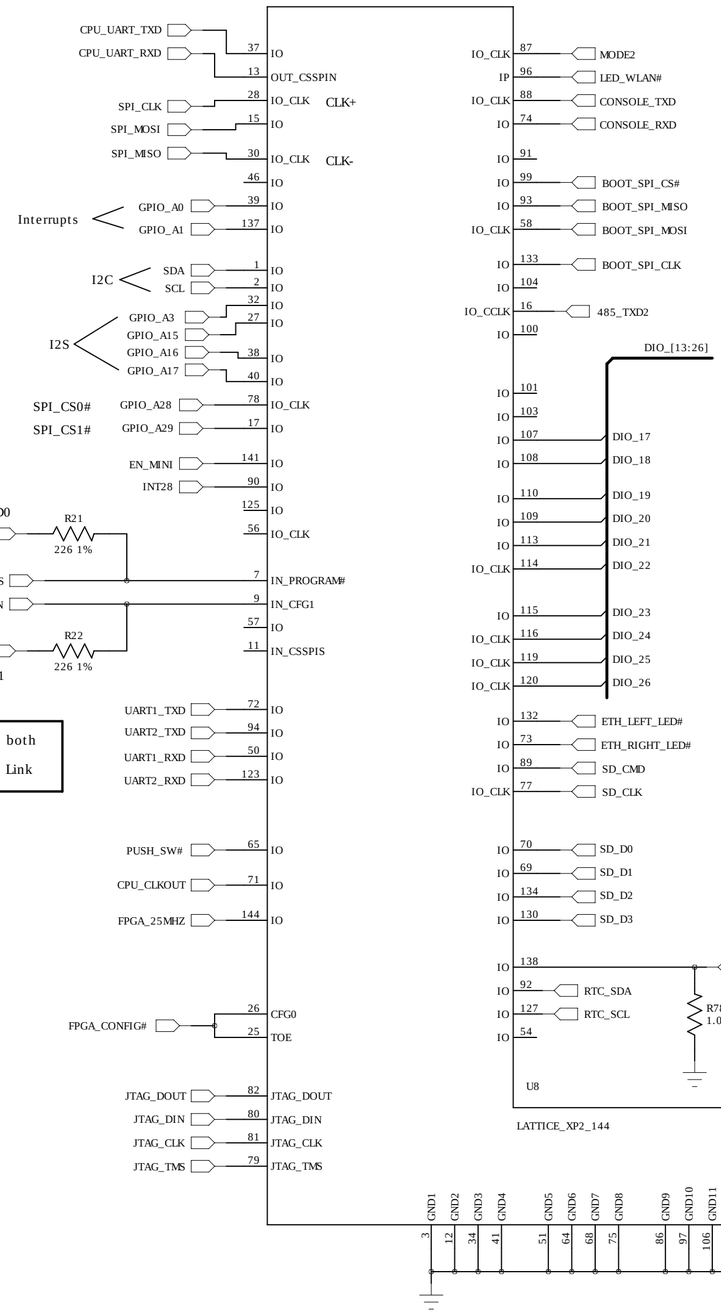
MODE1 and MODE2 have 4.7K resistor pull-ups on TS-7552

Use 680 ohm resistor to GND to set low

FPGA with 5000 LUTs

XP2-5 has:
5K LUTS 2 PLLs
9 blocks of 1Kx18 Block RAM
12 18x18 Multipliers

100 I/O with 144 pin package
"instant ON" = about 1.5 mS
input PLL clock = 10 MHz min



Board ID bits

	Pin 54 (weak PU)	Pin 138 (weak PD)	Pin 71	Pin 37
TS-7500	1	1	1	1
TS-7550	1	1	0	1
WM-7551	0	0	1	1
TS-7552	1	0	1	1
Module #1	0	0	0	0

LED0 shows both Activity and Link

UN-RESET rising edge, deasserts CPU Reset
(Must be careful at start up)
It has a PD resistor -- always keep low

EN_SD_POWER should initialize high

During JTAG Flash programming the PROGRAM# pin should be high else it can inhibit Flash --> SRAM

DONE likewise must be high
These do have weak PU resistors

PROGRAM#, DONE, and INIT# are dedicated configuration pins when CFG0 is low. When CFG0 is high they are "general purpose I/O"

Page 4 of TN1141

Set CONFIG_MODE to NONE
This allows all pins to be used

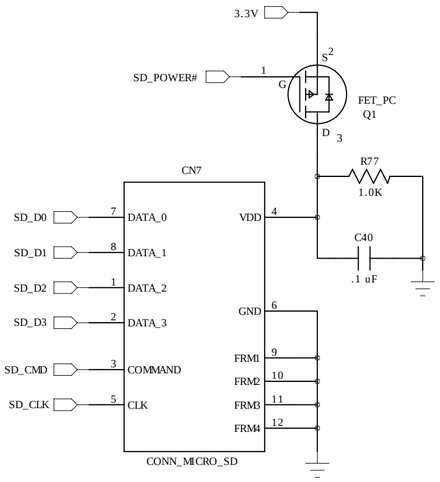
Pull-up and pull-down resistors are 6 to 30K ohms

Page 37 of Data Sheet (Hot Socketing)
Power Supplies can be sequenced in any order but must be monotonic

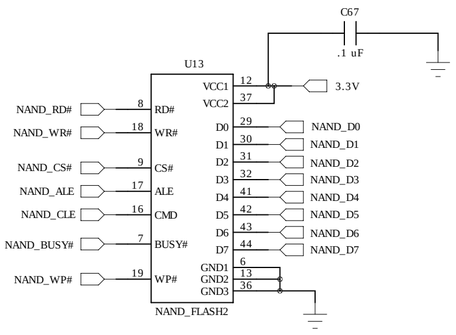
All I/O lines are tri-stated during power cycling

Technologic Systems	Date Jan. 17, 2010	
Title: TS-7552 FPGA, JTAG Header		
Rev:	Designer RLM	Sheet 2 of 7

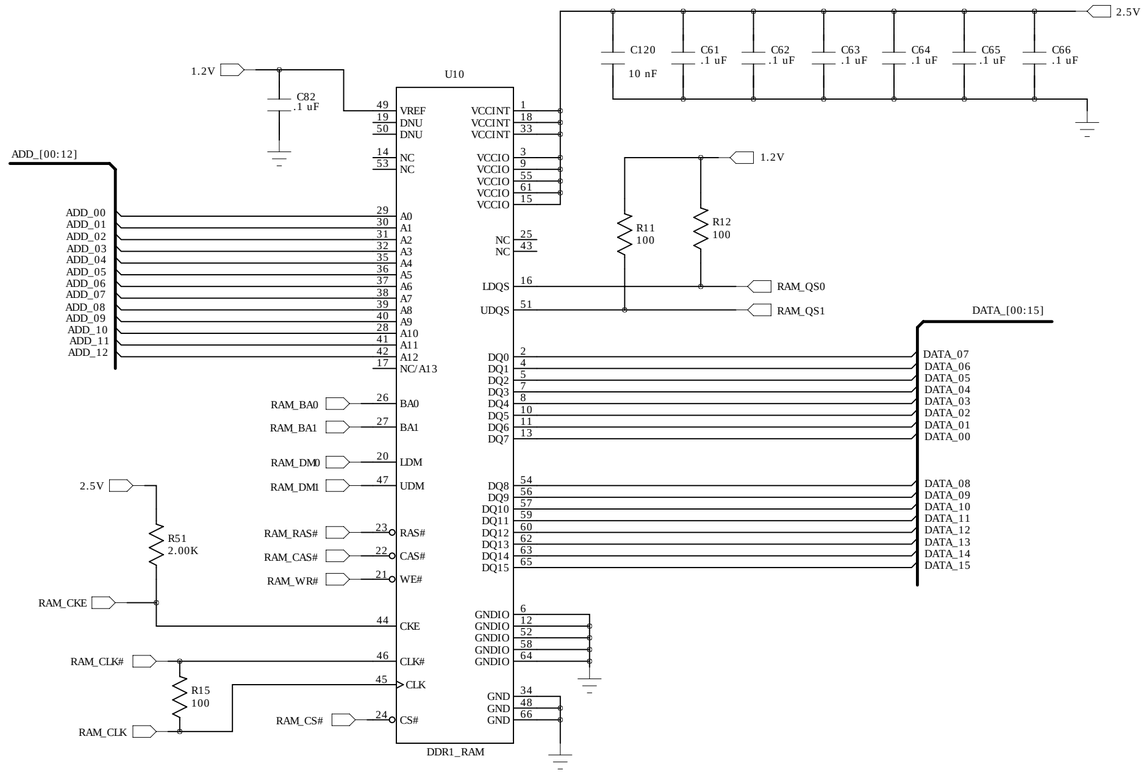
Micro SD Card Socket



512 Mbyte
NAND Flash



64 Mbyte
DDR1 SDRAM



DDR RAM Notes

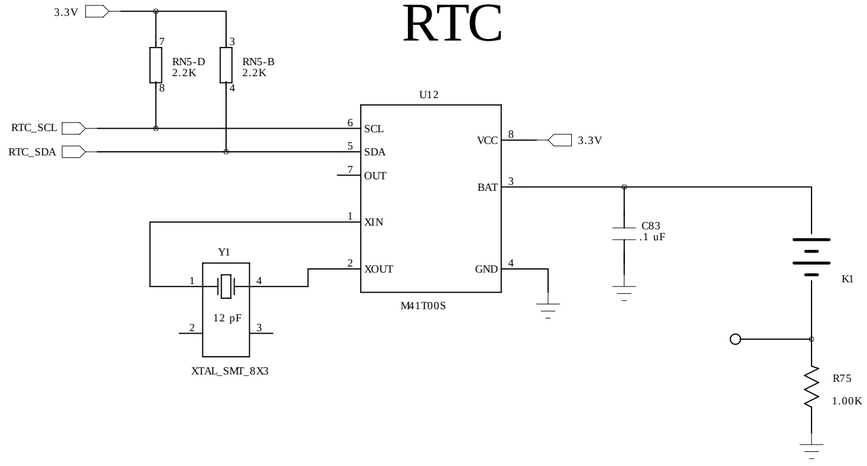
The DDR clock differential pair is the most critical trace on the entire board

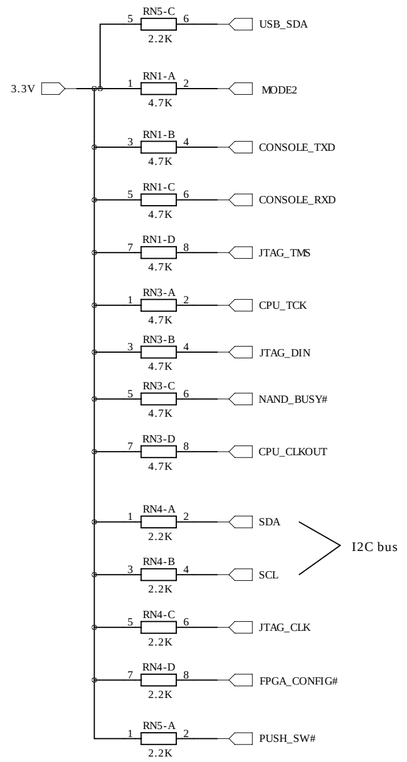
The data lines in each byte lane can be swapped on the RAM chip for optimal layout
Example: D0 and D5 can be swapped, but not D7 and D8

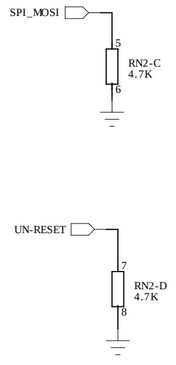
The trace length of each data line (in a single byte lane) and the respective QS and DM signals must be matched to within 2.5 mm

Address and Command signals can be grouped together, but must be isolated from data and M_DSQ and M_DM signals (by at least .5 mm)
Or run them on different layer

RTC

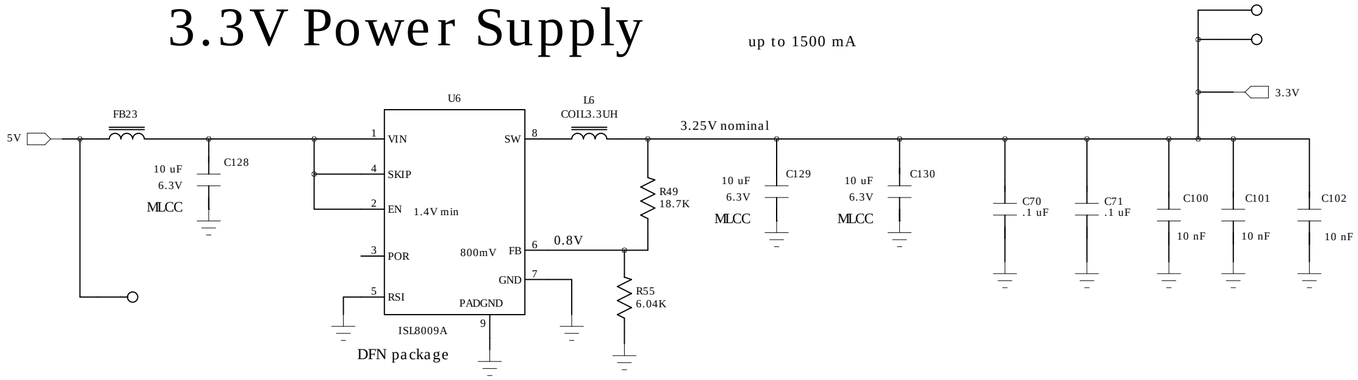






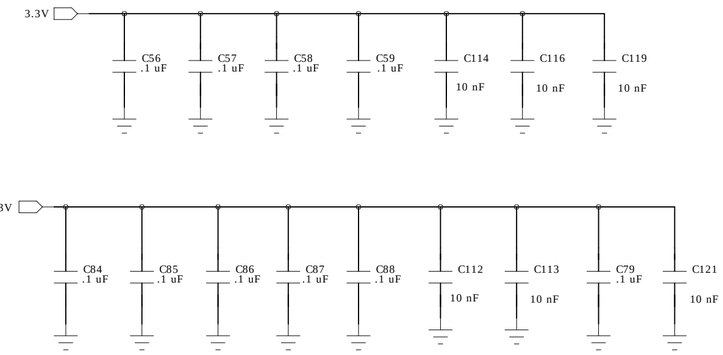
Technologic Systems	Date Jan. 17, 2010	
Title: TS-7552 RAM, RTC, Flash		
Rev:	Designer	Sheet 3 of 7

3.3V Power Supply

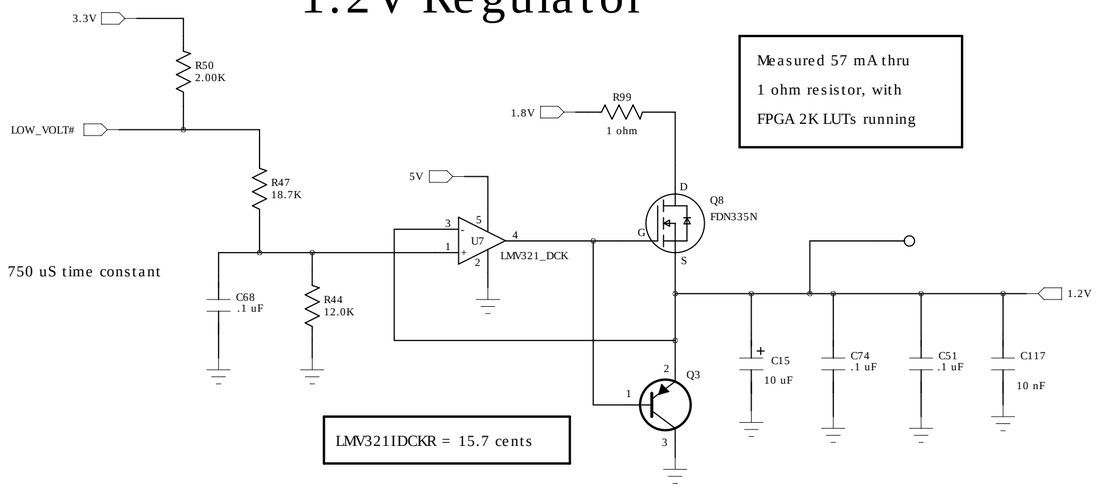


L6 = LQH44PN3R3

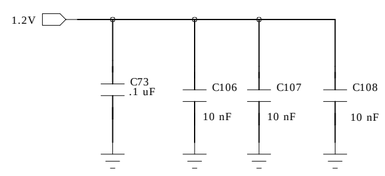
Max. current = 1.7 Amps



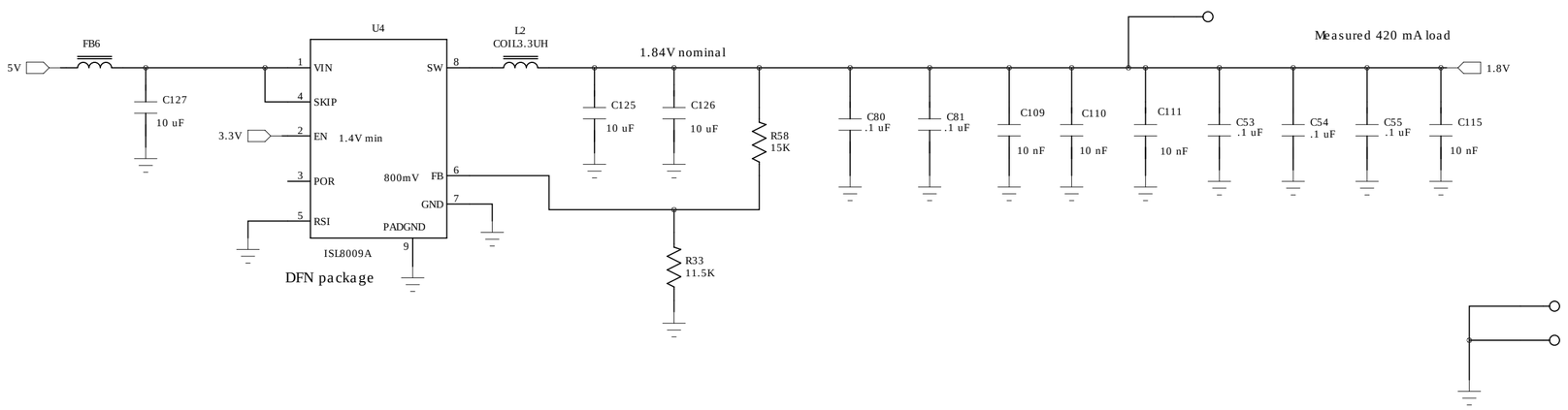
1.2V Regulator



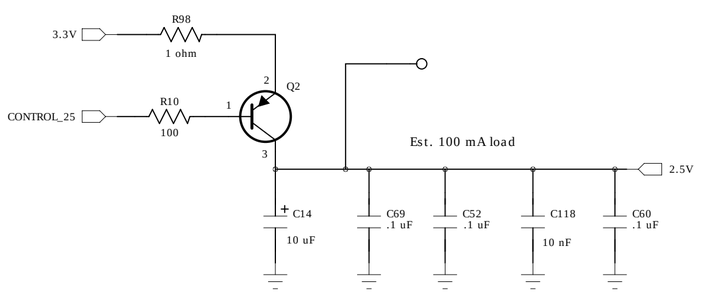
Measured 57 mA thru
1 ohm resistor, with
FPGA 2K LUTs running



1.8V Regulator

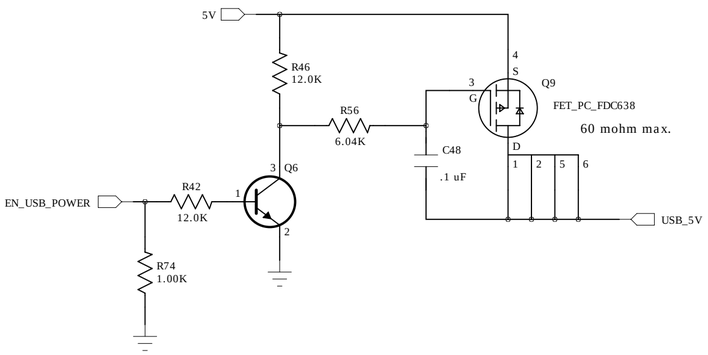


2.5V Regulator

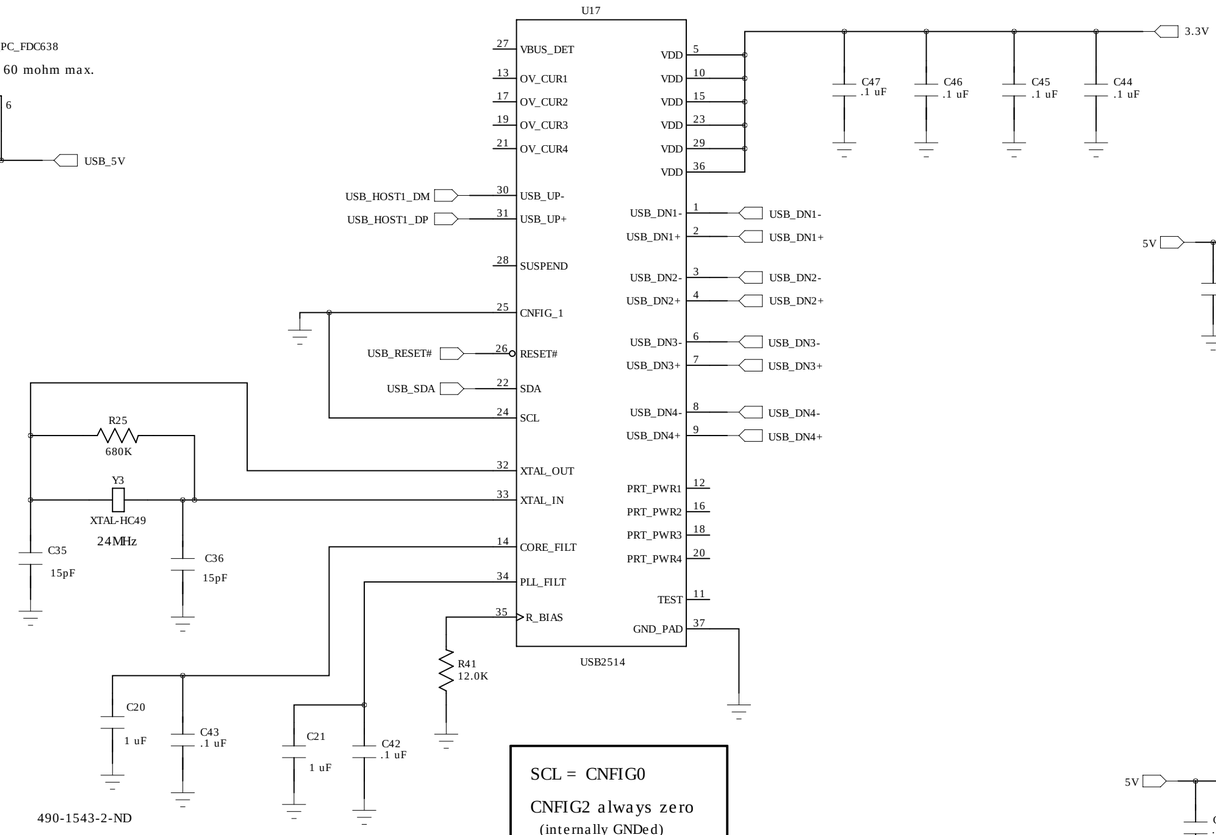


Technologic Systems	Date Jan. 17, 2010	
Title: TS-7552 Power Supplies		
Rev:	Designer RLM	Sheet 4 of 7

USB Power Switch



USB Hub

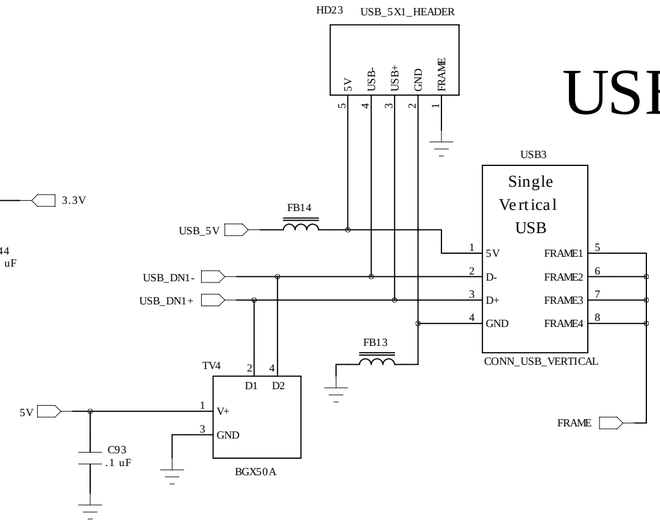


SCL = CNFIG0

CNFIG2 always zero
(internally GNDed)

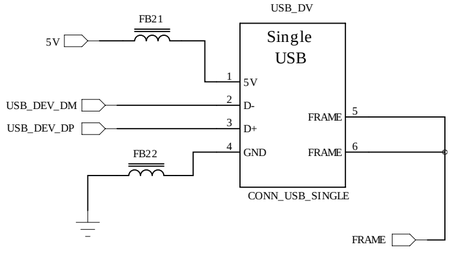
CFG0 and CFG1 both low =
self-powered and default mode
verified this is good strapping

USB 3

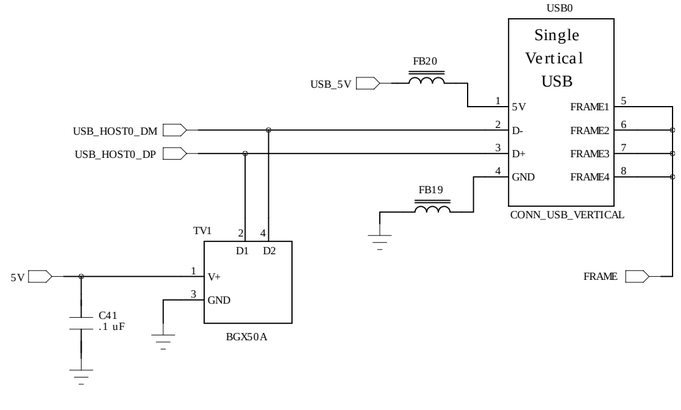


USB 2

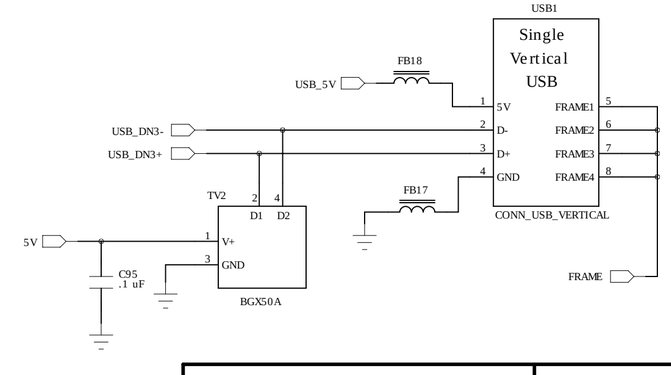
USB Device Port



USB 0



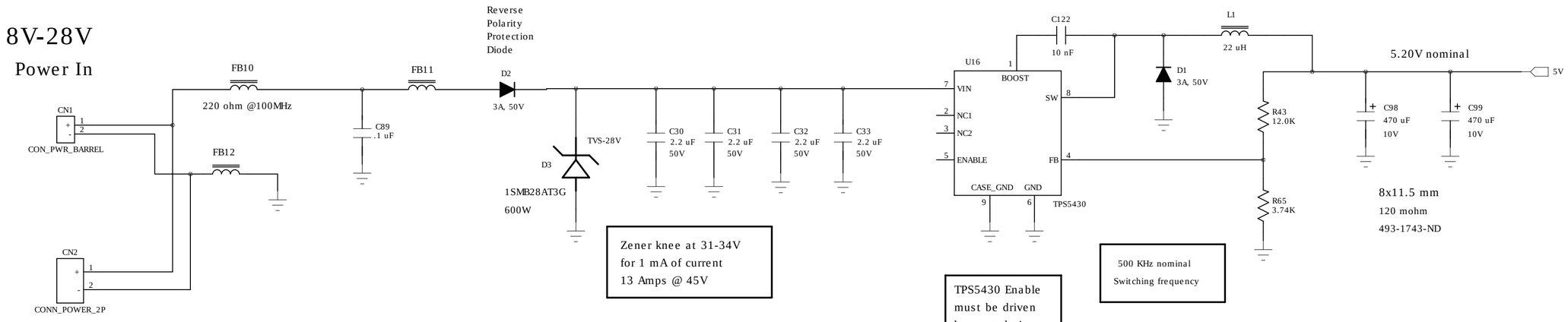
USB 1



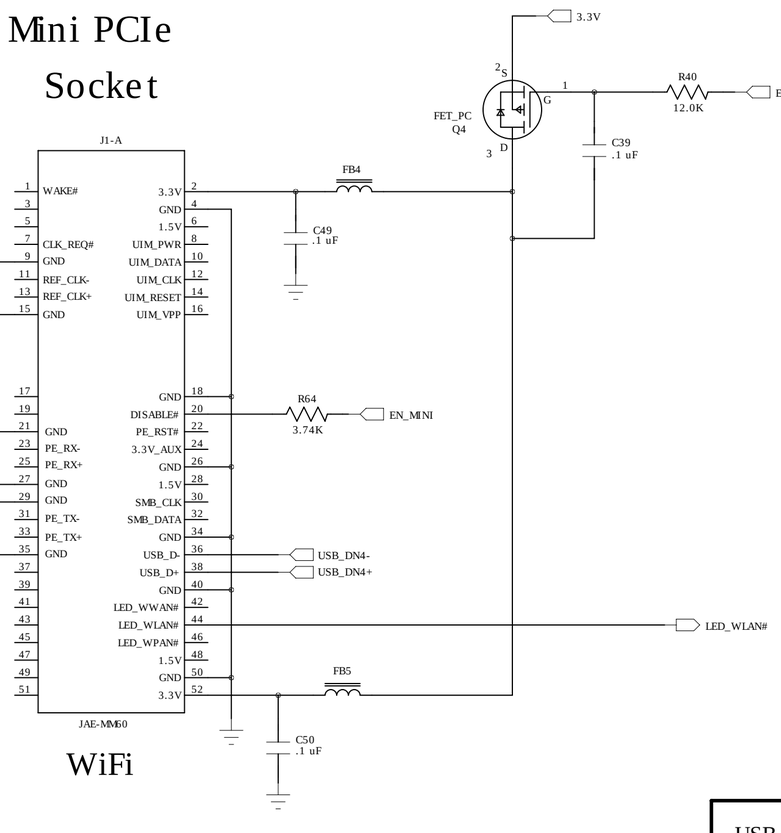
Technologic Systems		Date Jan. 17, 2010
Title: TS-7552 USB Hub		
Rev:	Designer	Sheet 5 of 7

5V Power Supply (2.6 Amps)

8V-28V Power In

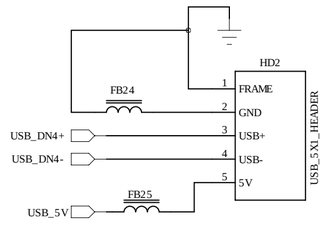


Mini PCIe Socket

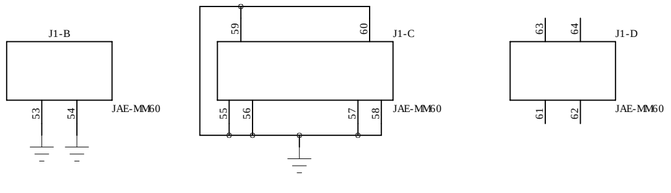


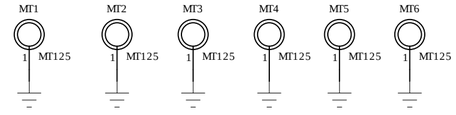
WiFi

USB4 Header

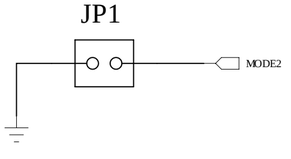


USB pair should have
90 ohm impedance





Force Boot to SD card



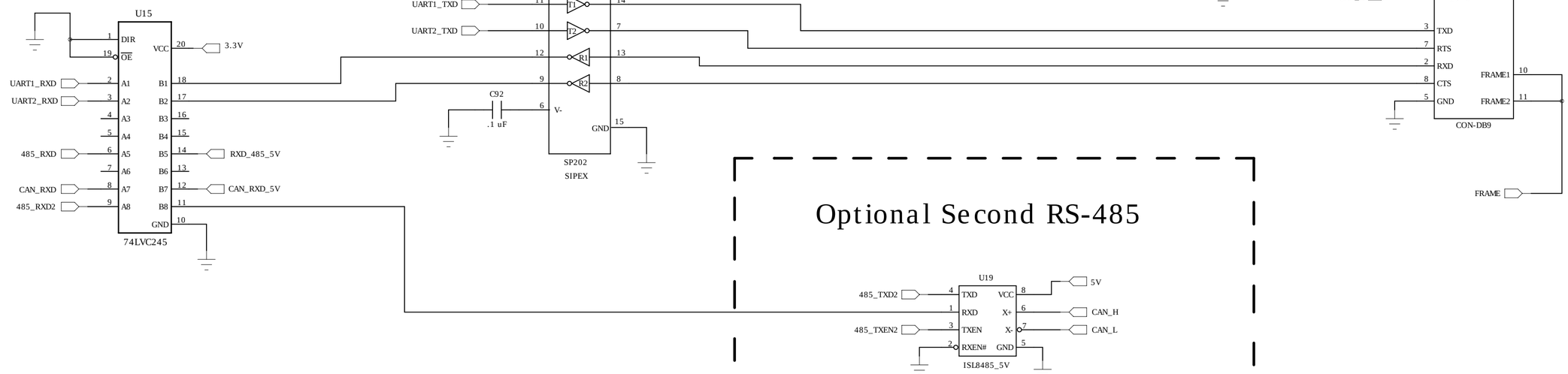
Technologic Systems	Date Jan. 17, 2010	
Title: TS-7552 7-28V to Reg. 5V Supply		
Rev:	Designer RLM	Sheet 6 of 7

RS-232 Transceiver

RS-485 Driver

COM
DB9M

5V --> 3.3V
Level shifter



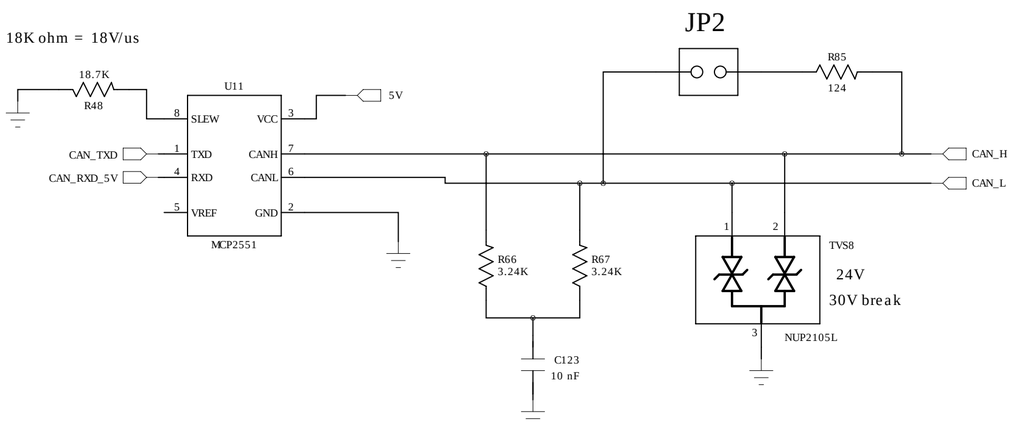
Optional Second RS-485

This chip is not normally populated

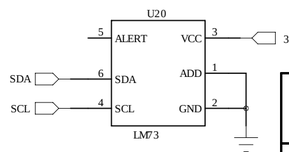
If it is, then CAN must be de-populated

CAN Tranceiver

18K ohm = 18V/us



Temp Sensor



Zero suffix has address at 100 1001

Best to Reset after all power cycles

Set PD bit, Wait 50 mS Then clear PD bit

Technologic Systems	Date Jan. 17, 2010	
Title: TS-7552 COM port, CAN, RS-485		
Rev:	Designer RLM	Sheet 7 of 7