**Micro SD Card Socket**

**64 Mbyte DDR1 SDRAM**

**512 Mbyte NAND Flash**

**DDR RAM Notes**

The DDR clock differential pair is the most critical trace on the entire board.

The data lines in each byte lane can be swapped on the RAM chip for optimal layout.

Examples: DD and DS can be swapped, but not D7 and D8

The trace length of each data line (in a single byte lane) and the respective Q5 and DW signals must be matched to within 2.5 mm.

Address and Command signals can be grouped together, but must be isolated

- from data and M_DQS and M_DW signals (by at least .5 mm)
- or run them on different layers

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**Technologic Systems**

**Title:** TS-7553 RAM, RTC, Flash

**Date:** Feb. 24, 2010

**Rev:**

**Designer:**

**Sheet:** 3 of 7
RS-232 Transceiver

3.3V --- 5V
Level shifter

RS-485 Driver

COM DB9M

Optional Second RS-485

This chip is not normally populated.
If it is, then CAN must be de-populated
and Xbee radio cannot be used.

CAN Transceiver

Temp Sensor

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