The DDR clock differential pair is the most critical trace on the entire board.

The data lines in each byte lane can be swapped on the RAM chip for optimal layout. Example: D0 and D1 can be swapped, but not D7 and D8.

The trace length of each data line (in a single byte lane) and the respective Q5 and DM signals must be matched to within 2.5 mm.

Address and Command signals can be grouped together, but must be isolated from data and M_DSQ and M_DM signals (by at least .5 mm) or run them on different layers.

Example: D0 and D5 can be swapped, but not D7 and D8.
5V Power Supply (2.0 Amps)

Input Power

5.0V to 30V

Power Conn.

5V
USB Power Switch

Temp Sensor

16 MB Phase
Change memory

Push Switch

Dual USB Host

Force Boot to SD card

SD Boot
4 Isolated Outputs

ISO_OUT # 1

ISO_OUT # 2

ISO_OUT # 3

ISO_OUT # 4

Outputs rated for 200 mA at 40V max.

Buffer for Isolated Inputs

5V → 3.3V
Isolated Inputs

32V tolerant
50 KHz Bandwidth

Logic high = 3V-30V
4 Channels of 12-bit A/D

R115-R118 not normally Populated

Precision 3.3V Reg.

12-bit ADC

Op Amp gain = 1 or 2.
Gain = 2 for 0-5V range

R115-R118 not normally Populated

ADC notes
Input Impedance = 70 Kohm
TVS adds 1000-3000 pF

typ. MUX ON resistance = 120 ohm
typ. Delta between chan = 10 ohm

Reading channel 0 allows calibrating out most error
2x20 positions of Screw Terminals

Top Row

Bottom Row