All JTAG have 47K internal pull resistors except RTCK.
FPGA with 5K LUTs

NAND Bus from CPU

SD Card LEDs

JTAG

On Bd. RA LEDs

Console

Page 37 of Data Sheet (Hot Sockeiting)
Power Supplies can be sequenced in any order but must be monotonic.
All I/O lines are tri-stated during power cycling.
Aux. 3.3V Reg

FPGA 1.2V Reg.
RTC and Reset Sequencer

RTC and Temp. Sensor

BAT must be > 2.7V for temp comp to work

Temp takes 68 uA for 22 ms
Once every 1 or 10 min.

Analog Inputs

FPGA Bypass Caps

Title: TS-7600 Boot Flash, RTC, Reset
Rev: A Designer Sheet 4 of 6
44-Pin DIO Header

MODE and MODE2 states are latched when CPU_RESET# is deasserted.

MODE1 and MODE2 have 4.7K resistor pull-ups on TS-7500.

Logic '0' on MODE2 signals boot from SD card.

Logic '0' on MODE1 forces Console onto the TXD and RXD lines.

USB Host Ports

USB Device Port