Rev. A --> Rev. B

Connected CAN bus to FPGA
CPU changed to MX286

Audio
SD Card
SPI Boot

NAND, PWM
JTAG, I2C
PSWITCH can be driven to 3.3V if a series 10K resistor is used.

USB

FPGA is fully functional when CPU Reset# deasserted.
MX283

DDR2 SDRAM (128 or 256 MByte)

MX283

64M x 16
128 MB

OR

128M x 16
256 MB

Title: TS-7600 DDR2 RAM

Technologic Systems

Date: May 20, 2014

Rev. B

Designer

Sheet 3 of 9
Auto MDIX is supported and Polarity Correction supported
RTC and Reset Sequencer

RTC and Temp. Sensor

FPGA Bypass Caps

Analog Inputs

BAT must be > 2.7V for temp comp to work
Micro SD Card Sockets

SD LEDs

SPI Boot Flash

Red/Green LEDs
44-Pin DIO Header

MODE1 and MODE2 states are latched when CPU_RESET# is deasserted.

MODE1 and MODE2 have 4.7K resistor pullups on TS-7500.

Logic '0' on MODE2 signals return Boot from SD card.

Logic '0' on MODE1 returns Console output to the TXD and RXD lines.

USB Device Port

USB Host Ports

Technologic Systems
Date: May 20, 2014
Title: TS-7600 44-pin DIO and USB
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