

# Comments:

Cortex M0 can be powered from USB or by 8-28VDC Power  
 If D8 installed, then MX286 can be powered by USB power  
 Cortex M0 is powered up first, then it controls MX286 start up  
 Cortex M0 does these functions:

- Controls MX286 power up sequence
- Controls MX286 Boot Strapping
- USB Device to Console conversion
- Controls Blue LED
- Can read Push Switch
- Measures Analog Vin value
- Reads SD\_BOOT Jumper
- Contains customer specific "ID Code" ?
- Other NV Parameter storage ?

MX286 UART0 supports RTS/CTS hardware flow control

Rev.A Problem -- FB20 and FB28 have bad Silkscreen

# Notes:

- 1) How do we do WatchDog ?  
 If MX286 uses internal WD, then we must keep BATT\_LOAD# asserted all the time - about 3 mA
- 2) Where is MAC address stored ?  
 Is it better to have it in M0 ?
- 3) For Modbus 1024K baud operation - must use DMA  
 Serial Port RX DMA on MX286 says "must be multiples of 4 bytes"  
 TX DMA does not say restricted to 4 byte multiples

Page 1944

## GPS option adds:

U14, PF2, L4, HD3

## 2nd CAN adds:

U26 and TVS6

## Quebec Gov't

HD2 only pop for them  
 No Modbus  
 128MB RAM, one CAN, GPS pop  
 MX286 CPU (extended temp)  
 Needs Ext. Temp 1GB SD card

## Serial Port Usage

UART0 = RS-232  
 UART1 = RS-232  
 UART2 = Modbus/DC  
 UART3 = DC  
 UART4 = GPS Radio  
 Debug = Console/DC

DC = Daughter Card  
 10 DIO also go to DC

Rev.A has no A/D from CPU

## Standard TS-7670

DNP: RN14, RN24, RN25, R65, HD2  
 2nd CAN port is an option  
 GPS Radio is an option  
 FB7 not Pop, U7 is populated  
 use MX286 CPU  
 128MB and 256MB RAM sizes

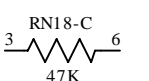
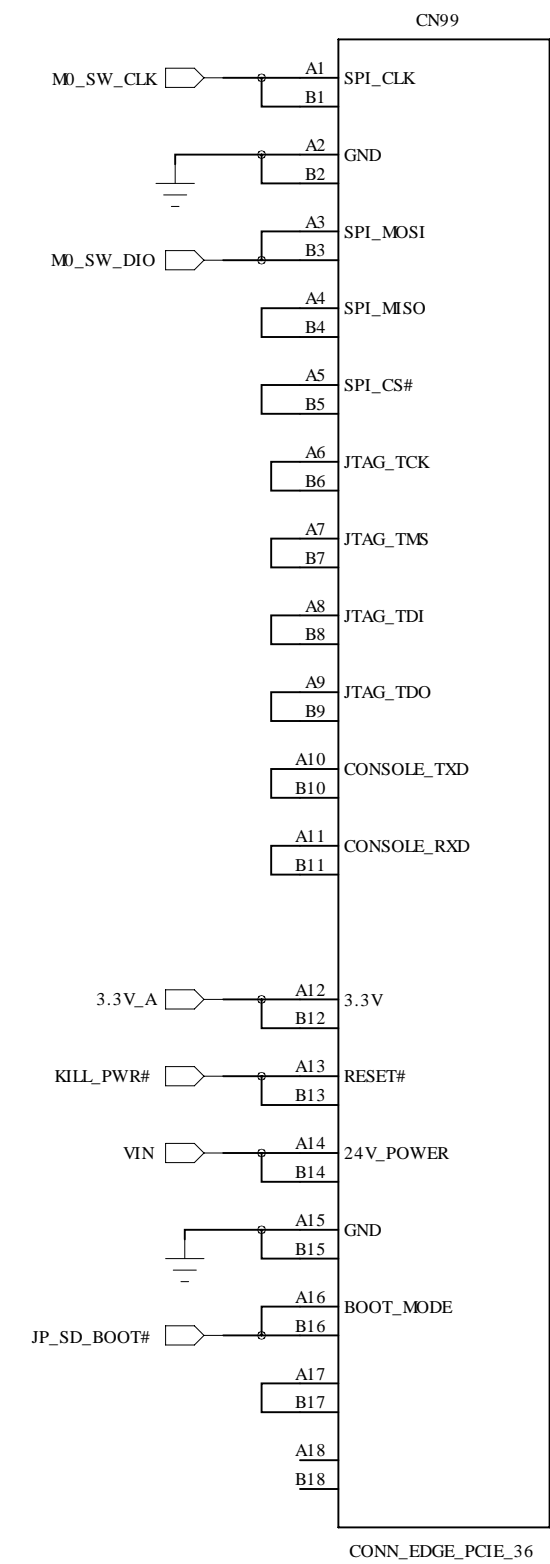
### BOM Warning:

Never Pop. FB28  
 Two 2x1 --> Single 2x2

## Drop-Tank.com

Requires special BOM                      Use MX283 CPU ?  
 No RTC, No CAN, No Modbus, One SD card, 256 MB RAM  
 Install: RN14, RN24, RN25, R65            ] non-std serial pinout  
 Remove: RN21, RN22, RN23

# Programmer Edge Conn.

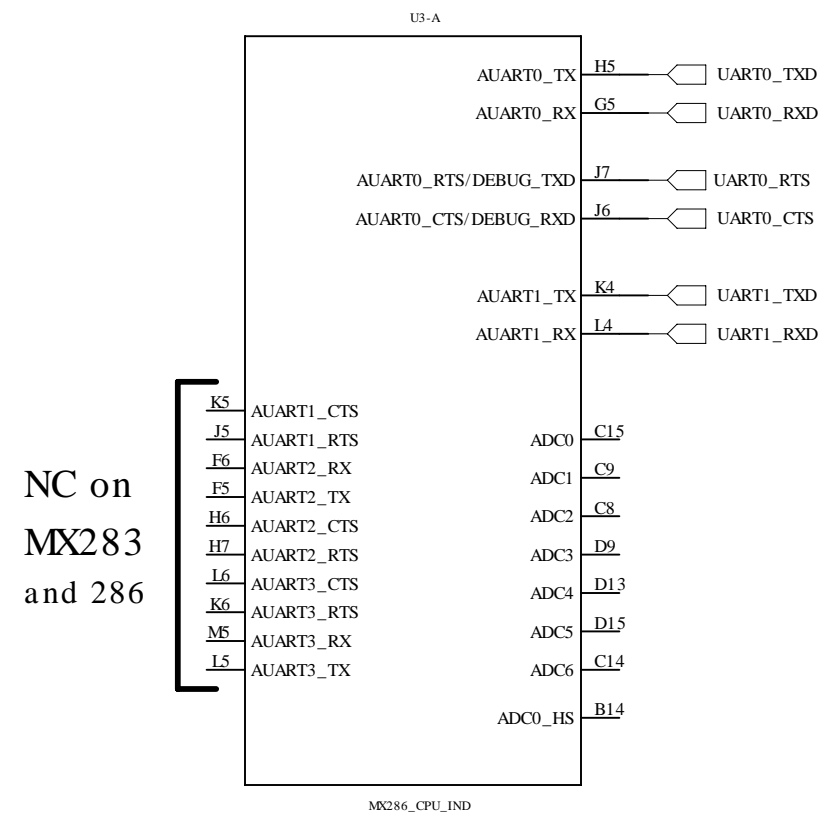


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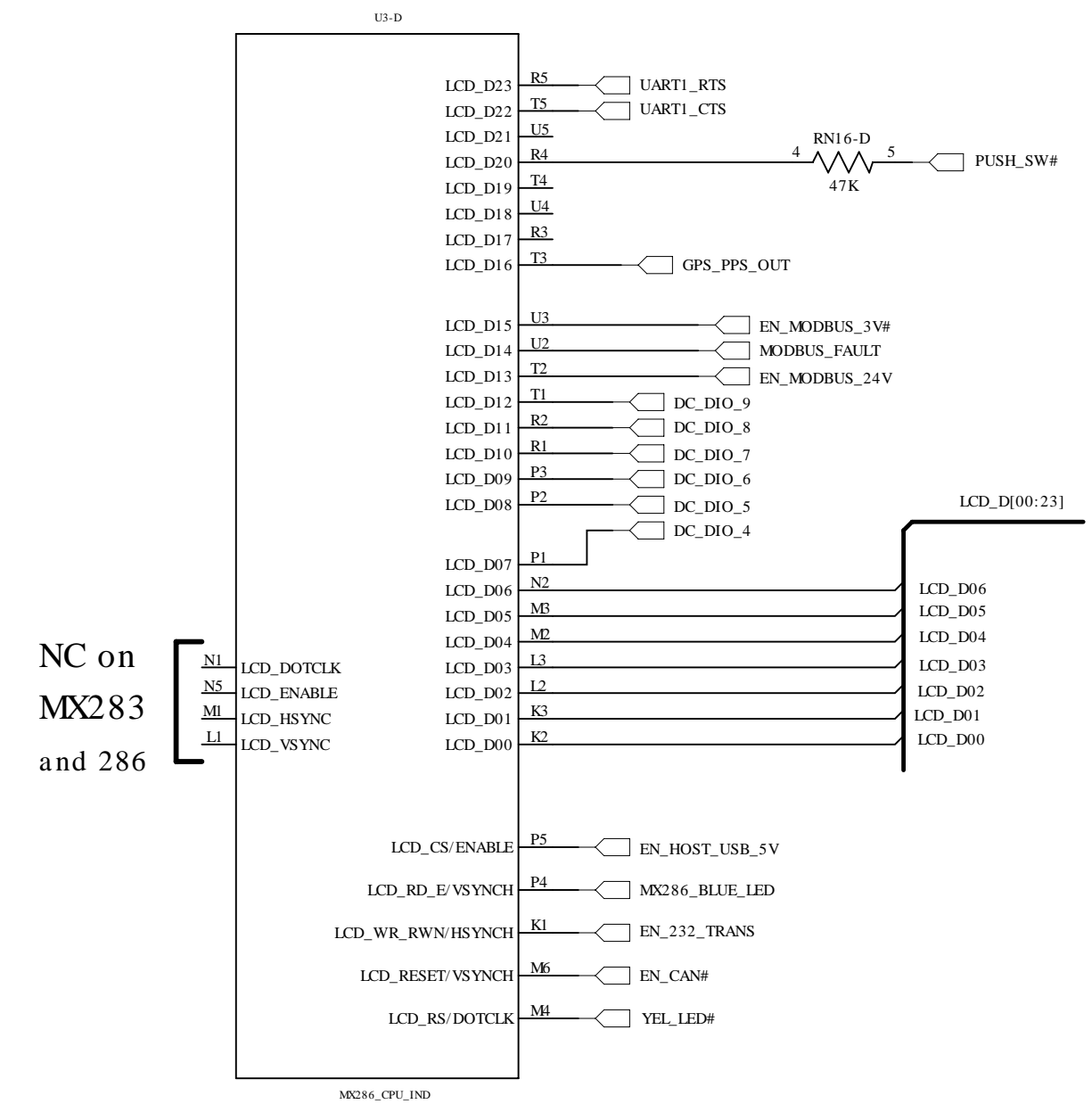


# MX286 ARM9 CPU

## UARTs, ADC

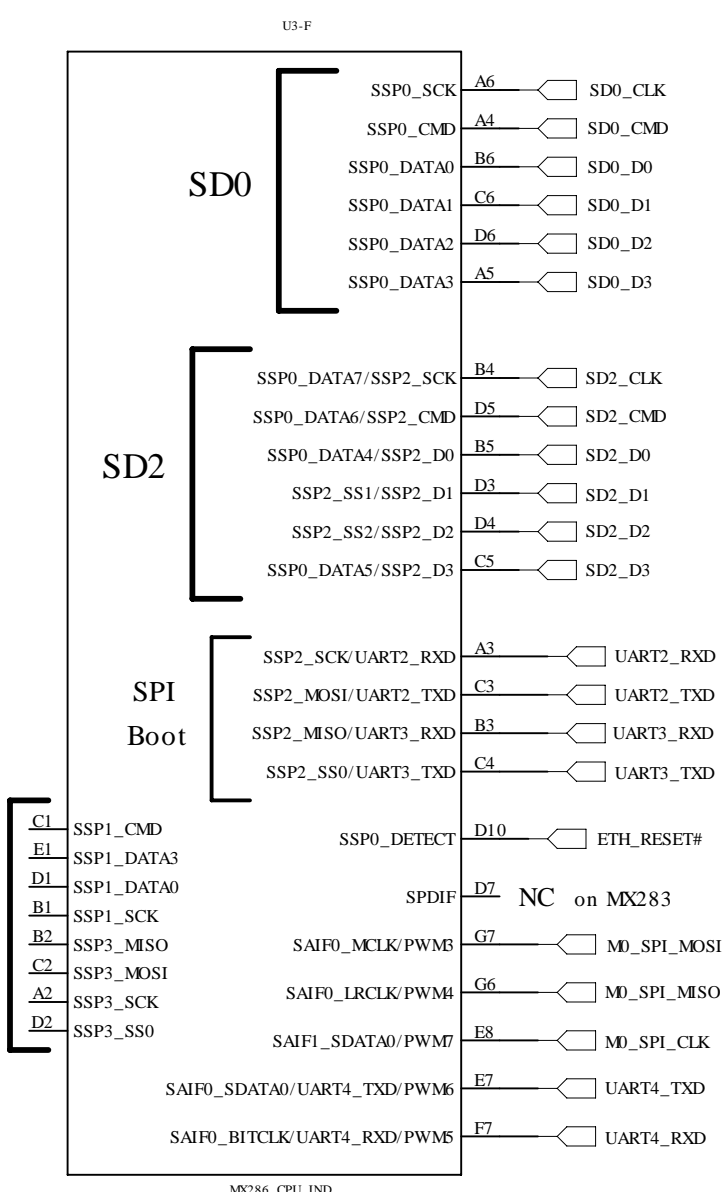


## LCD



## NAND, PWM JTAG, I2C

## Audio SD Card SPI Boot



### SPI

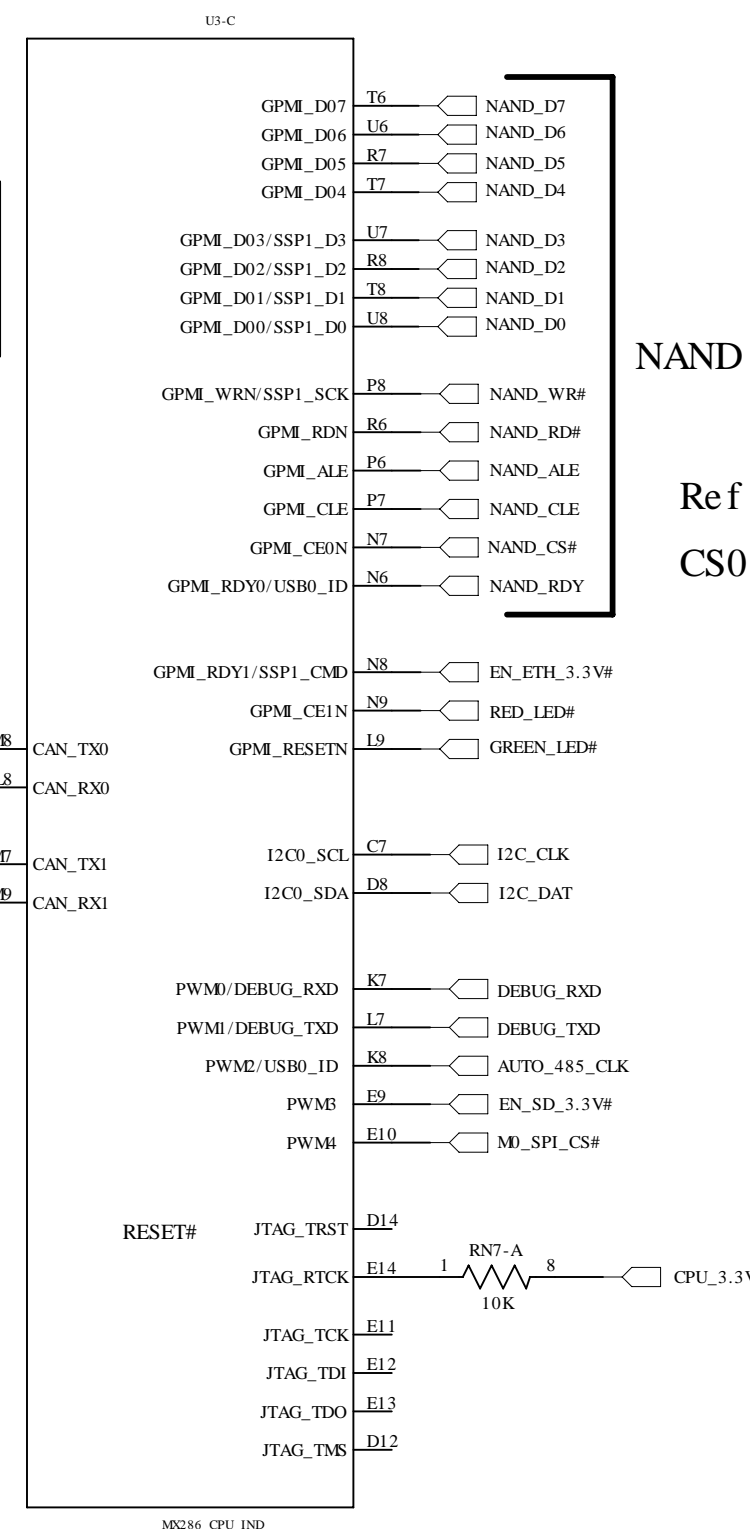
SCK = CLK  
CMD = MOSI  
D0 = MISO  
D3 = CS#

MX286 adds  
4 CAN signals  
and ball D7

12 MHz default boot clock

U3.D3 and U3.D4 are extra  
2 data lines for SPI x4 read  
Page 1313 of Data sheet

Page 1311 - Winbond SPI x2 and x4 supported  
EVK schematic references a 8Mbit Winbond chip



NAND Interface

Ref Design uses  
CS0 and RDY0

LCD\_00 thru LCD\_04  
Control Boot Source

LCD\_05 and 06 bias low  
LCD\_RS biased high  
LCD\_RS low = use OTP  
See: EVK schematic, Page 15

F3 is EVK ETH\_RESET#  
F5, F6 are EVK USB\_PWR\_EN  
E1 is EVK Eth\_PWR\_EN  
C7 and D8 = EVK I2C  
J5 is EVK USB\_0\_ID  
K8 is EVK LCD PWM  
K7 and L7 are EVK console

E10 is EVK SD1\_PWR\_EN

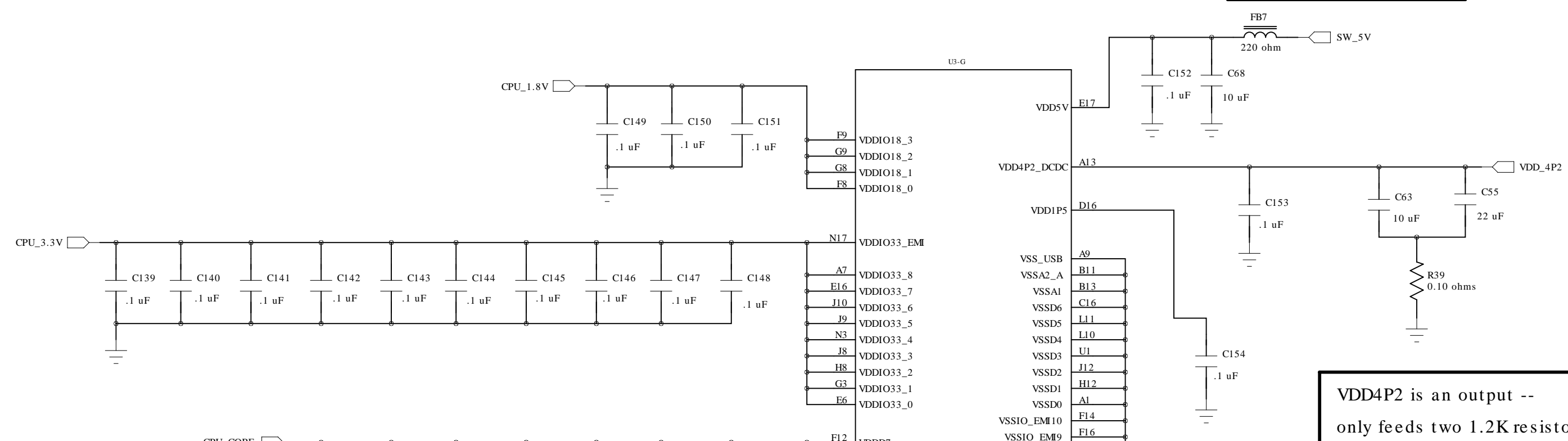
E9 is SD0 PWR\_EN on both  
EVK and Green schematics

PWM outputs can be 24 MHz  
divided by 16-bit integer  
Allows clock 12MHz and lower

All JTAG have 47K internal PU except RTCK

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FB7 not populated ?  
See U7

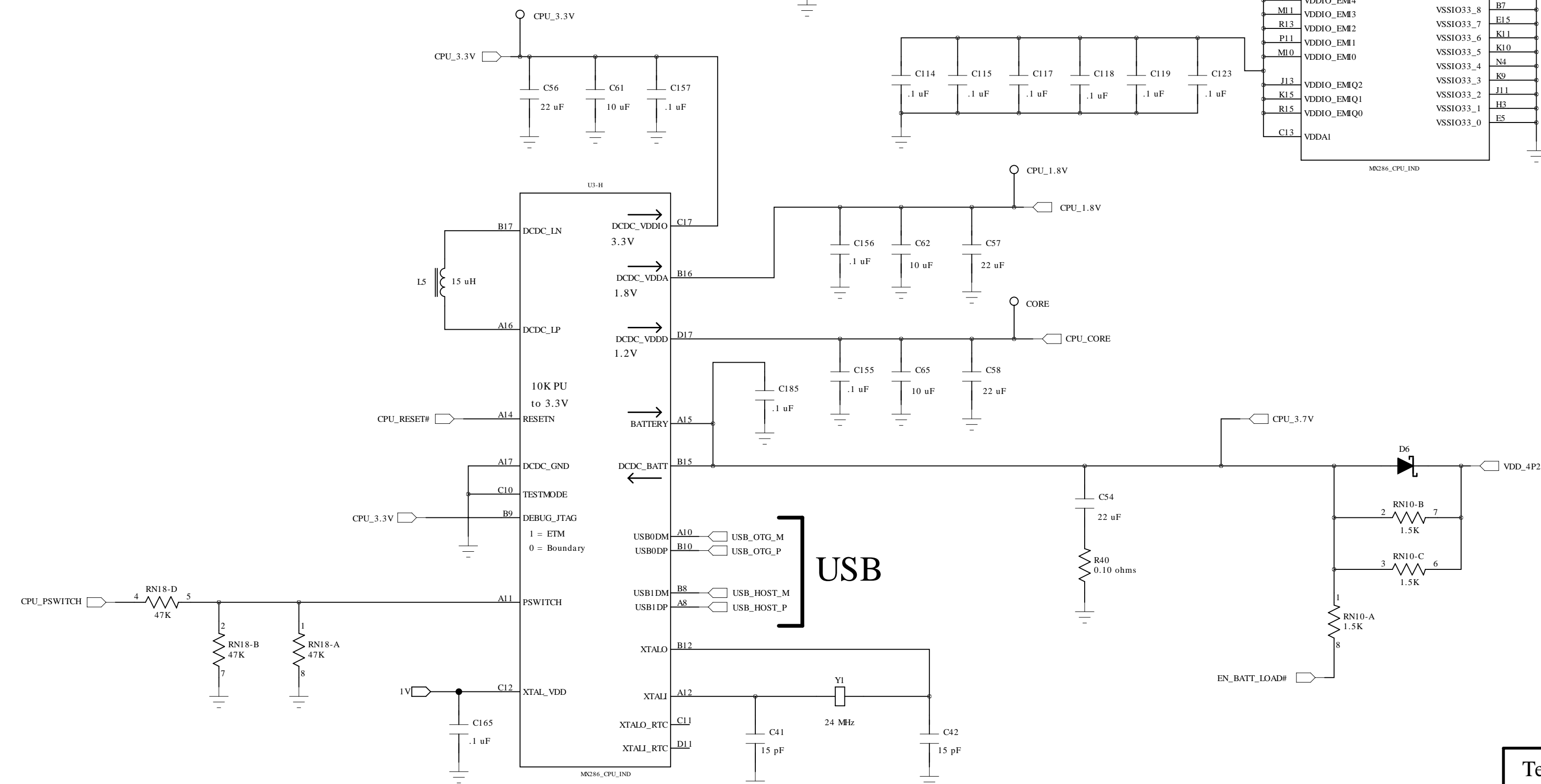


VDD4P2 is an output --  
only feeds two 1.2K resistors

Reg VDD1P5 goes to nothing

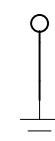
Battery pin supplies current to charge battery

DCDC\_BAT pin is power input for DCDC converters -- connect direct to battery



EVK has FET in parallel with  
D5 "to improve efficiency"

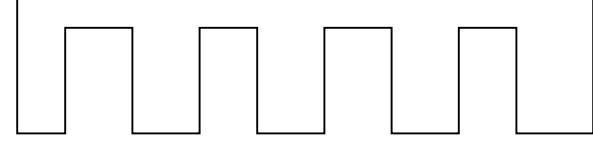
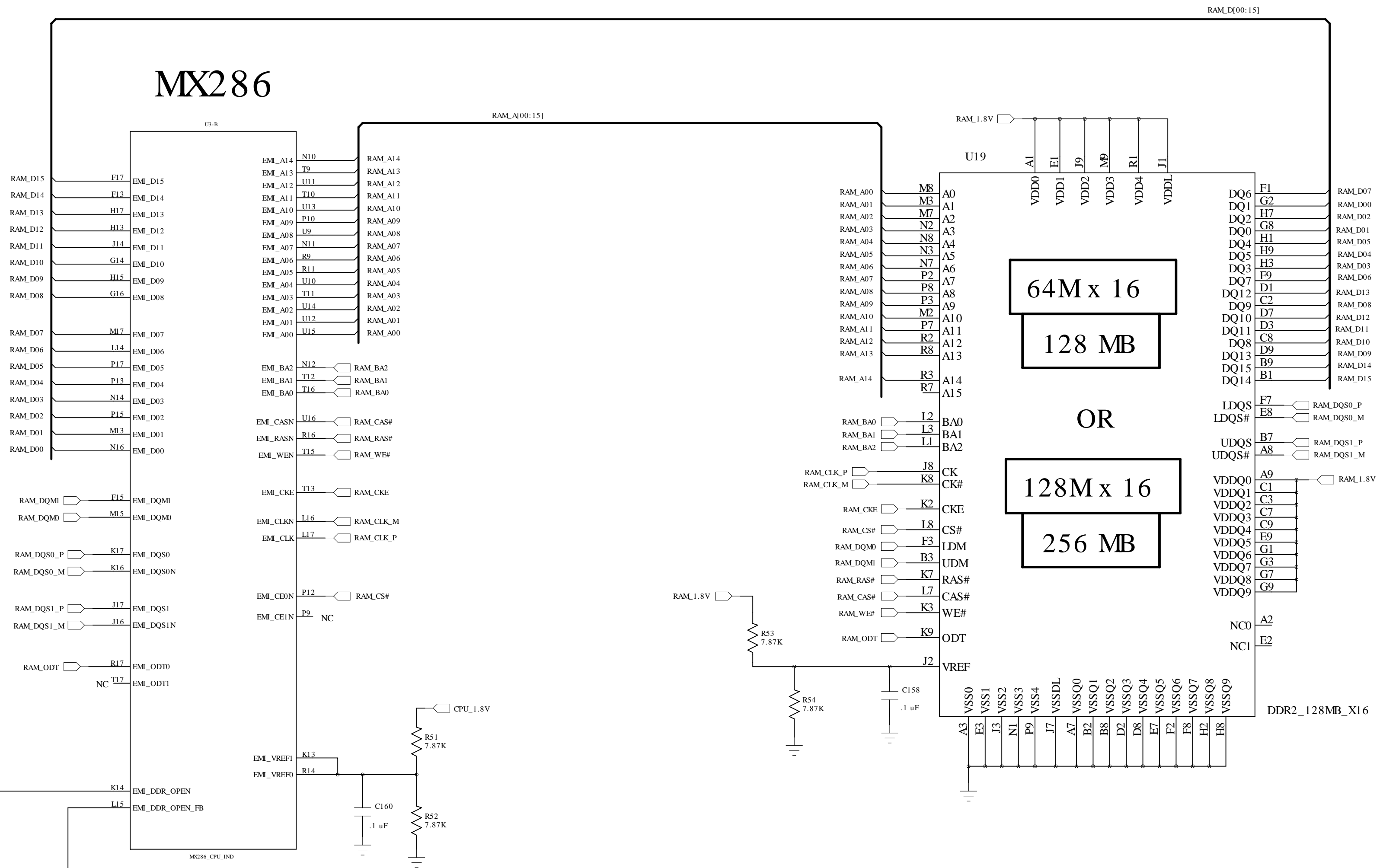
GND Test Point



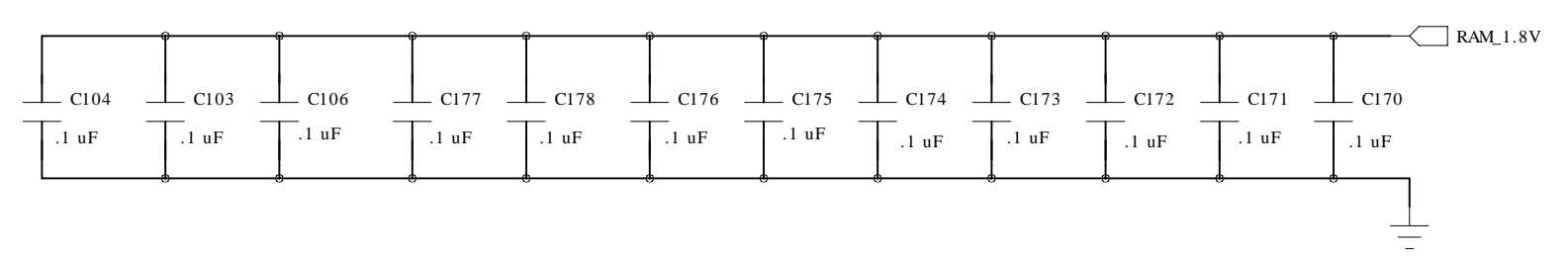
PSWITCH can be driven to 3.3V if a series 10K res is used

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# DDR2 SDRAM (128 or 256 MByte)

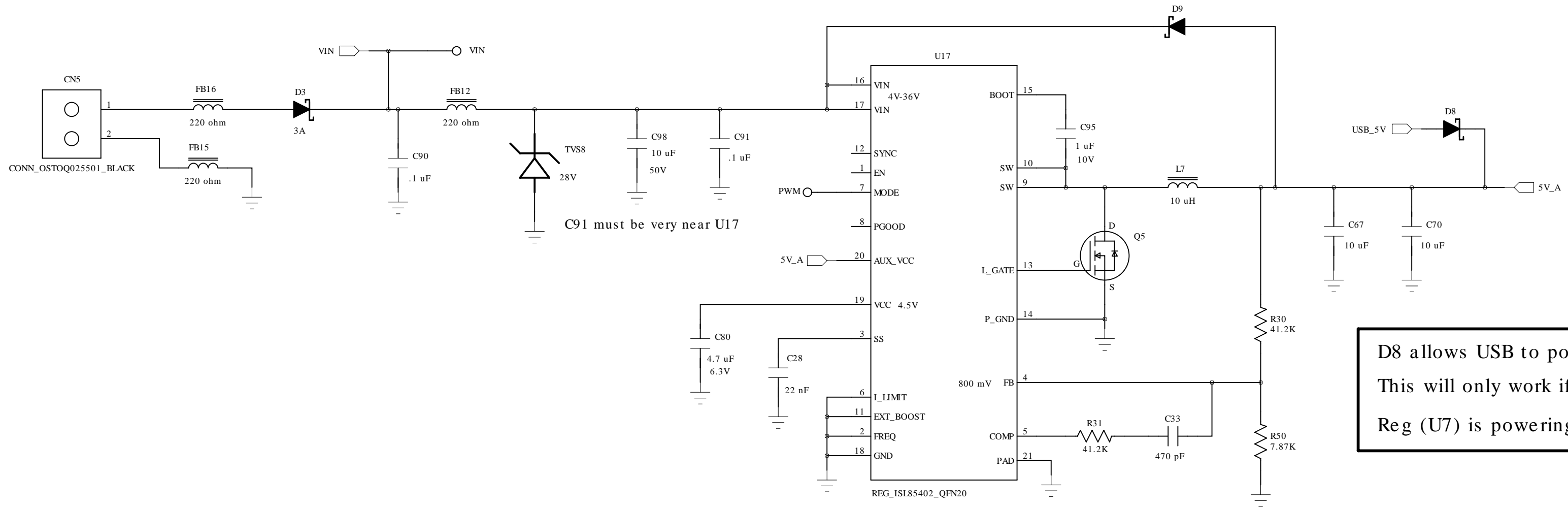


Length of this trace is equal to [CLK + Data] lengths  
Data = Average length of all data traces



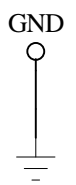
# 5V Power Supply (2000 mA)

8-28 VDC  
Power Input

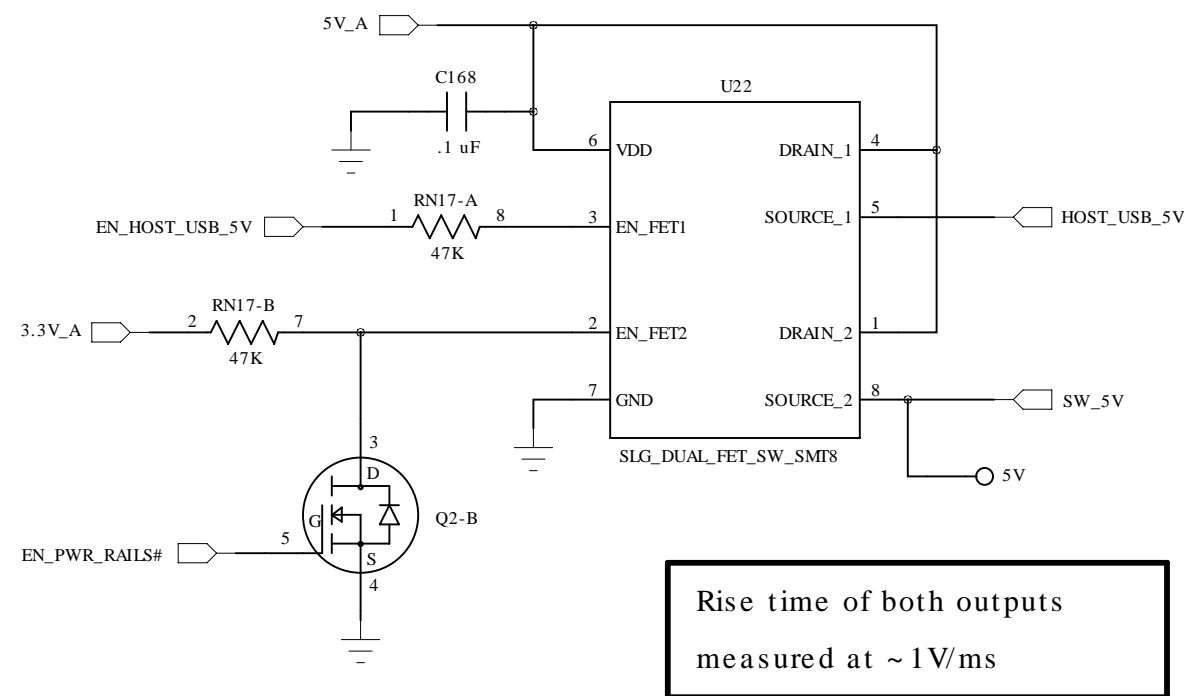


D8 allows USB to power MX286  
This will only work if 3.7V  
Reg (U7) is powering MX286

.063 hole

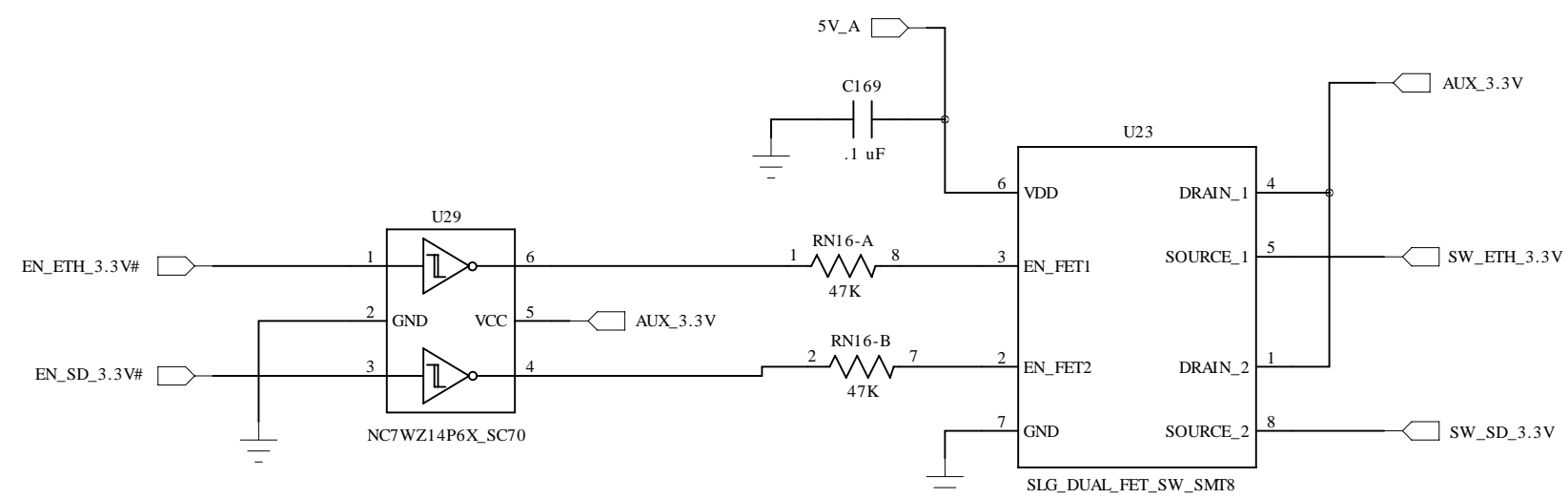


USB and MX286  
Switched Power



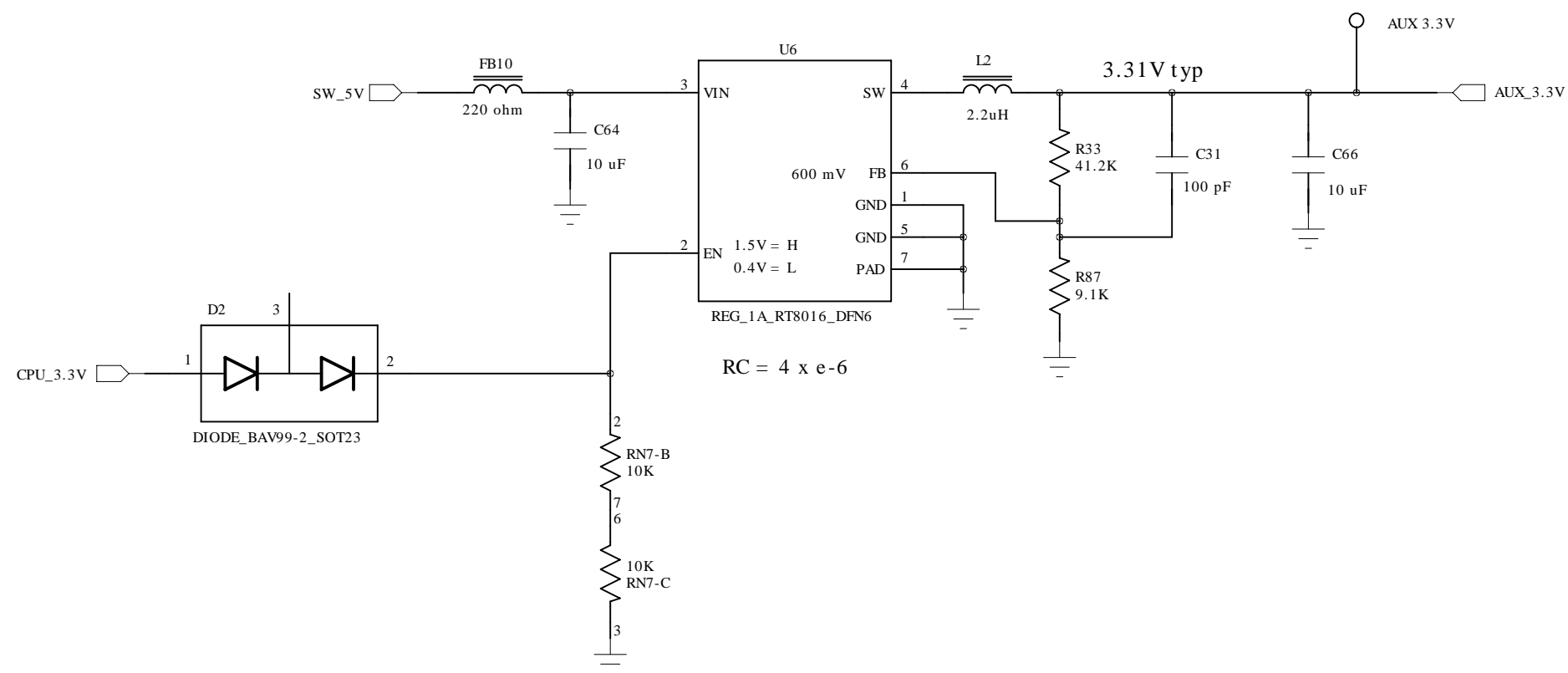
Rise time of both outputs  
measured at ~1V/ms

Ethernet and SD  
Switched Power



Rise time of both outputs  
measured at ~1V/ms

## Aux. 3.3V Reg

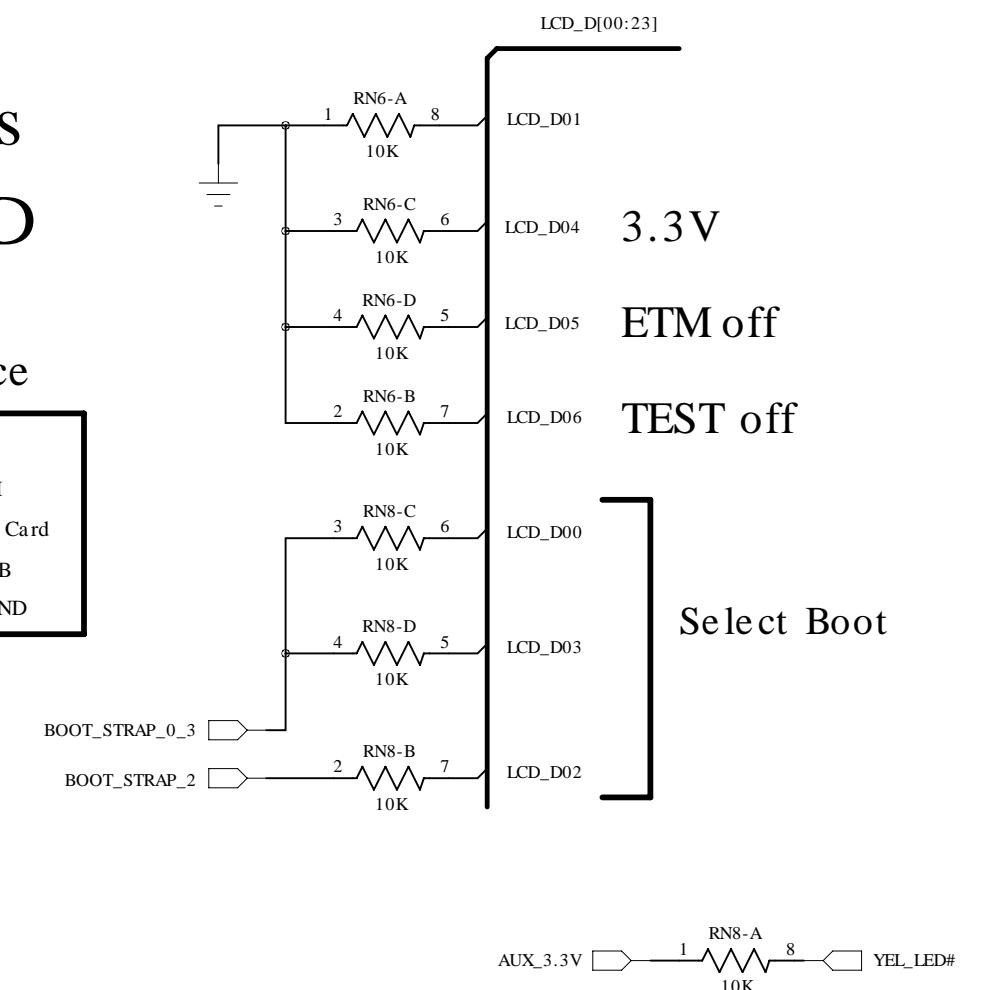


## Boot Strap Bias Res.

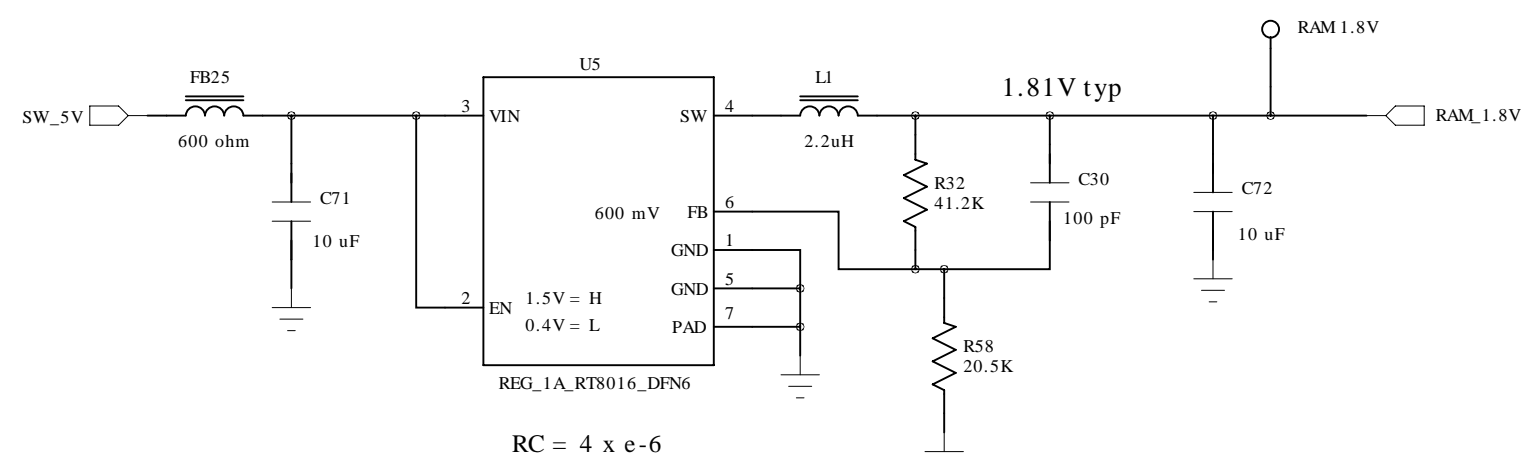
Defaults to NAND

Boot Source

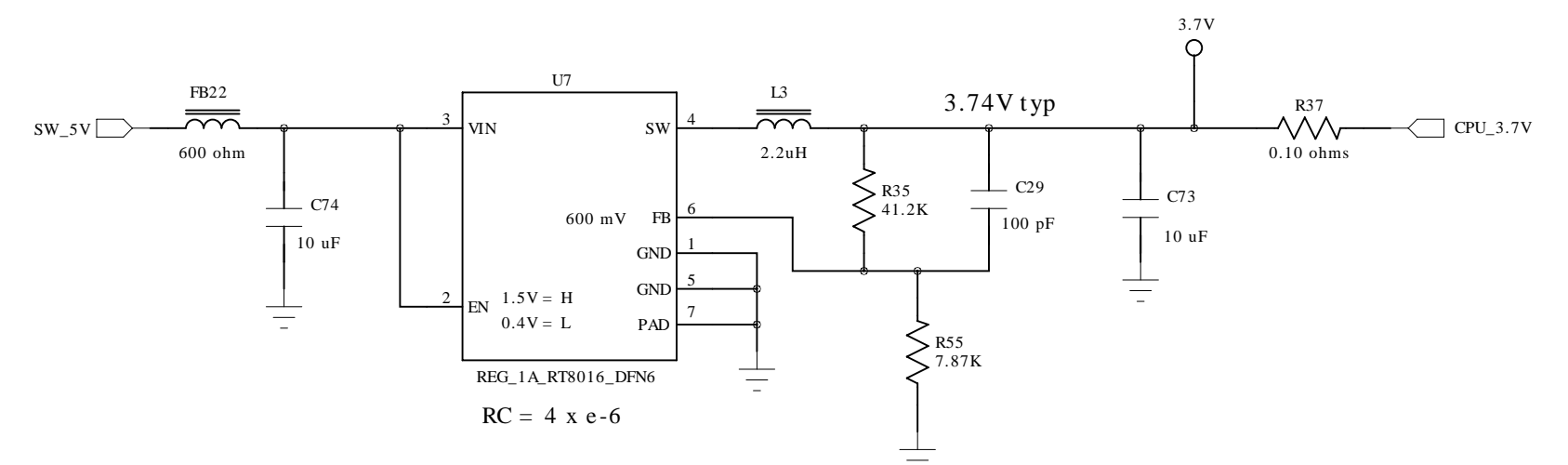
LCD_3	LCD_0	
0 0 1 0		SPI
1 0 0 1		SD Card
0 0 0 0		USB
0 1 0 0		NAND



## RAM 1.8V Reg



## CPU BATT 3.7V



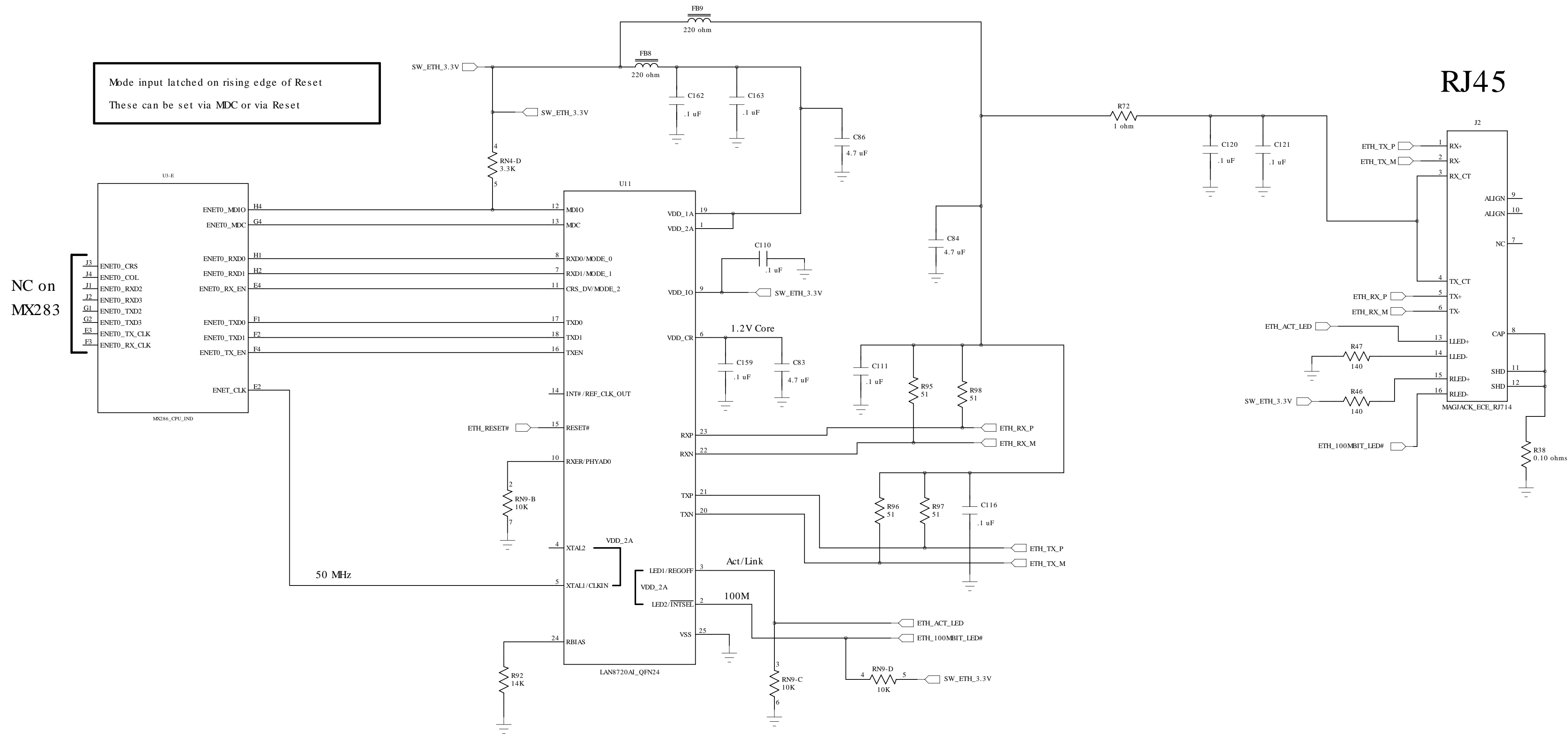
This Reg only required for extra low power mode

FB7 not installed when this reg. is used

Requires a positive pulse on PSWITCH

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# 10/100 Ethernet



Mode input latched on rising edge of Reset  
These can be set via MDC or via Reset

NC on MX283

PHY address and modes latched on rising edge of Reset#

LED high voltage is VDD\_2A = 3.3V

LED active state is always the opposite as the strap state

MDIO bus can not be used until 100 uS after Reset# is deasserted  
MDCLK max is 2.5 MHz

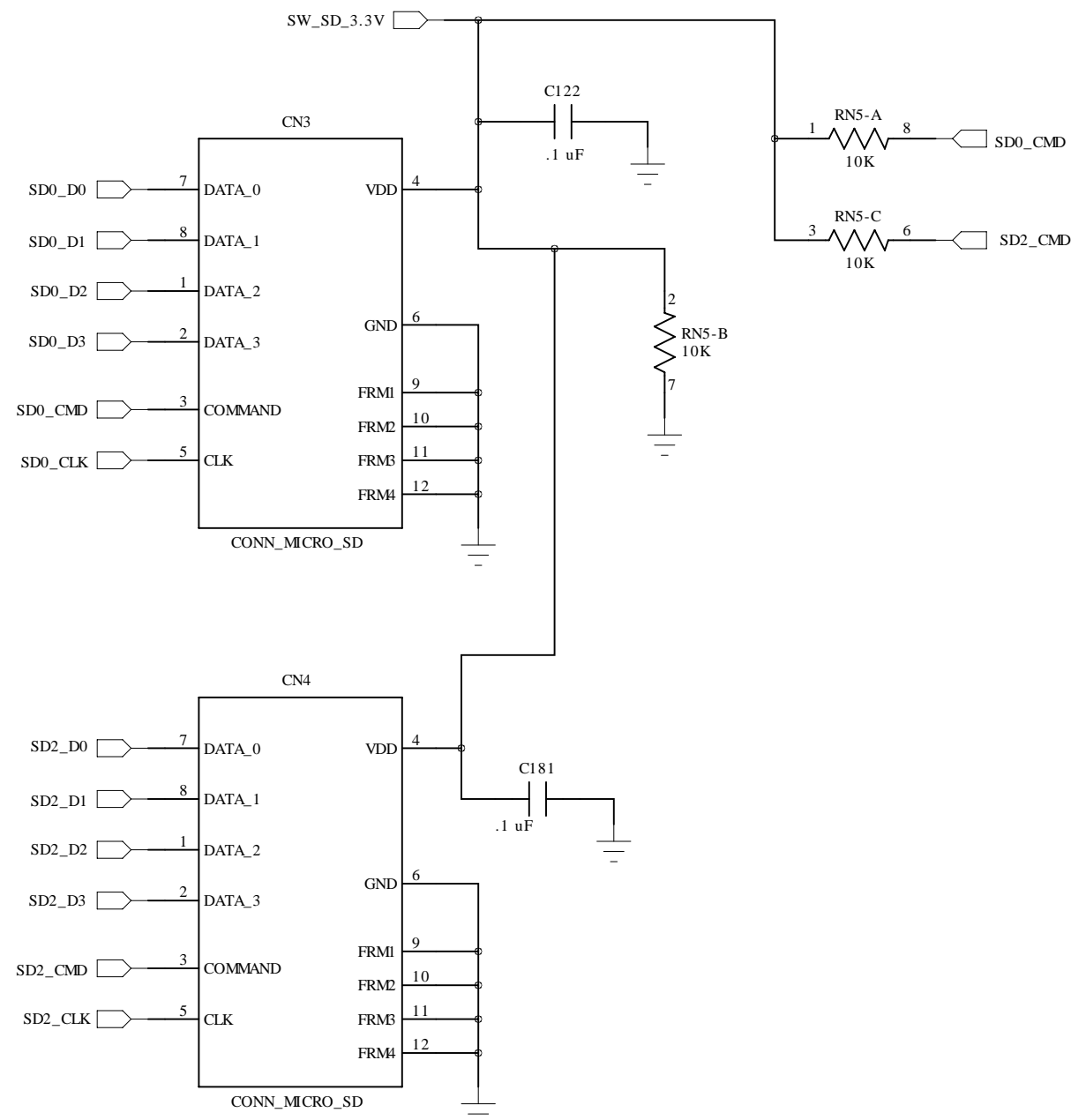
Auto MDIX is supported and  
Polarity Correction supported

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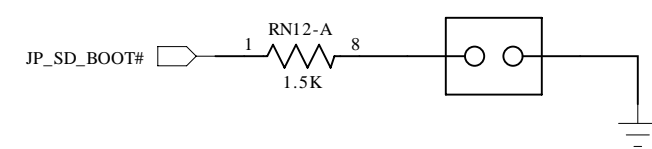


# Flash Memory

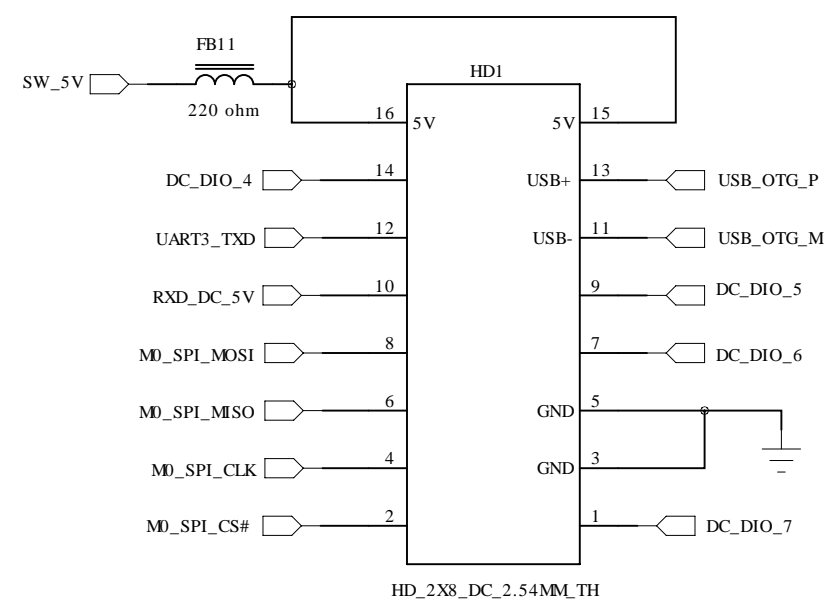
## Micro SD Card Socket



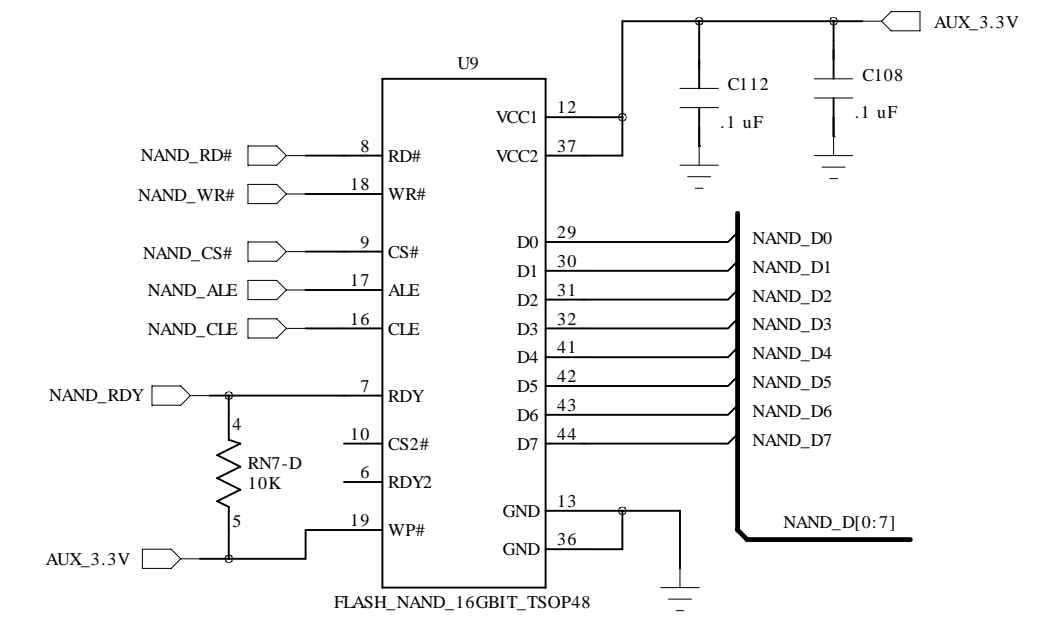
## SD Boot Jumper



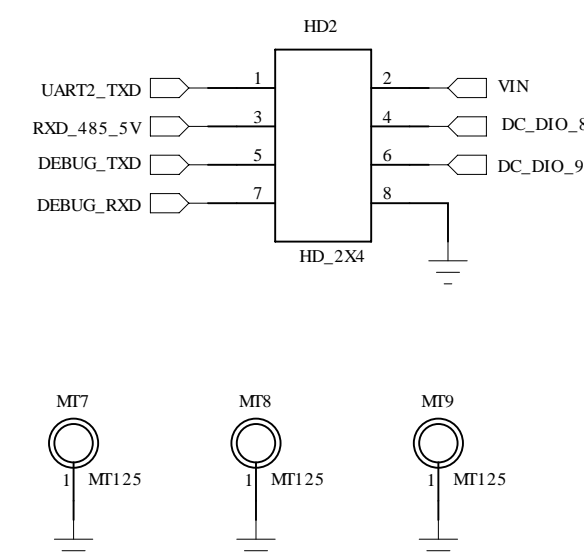
## Daughter Card Interface



## NAND Flash

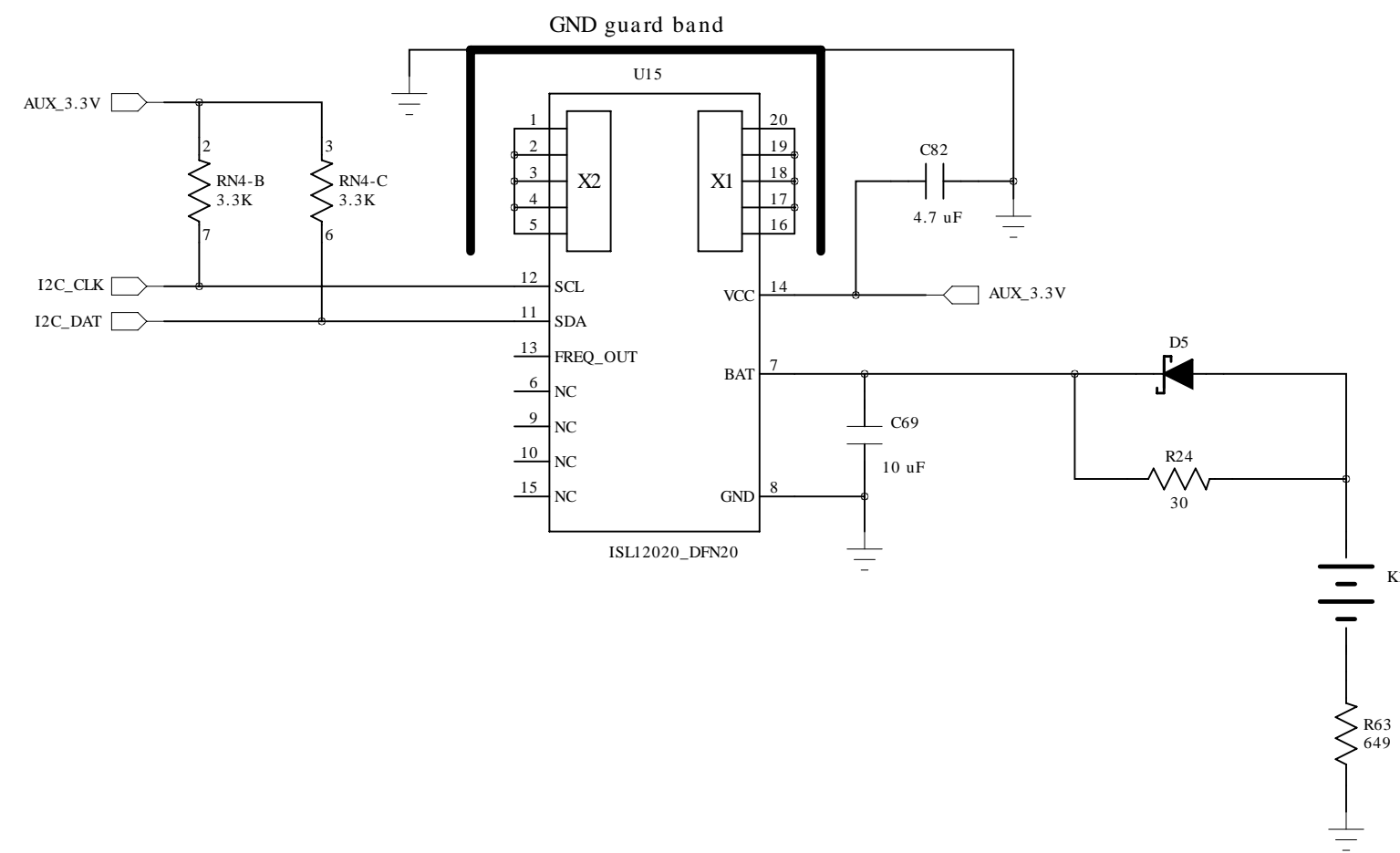


## Supplemental Interface

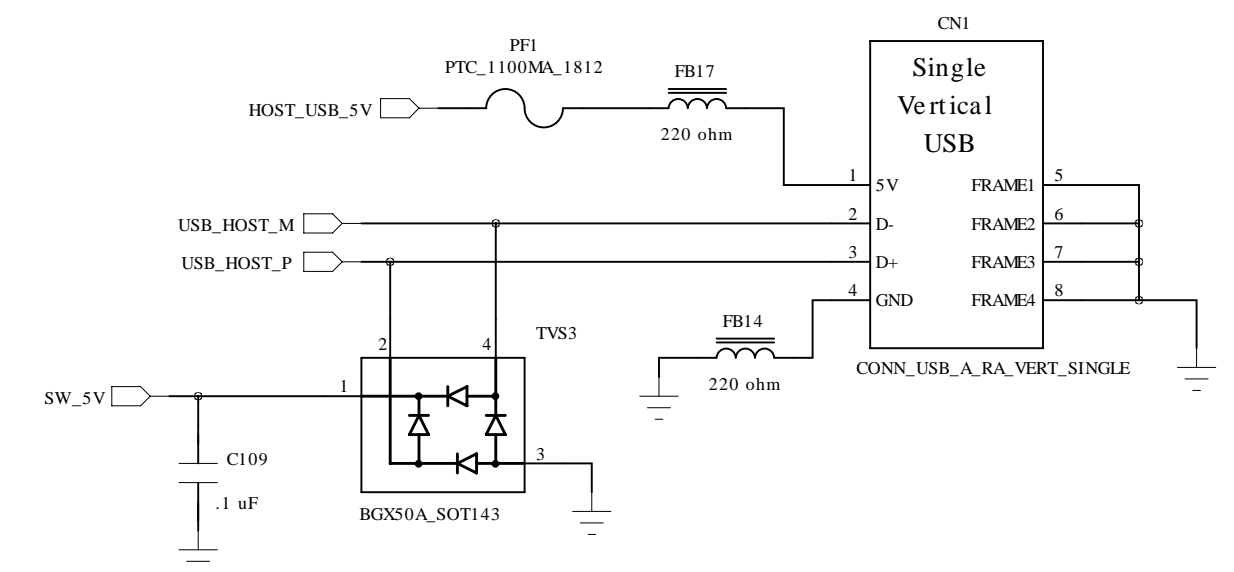


# RTC and Host USB

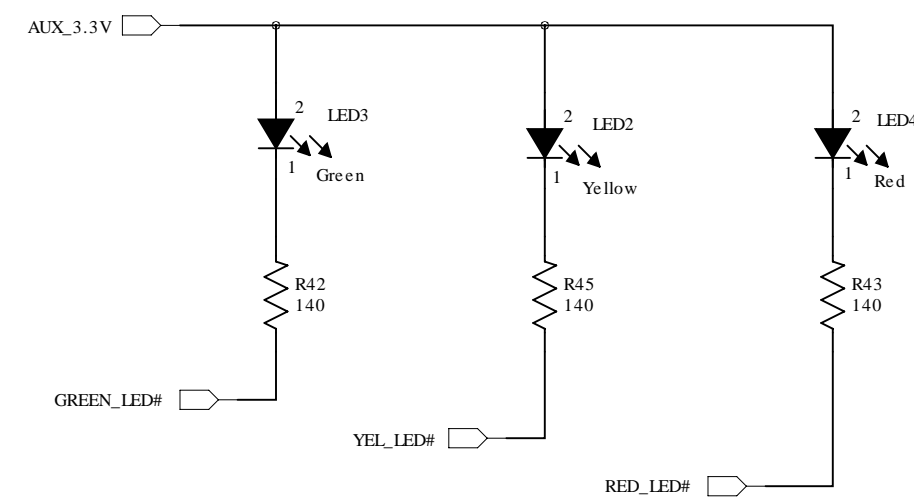
## RTC and Temp. Sensor



## External Host USB Port



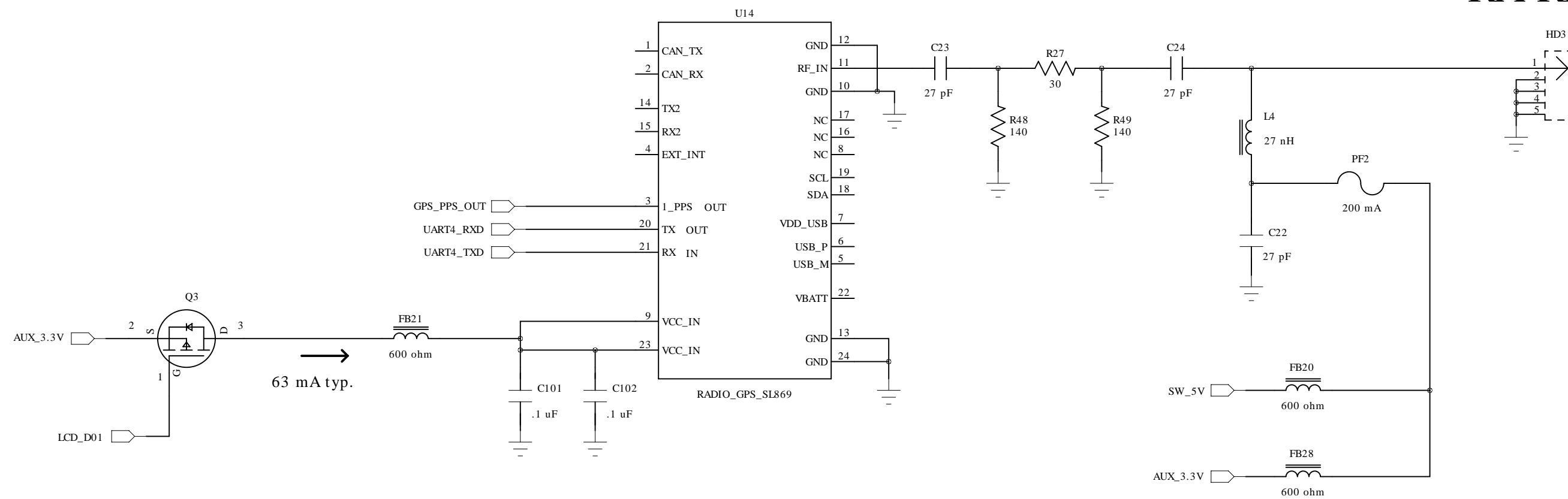
## SMT RA LEDs



# GPS Radio and Auto RS-485

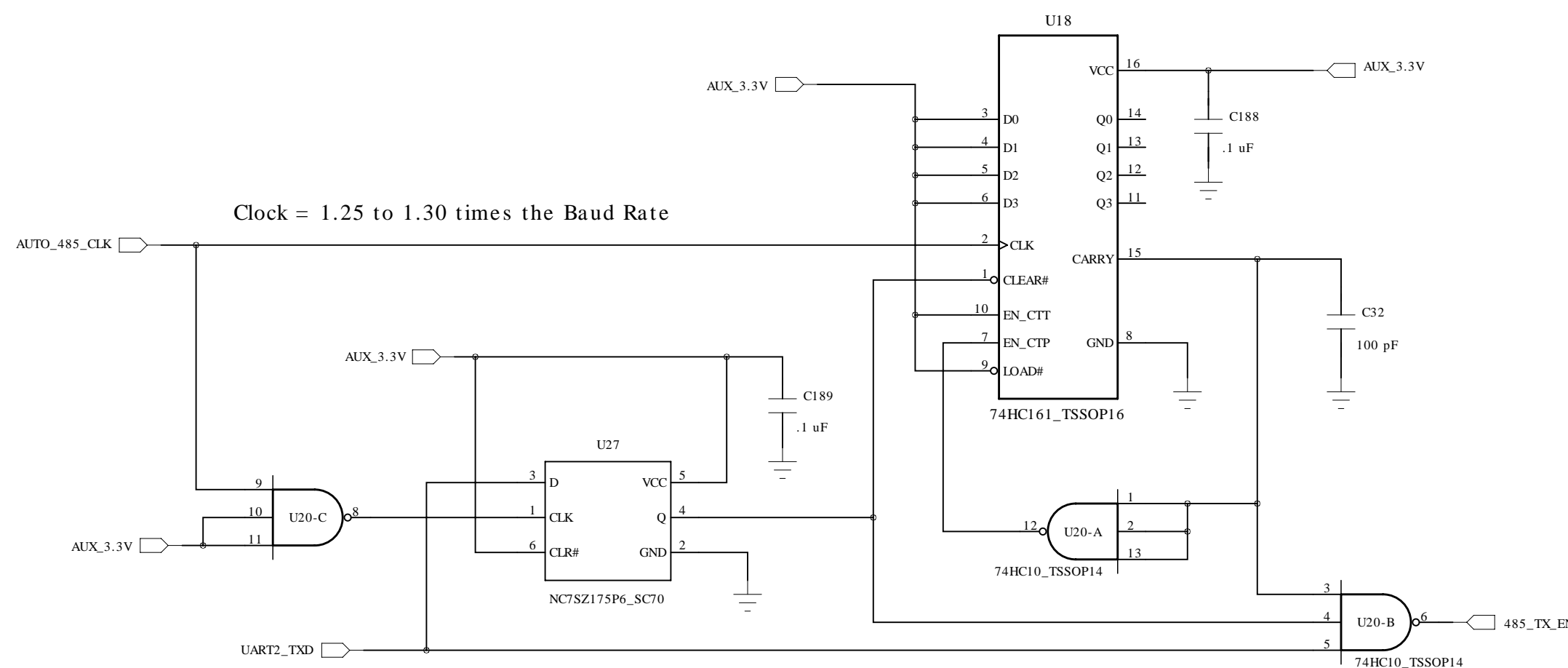
## Telit SL869 GPS Radio

RF Conn.  
RA RMA



Warning: DNP FB28 !

## Modbus Auto 485 TX Enable



## Auto RS-485 Enable

Counter asserts TX\_EN for 14.5 clocks after Clear removed  
 Assuming the clock is 1.28 times the Baud rate, this is 11.3 data bits  
 Worst case (bit 7 = 0 of last data byte in packet),  
 TX\_EN asserted about 11 bit times past end of packet  
 Quickest Turn off of TX\_EN occurs when last packet byte is FF  
 Then TX\_EN turns off about 2 bit times after end of packet

Max Baud Rate supported is 1042 Kbaud

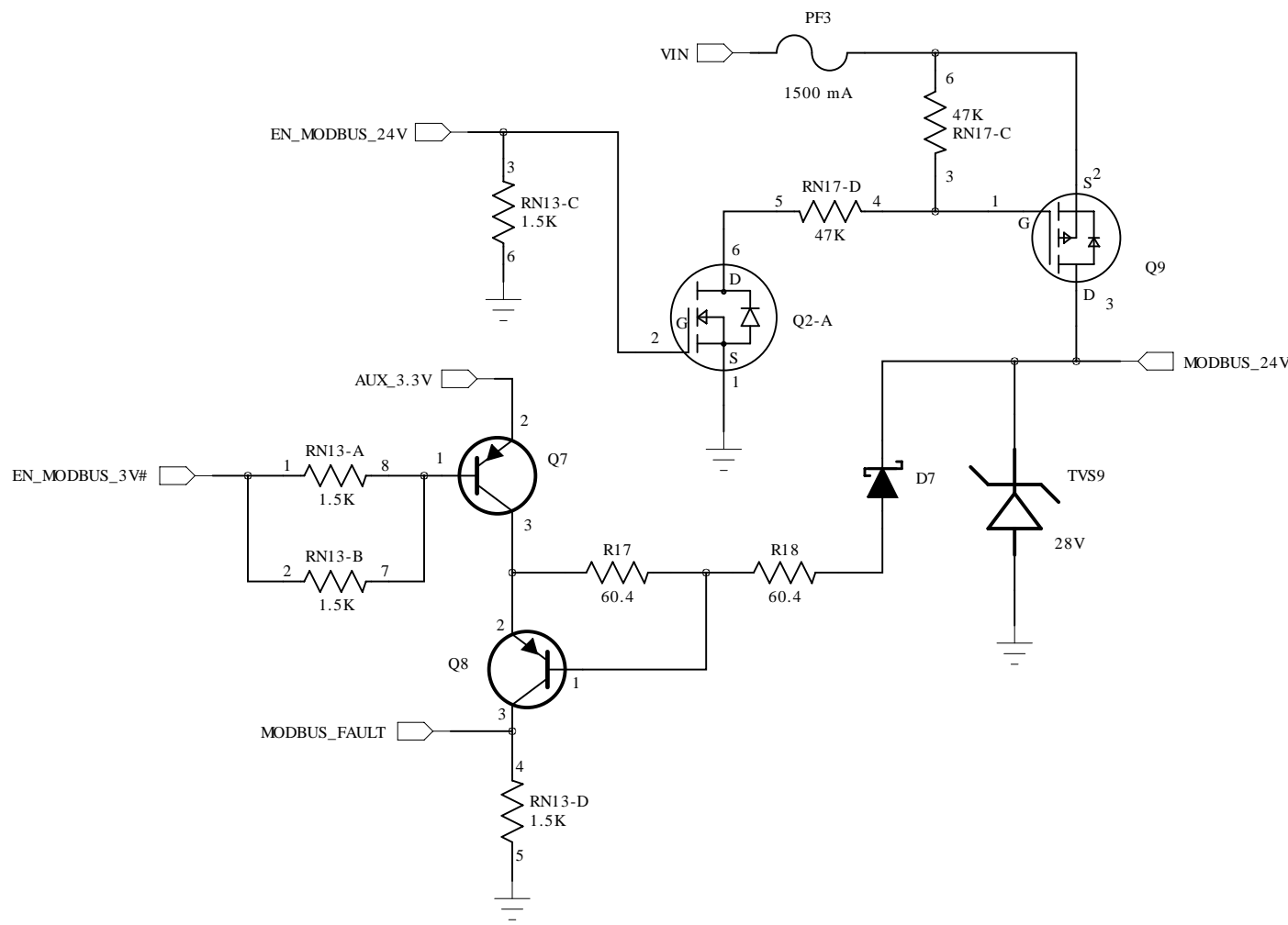
Clock for this baud rate is 1.33 MHz

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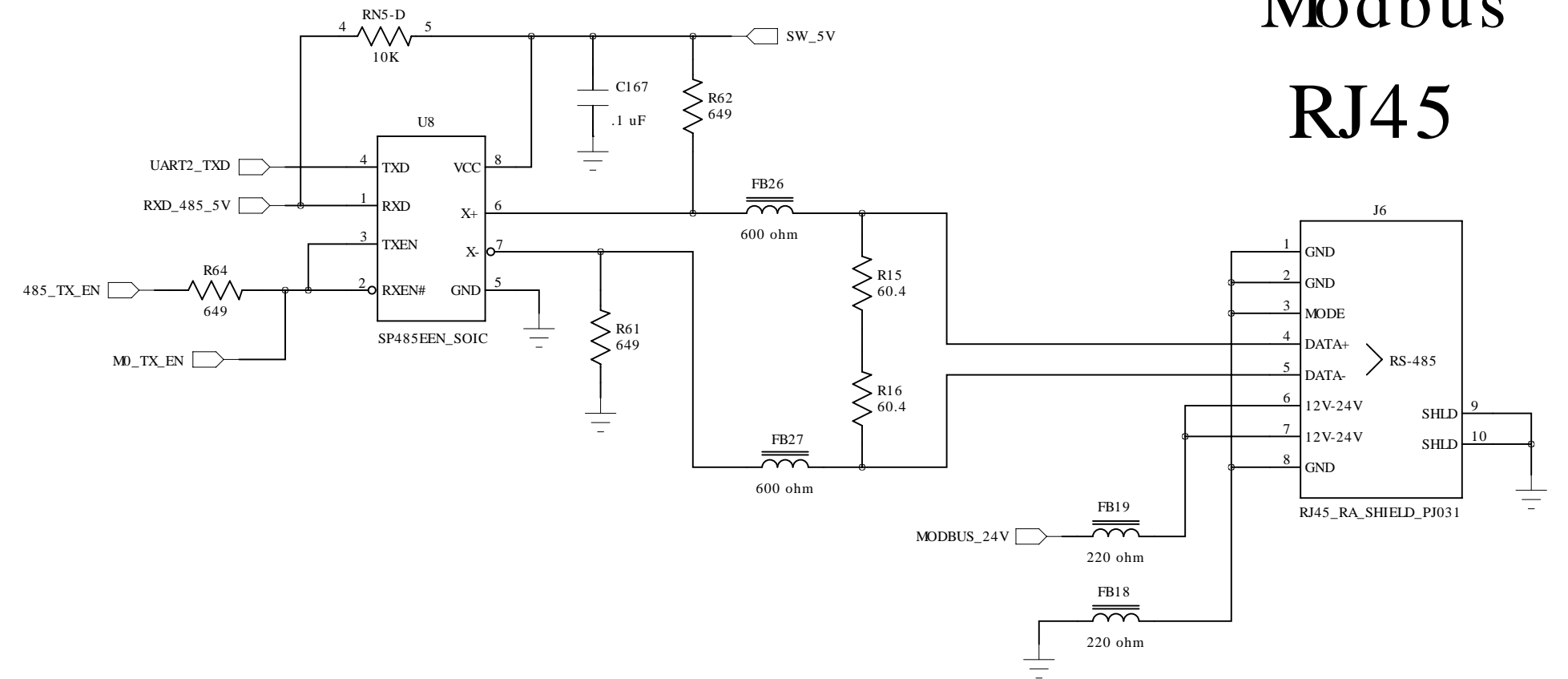


# Mod Bus RS-485 and CAN Port

## Modbus Power Switch

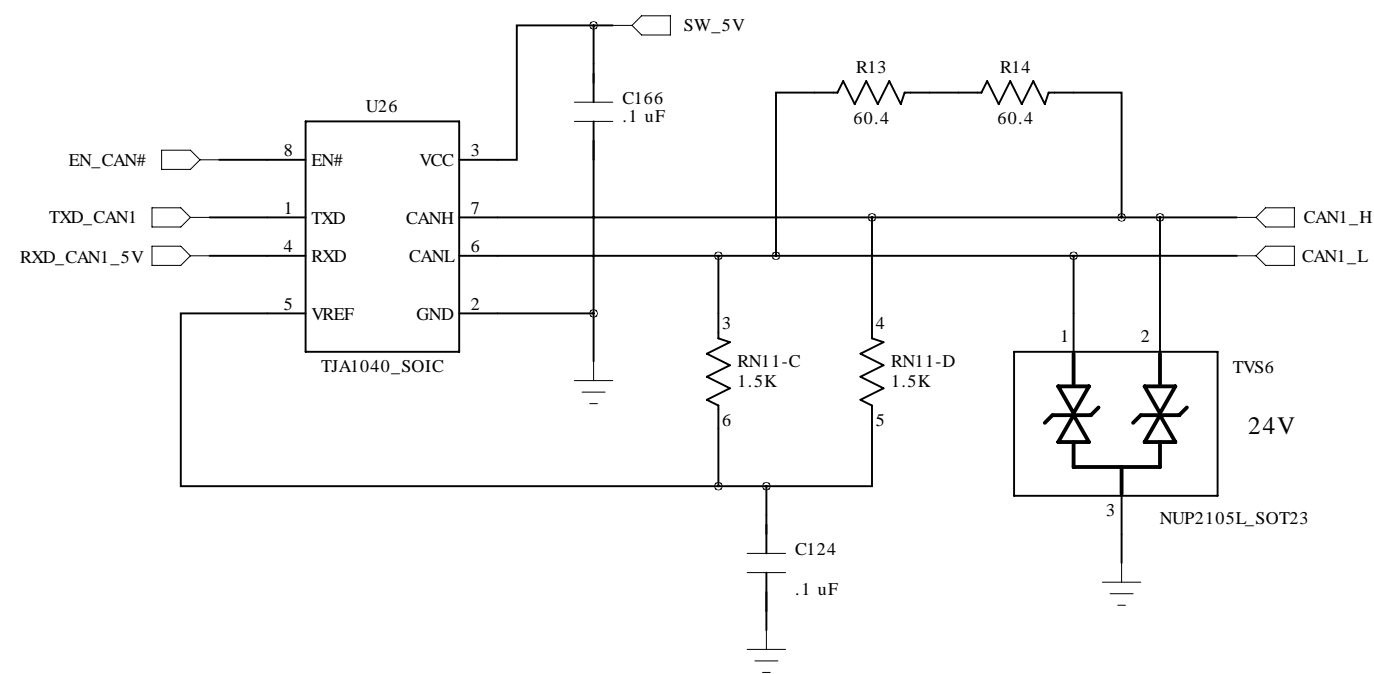


## RS-485 Driver

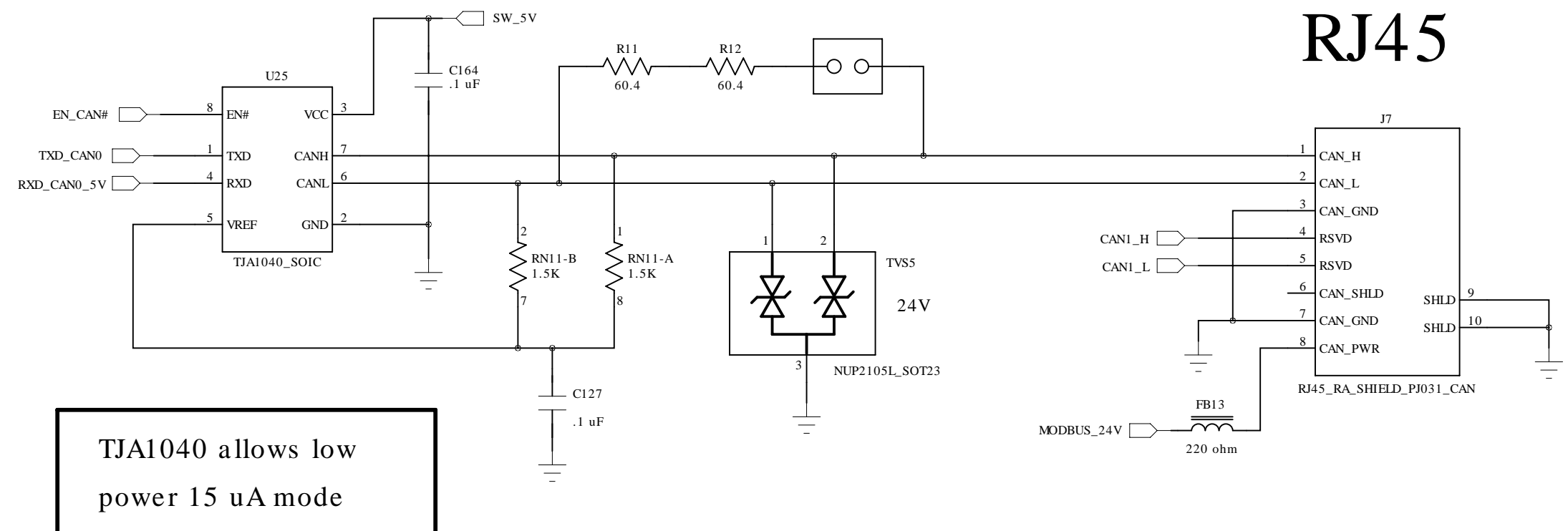


## Modbus RJ45

## CAN\_1 Tranceiver



## CAN\_0 Tranceiver



## CAN RJ45

TJA1040 allows low power 15 uA mode

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