Comments:

Board can be powered from USB
or by 8-28VDC, or by 24VAC

Cortex M0 is powered up first, then it controls MX286 start up

Cortex M0 does these functions:

- Controls MX286 power up sequence
- Controls MX286 Boot Strapping
- USB Device to Console conversion
- Controls Blue LED
- Can read Push Switch
- Measures Analog Vin value
- Reads SD_BOOT Jumper
- Board ID

Rev.P1 Problems:

Serial Port Usage

UART0 = RS-232
UART1 = RS-232
UART2 = Modbus
UART3 = STC RS-485
UART4 = Blue or DC
Debug = Console/DC

DC = Daughter Card
STC = Screw Term. Conn.

Notes:

1) Check Ethernet LEDs
RAM_1.8V rail turns on later than TS-7670
Test 24VAC power

2) For Modbus 1042K baud operation - use DMA ?
Serial Port RX DMA on MX286 says "must be multiples of 4 bytes"
TX DMA does not say restricted to 4 byte multiples

3) BOM Warning:

R33, R34 and HD3 not pop
JP1 thru JP5 is 5x2 header = 15-3070-7
CAN ports are options
128MB and 256MB RAM sizes

CAN Option

U25, U26 and TVS16

UART2 and UART3 changed to SPI
when programming FPGA

Warning: 1.8V Levels

- SD2 signals
- WIFI_IRQ
- FPGA_SPARE_0
- FPGA_SPARE_1
- FPGA_SPARE_2

I/O Diff from TS-7670

UART0_RTS --> E2_I2C_CLK
UART0_CTS --> E2_I2C_DAT
UART1_CTS --> WIFI_IRQ (1.8V)
DC_DIO_9 --> DISABLE_TXEN2#
EN_232_TRANS = No Connect
EN_ETH_3.3V# = No Connect

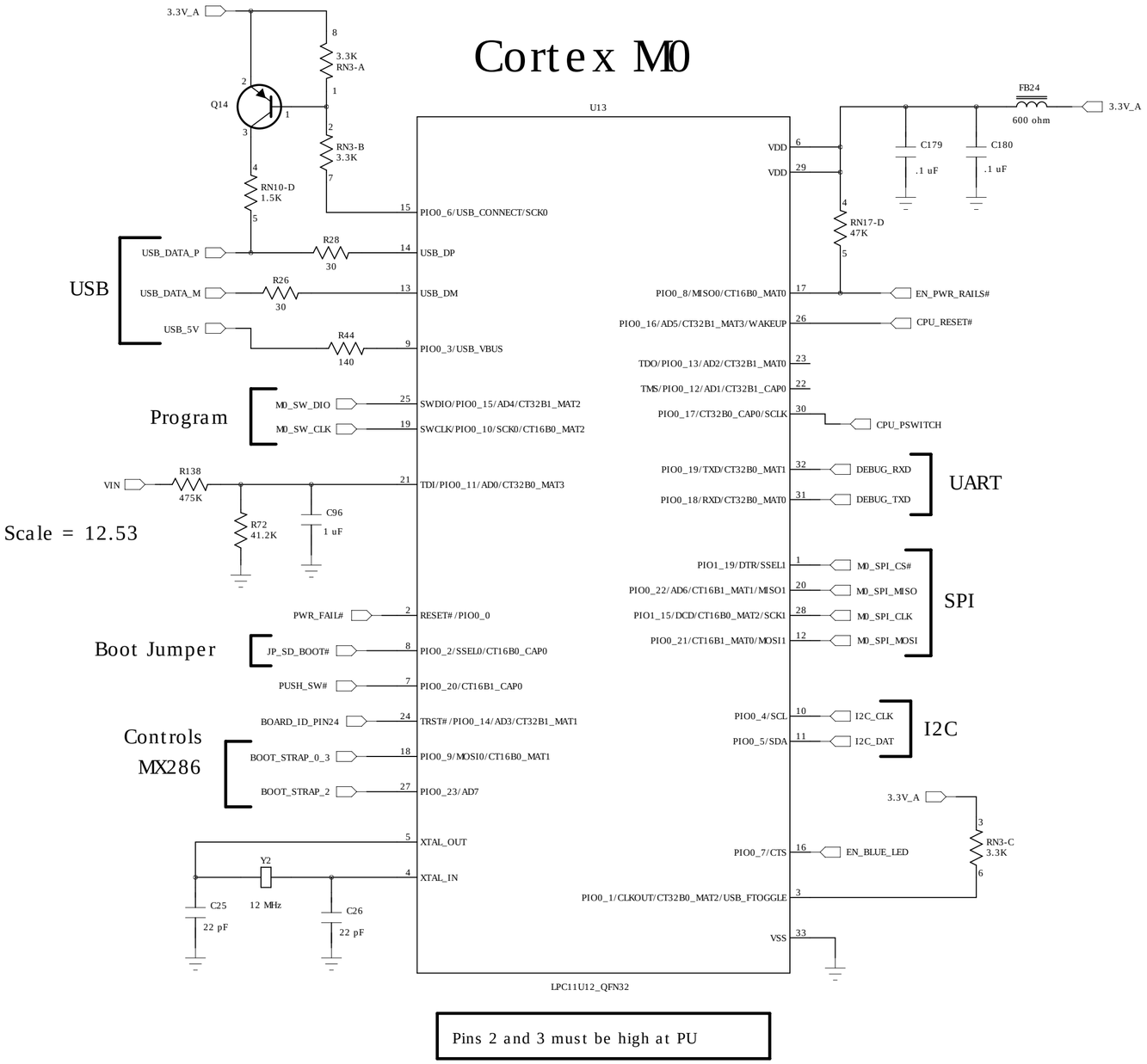
GPS_PPS_OUT --> FPGA_DONE
U3.R3 = FPGA_RESET#
U3.U4 = FPGA_SPI_CS#
U3.T4 = FPGA_IRQ
UART1_RTS = FPGA_SPARE_0 (1.8V)
U3.U5 = FPGA_SPARE_1 (1.8V)
DC_DIO_8 = FPGA_SPARE_2 (1.8V)

Changed VIN A/D scaling !

Technologic Systems	Date April 21, 2014	
Title: TS-7680 Documentation		
Rev: P1	Designer	Sheet 1 of 18

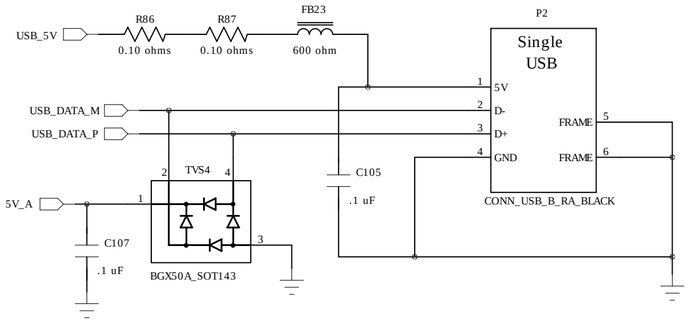
USB Device Port and Cortex M0

Cortex M0

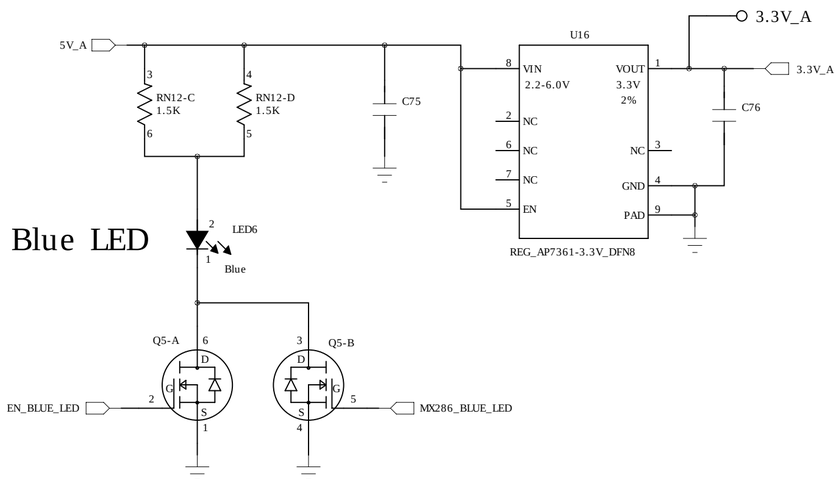


Pins 2 and 3 must be high at PU

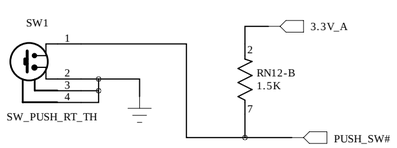
USB Device Port



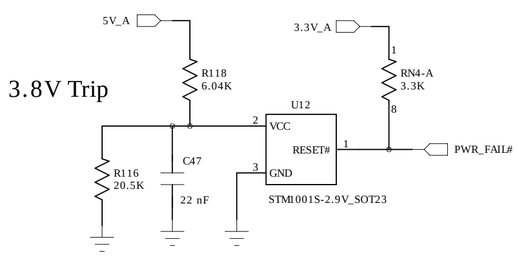
3.3V Reg. for M0



Push Switch



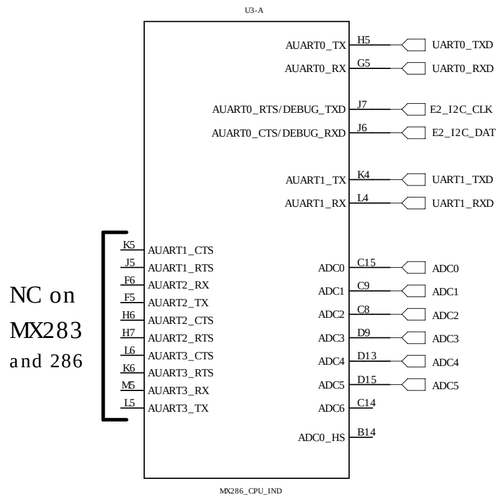
Brown out Detect



Technologic Systems	Date April 21, 2014	
Title: TS-7680 Cortex M0 Controller		
Rev: P1	Designer	Sheet 2 of 18

MX286 ARM9 CPU

UARTs, ADC

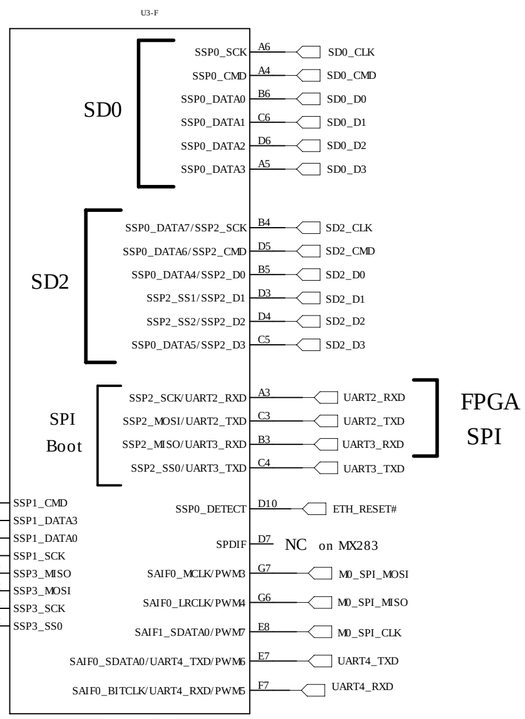


NC on MX283 and 286

Audio

SD Card

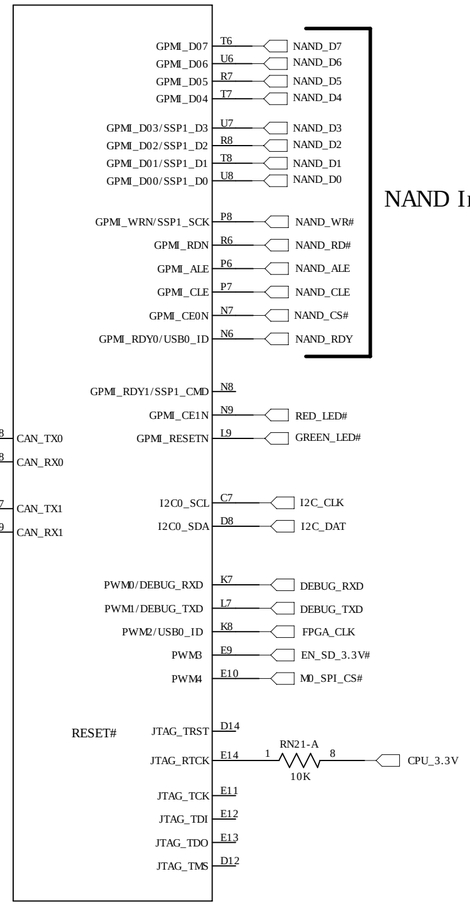
SPI Boot



NC on MX283 and 286

NAND, PWM

JTAG, I2C



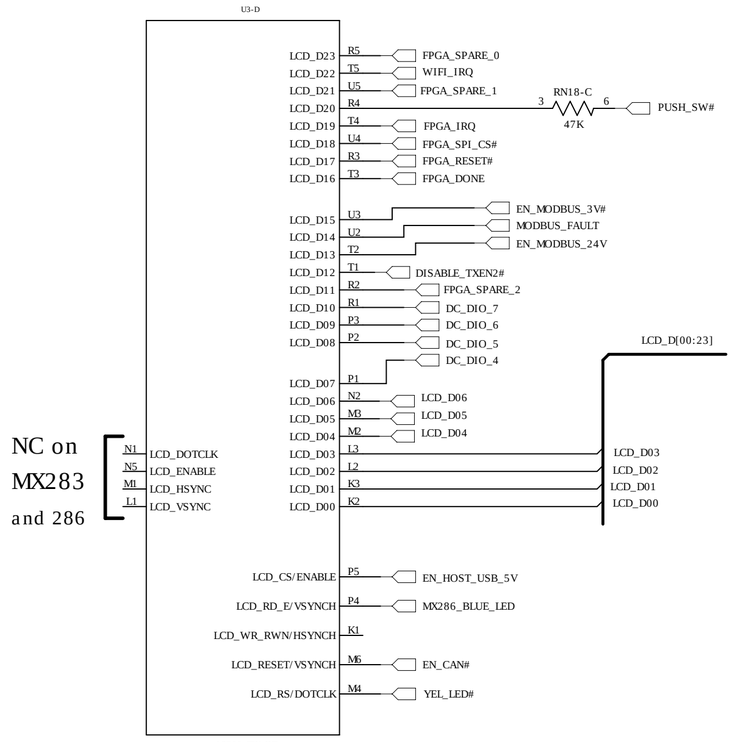
SPI

SCK = CLK
CMD = MOSI
D0 = MISO
D3 = CS#

MX286 adds
4 CAN signals
and ball D7

All JTAG have 47K internal PU except RTCK

LCD



NC on MX283 and 286

LCD_00 thru LCD_04
Control Boot Source

LCD_05 and 06 bias low
LCD_RS biased high
LCD_RS low = use OTP
See: EVK schematic, Page 15

F3 is EVK ETH_RESET#
F5, F6 are EVK USB_PWR_EN
E1 is EVK Eth_PWR_EN
C7 and D8 = EVK I2C
J5 is EVK USB_0_ID
K8 is EVK LCD PWM
K7 and L7 are EVK console

E10 is EVK SD1_PWR_EN

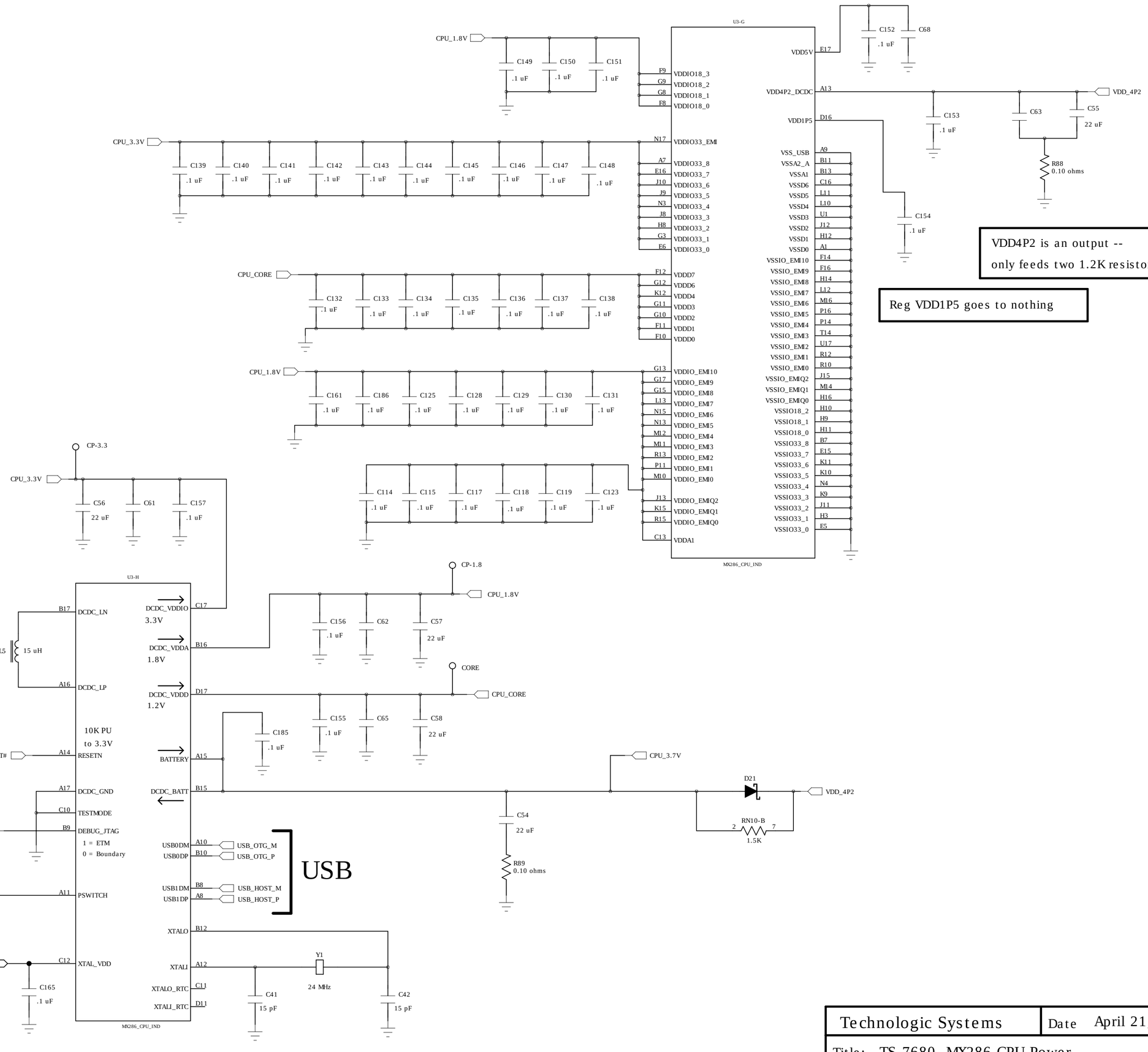
E9 is SD0 PWR_EN on both EVK and Green schematics

PWM outputs can be 24 MHz
divided by 16-bit integer
Allows clock 12MHz and lower

Technologic Systems	Date April 21, 2014	
Title: TS-7680 MX286 CPU		
Rev: P1	Designer	Sheet 3 of 18

Battery pin supplies current to charge battey

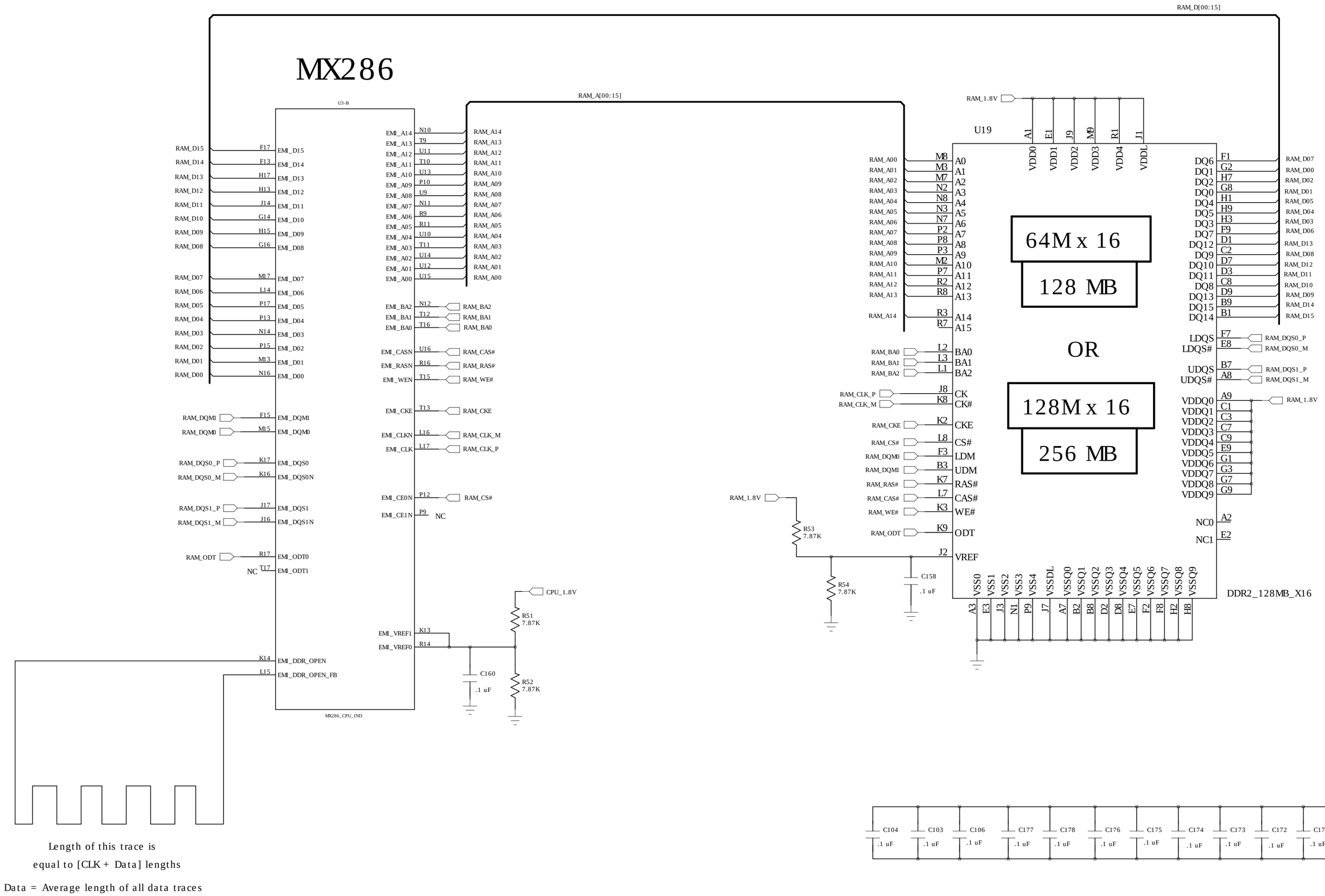
DCDC_BAT pin is power input for DCDC converters -- connect direct to battery



PSWITCH can be driven to 3.3V if a series 10K res is used

Technologic Systems	Date April 21, 2014	
Title: TS-7680 MX286 CPU Power		
Rev: P1	Designer	Sheet 4 of 18

DDR2 SDRAM (128 or 256 MByte)

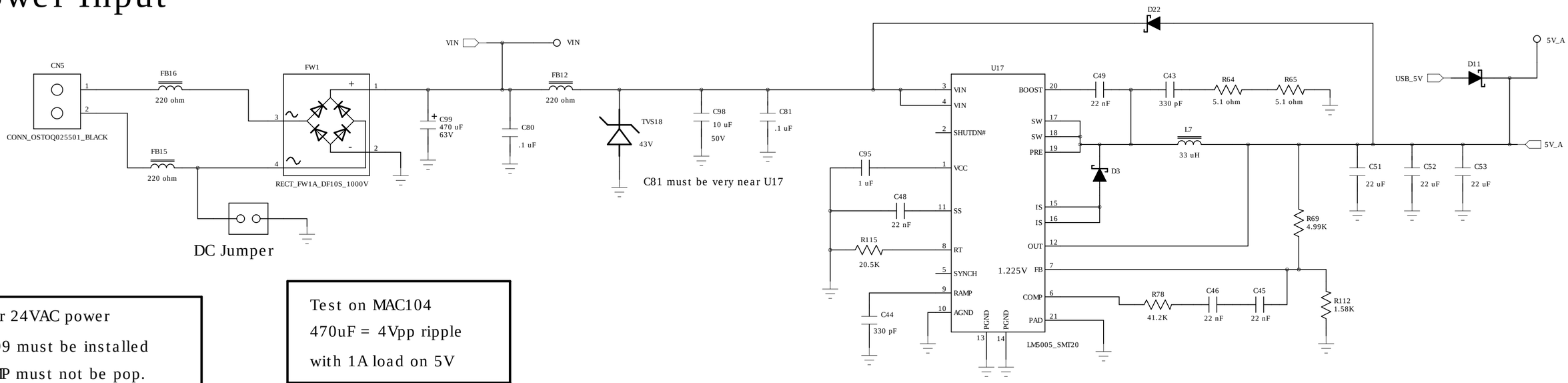


Technologic Systems	Date April 21, 2014	
Title: TS-7680 DDR2 RAM		
Rev: P1	Designer	Sheet 5 of 18

5V Power Supply (2000 mA)

D11 allows USB to power MX286
This will only work if 3.7V
Reg (U7) is powering MX286

8-28 VDC Power Input

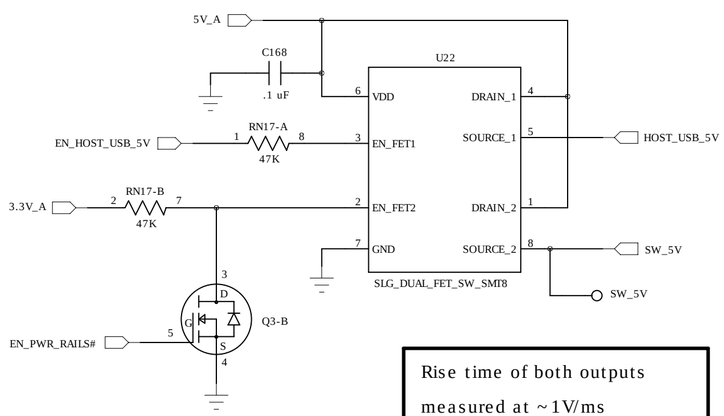


For 24VAC power
C99 must be installed
JMP must not be pop.

Test on MAC104
470uF = 4Vpp ripple
with 1A load on 5V

.063 hole
GND

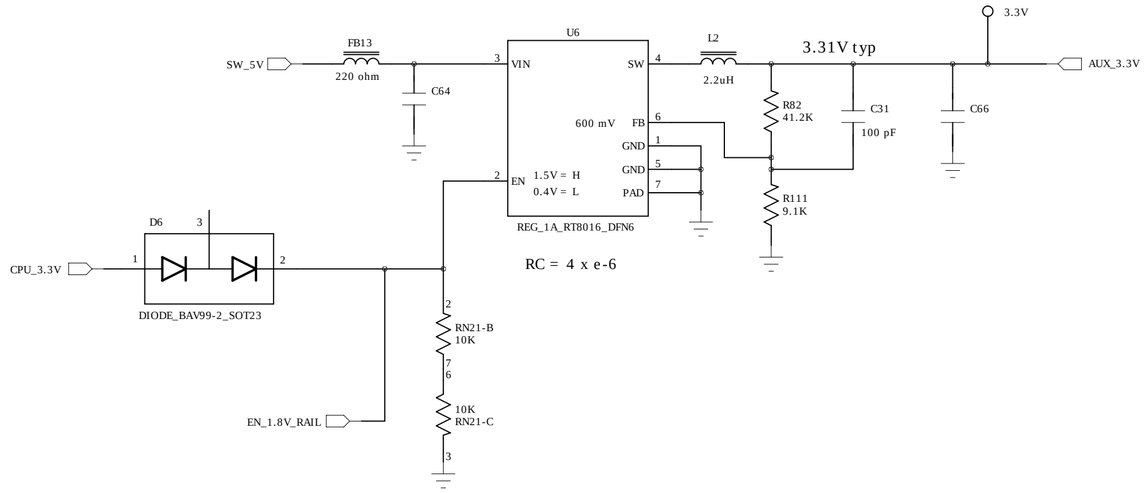
USB and MX286 Switched Power



Rise time of both outputs
measured at ~1V/ms

Technologic Systems	Date April 21, 2014	
Title: TS-7680 5V and Switched Power		
Rev: P1	Designer	Sheet 6 of 18

Aux. 3.3V Reg

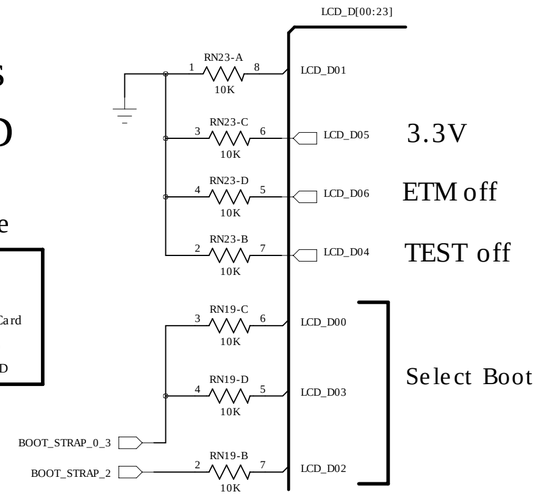


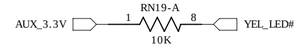
Boot Strap Bias Res.

Defaults to NAND

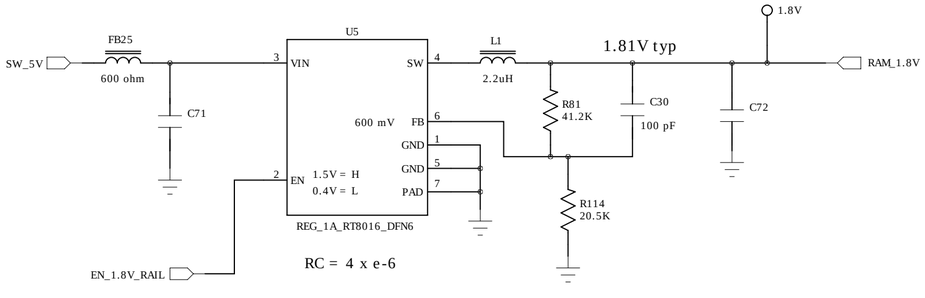
Boot Source

LCD_3	LCD_2	LCD_1	LCD_0	
0	0	1	0	SPI
1	0	0	1	SD Card
0	0	0	0	USB
0	1	0	0	NAND

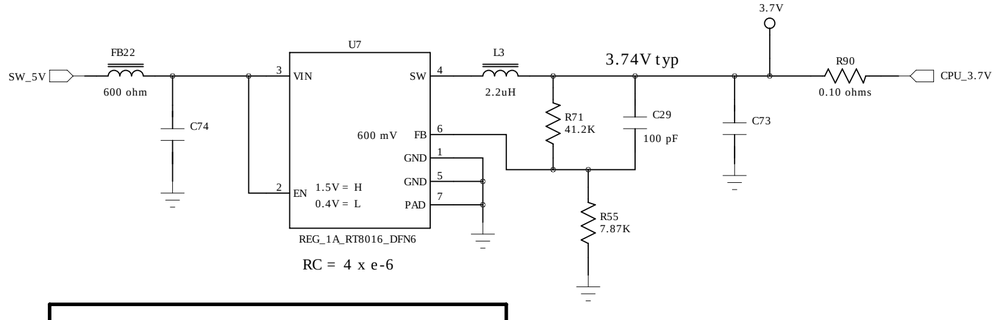




RAM 1.8V Reg



CPU BATT 3.7V



This Reg only required for extra low power mode

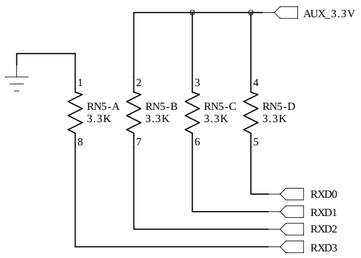
FB7 not installed when this reg. is used

Requires a positive pulse on PSWITCH

Technologic Systems	Date April 21, 2014	
Title: TS-7680 AUX Power Reg, Boot Strap		
Rev: P1	Designer	Sheet 7 of 18

10/100 Ethernet 4-Port Switch

"0111" = RMII MAC mode



Total 88E6020 100 Mbit

Current Drain includes
2 Ports with Mag CT

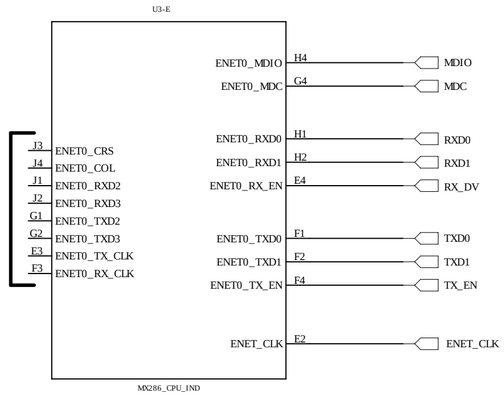
3.3V Rail = 20 mA
1.8V Rail = 80 mA
1.2V Rail = 62 mA

Power Down mode
42 mA on 1.2V rail
0 mA on other rails

Pull-downs default P6
to port disabled mode

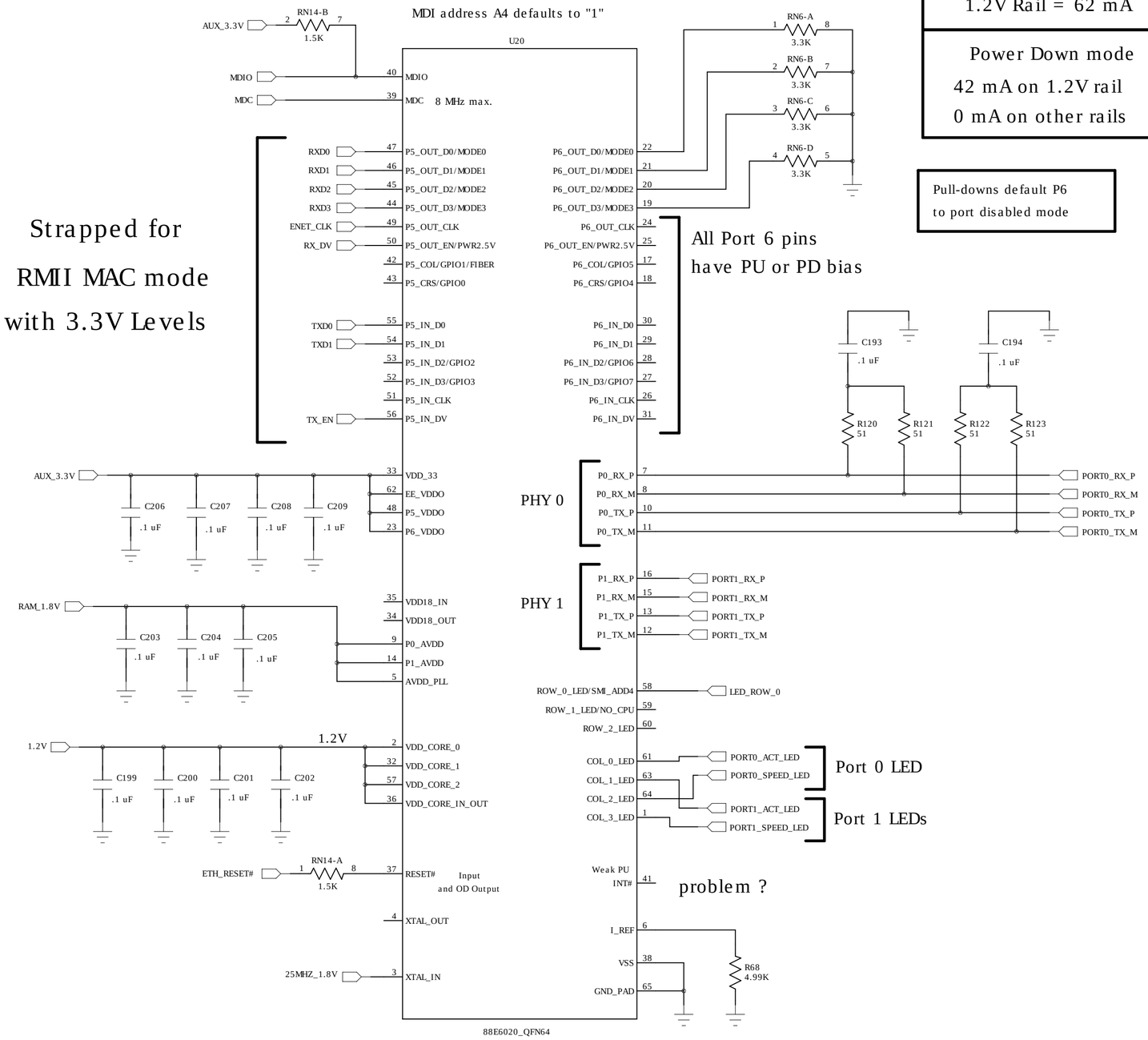
MX283

NC on MX283



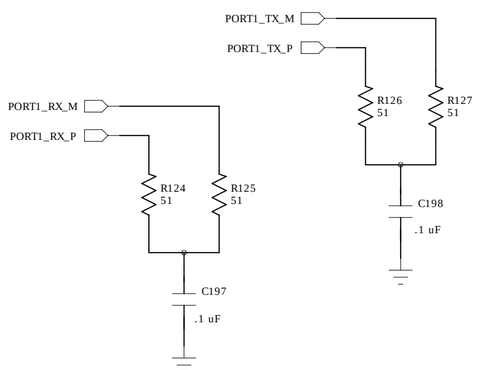
Strapped for
RMII MAC mode
with 3.3V Levels

MDI address A4 defaults to "1"



All Port 6 pins
have PU or PD bias

Requires Reset# asserted
for 10 ms after power



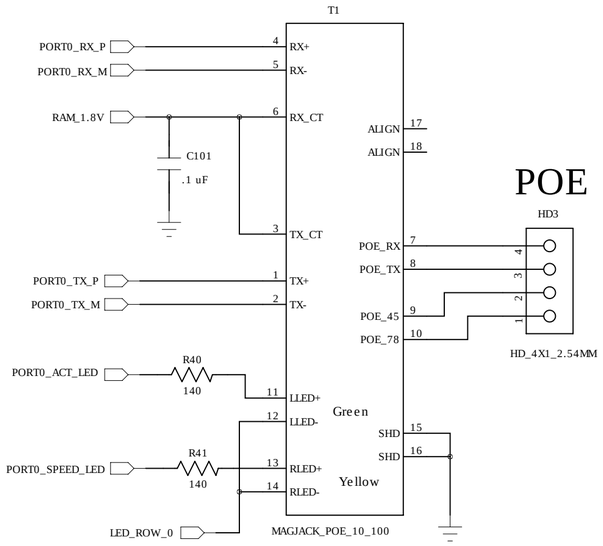
Auto MDIX is supported

Polarity Correction also supported

Technologic Systems	Date April 21, 2014	
Title: TS-7680 Ethernet Switch		
Rev: P1	Designer	Sheet 8 of 18

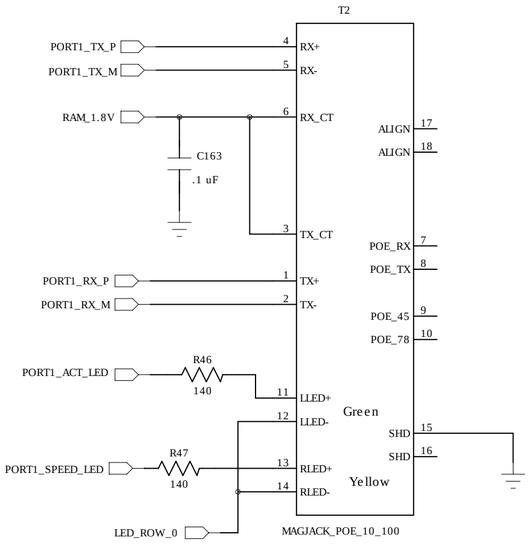
Port #0

10/100 MagJack



Port #1

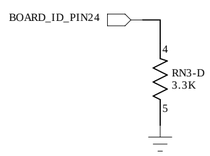
10/100 MagJack



Test LEDs on Prototype

Pin 16 deleted from GND
for layout purposes

Board ID



M0 Board ID

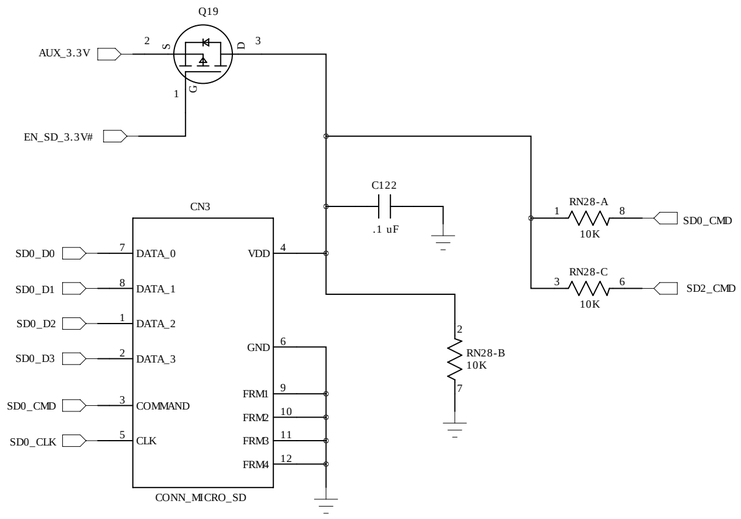
Pin 22	Pin 23	Pin 24	
1	x	1	TS-7670
1	1	0	TS-7680

Assumes weak PU on these 3 pins

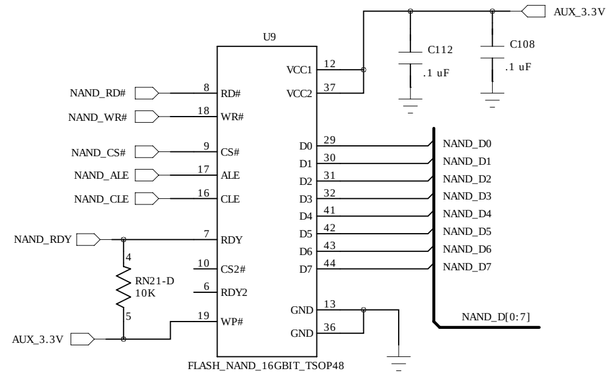
Technologic Systems	Date April 21, 2014	
Title: TS-7680 MagJacks		
Rev: P1	Designer	Sheet 9 of 18

Flash Memory

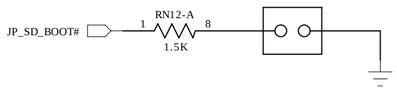
Micro SD Card Socket



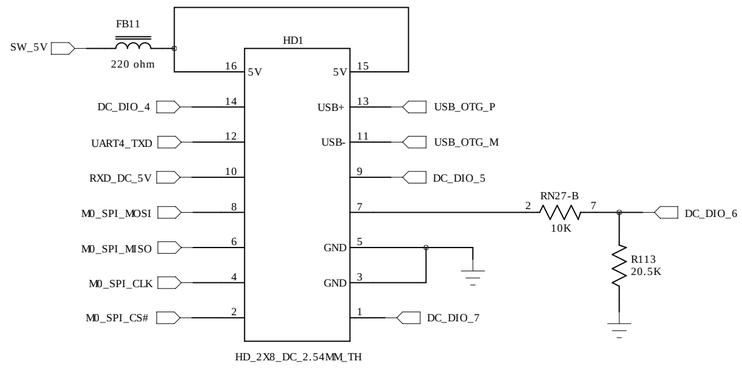
NAND Flash



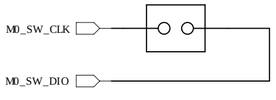
SD Boot Jumper



Daughter Card Interface



MD Program Header



MT7 MT125 MT8 MT125 MT9 MT125

Technologic Systems	Date April 21, 2014	
Title: TS-7680 NAND and SD Card		
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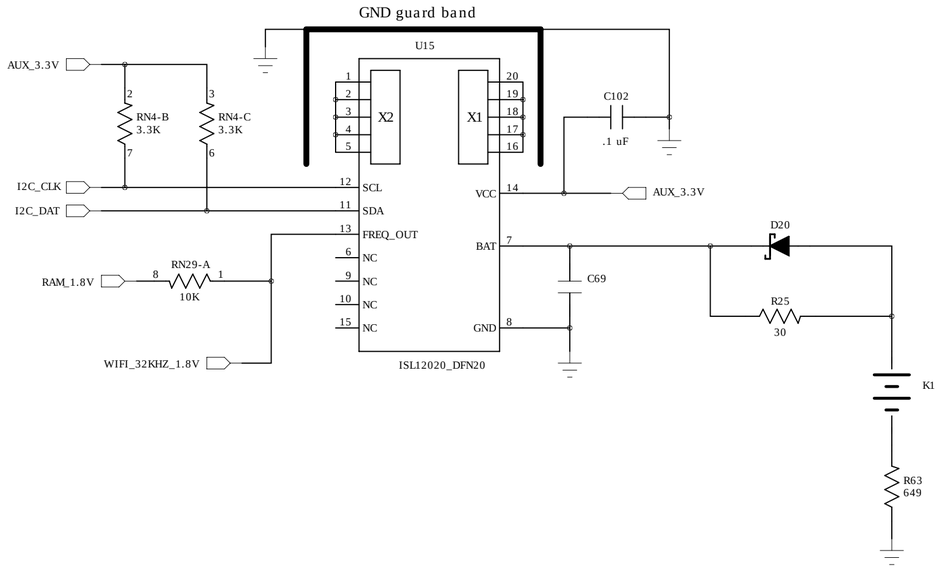
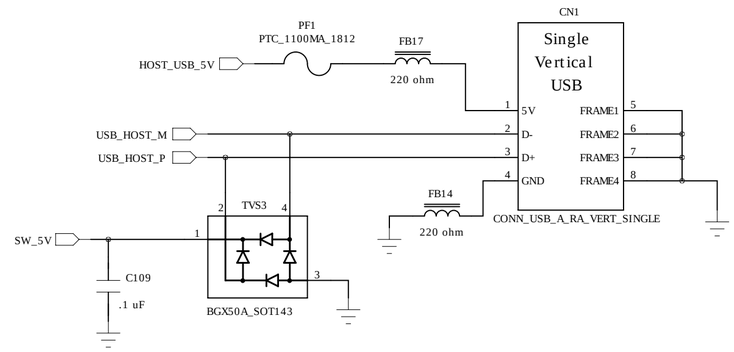
RTC and Host USB

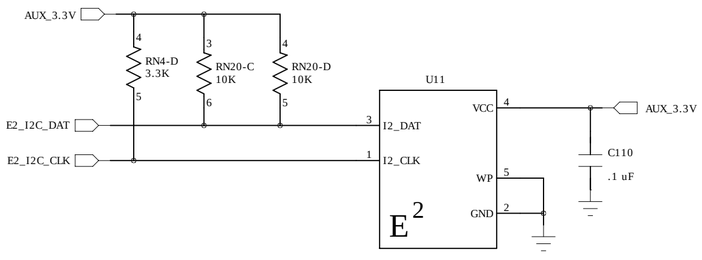
RTC and Temp. Sensor



External Host USB Port



EEPROM 1 Kbyte



For Calibration Values

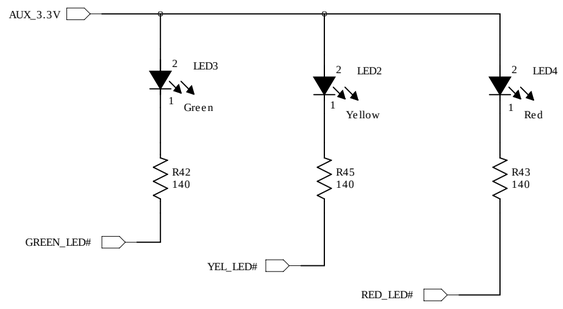
Warning

There is a I2C address conflict

between the RTC RAM and the EEPROM

EEPROM must use separate I2C bus

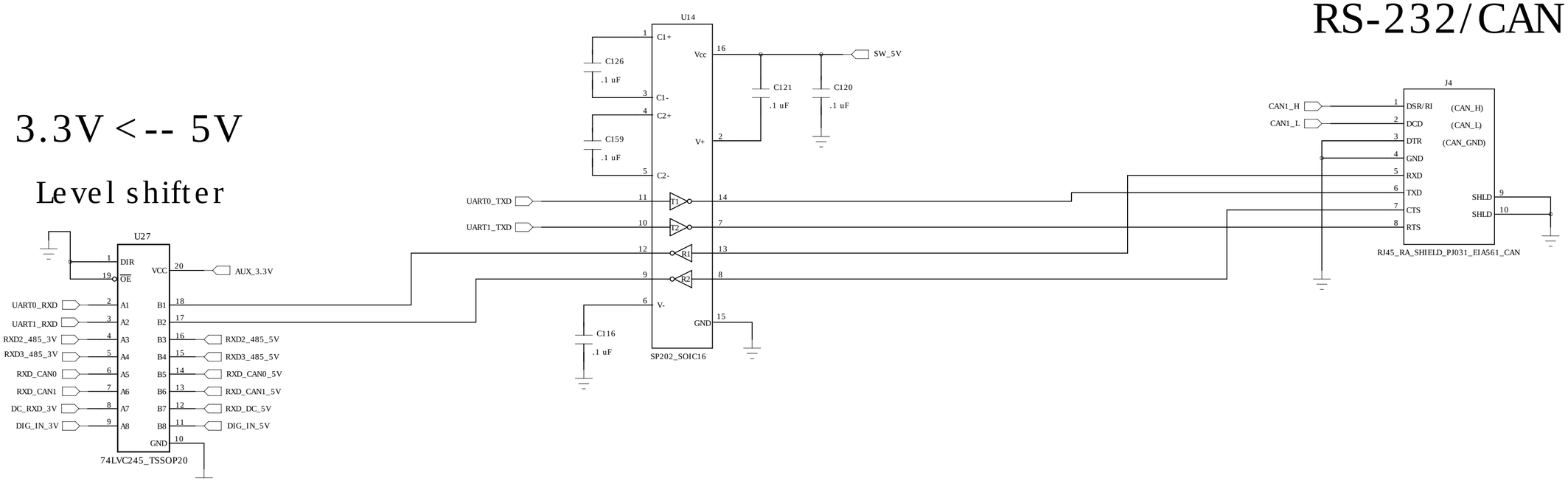
SMT RA LEDs



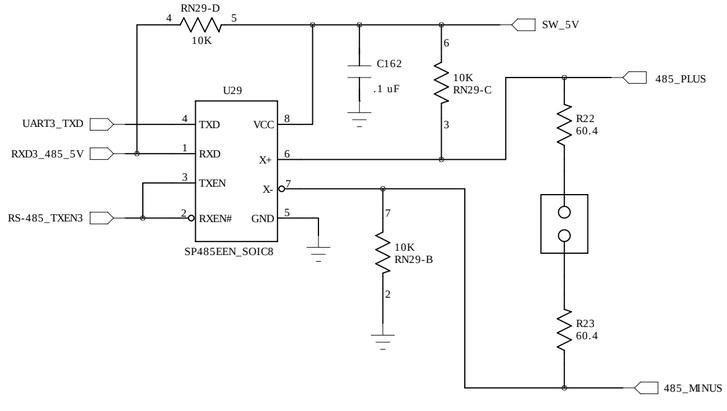
Technologic Systems	Date April 21, 2014	
Title: TS-7680 RTC and Host USB		
Rev: P1	Designer	Sheet 11 of 18

RS-232 Ports and Daughter Card Headers

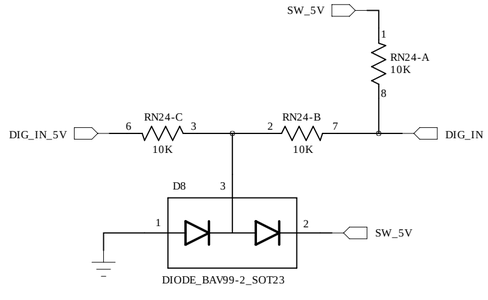
RS-232 Transceiver

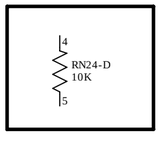


STC RS-485 Driver



Dig. Input



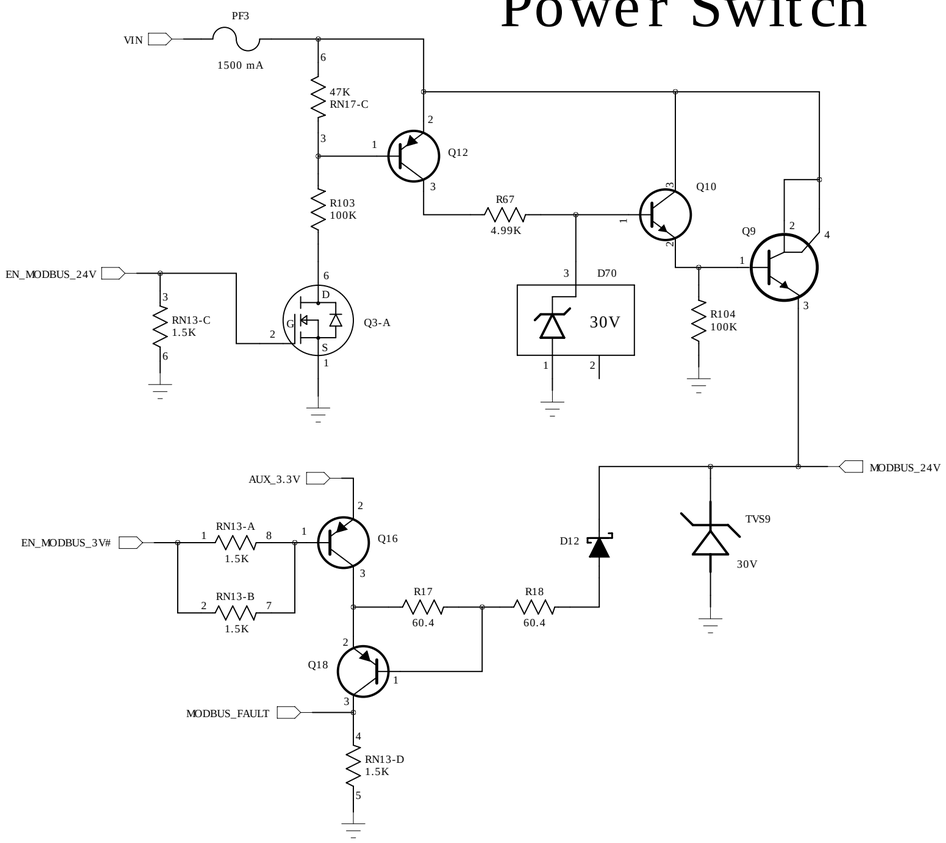


Do not use

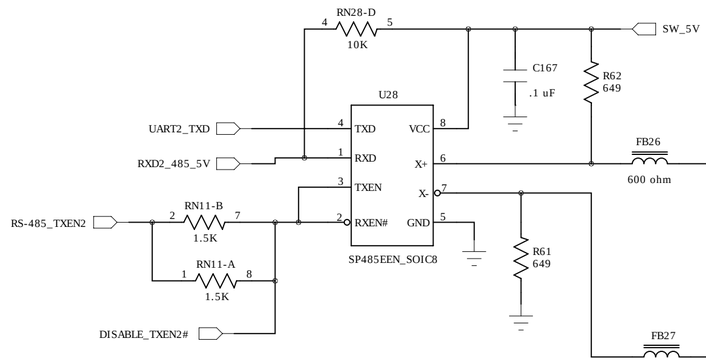
Technologic Systems	Date April 21, 2014	
Title: TS-7680 RS-232 Ports		
Rev: P1	Designer	Sheet 12 of 18

Mod Bus RS-485 and CAN Ports

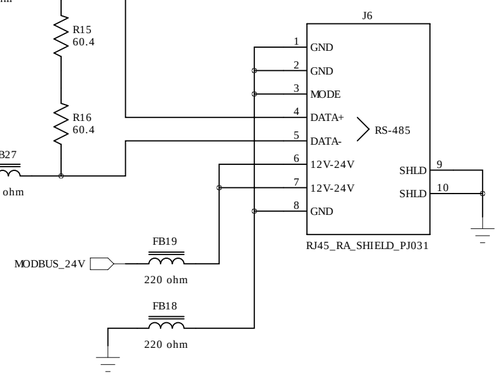
Modbus Power Switch



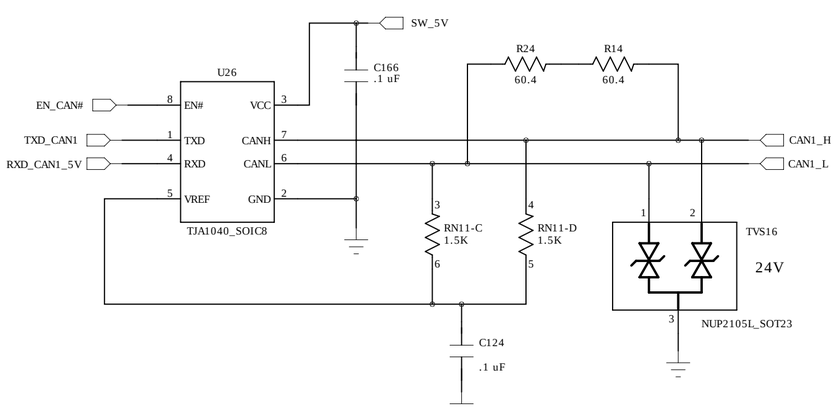
RS-485 Driver



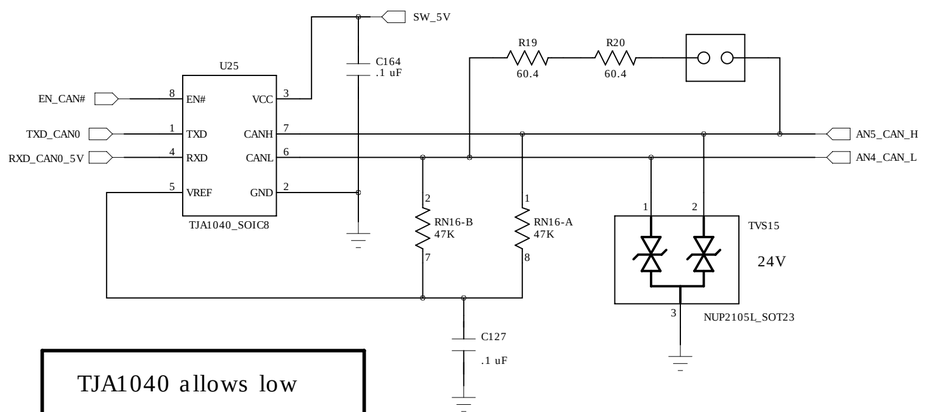
Modbus RJ45



CAN_1 Tranceiver

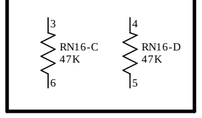


CAN_0 Tranceiver



TJA1040 allows low power 15 uA mode

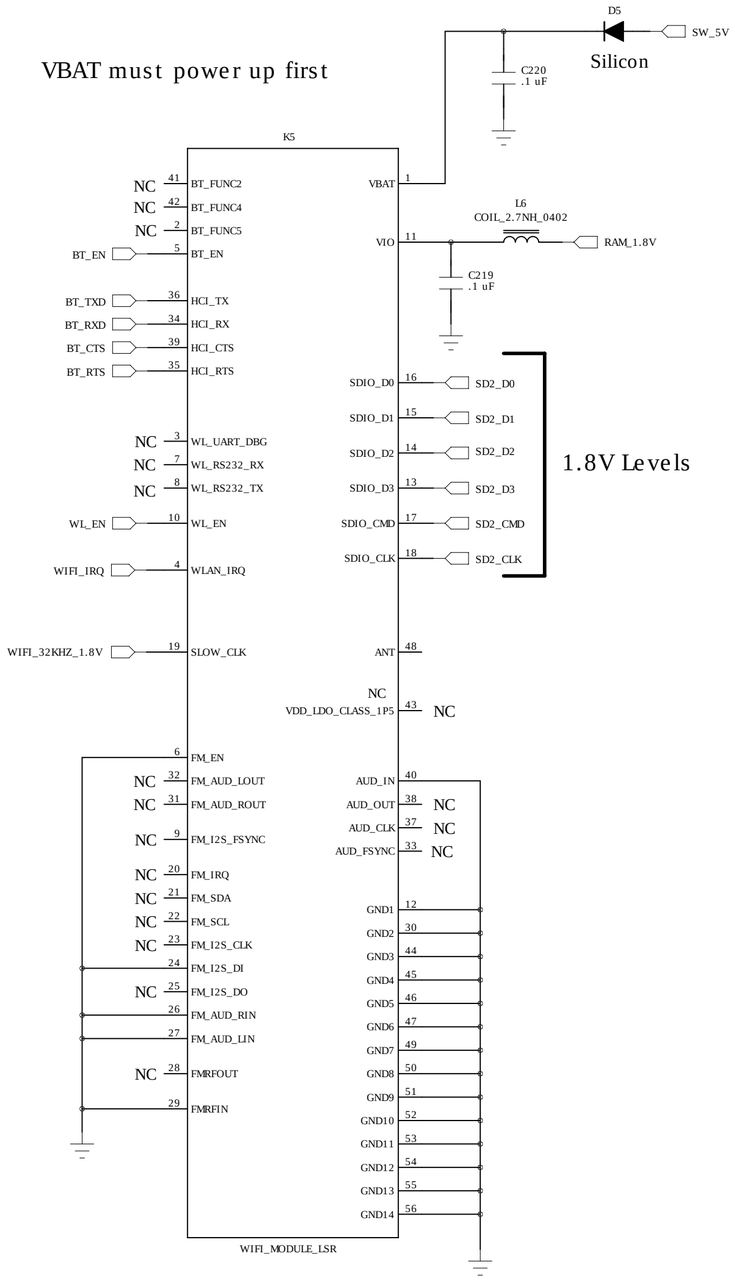
Do Not Use



Technologic Systems		Date April 21, 2014
Title: TS-7680 Modbus and CAN		
Rev: P1	Designer	Sheet 13 of 18

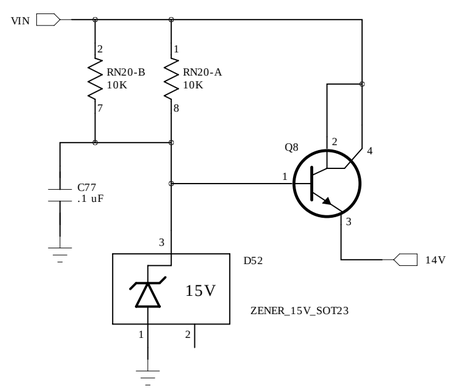
WiFi Radio

All I/O must be 1.8V levels

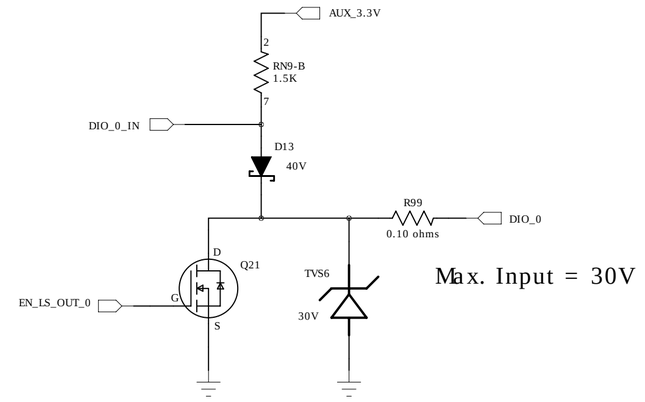


DAC

14V Supply

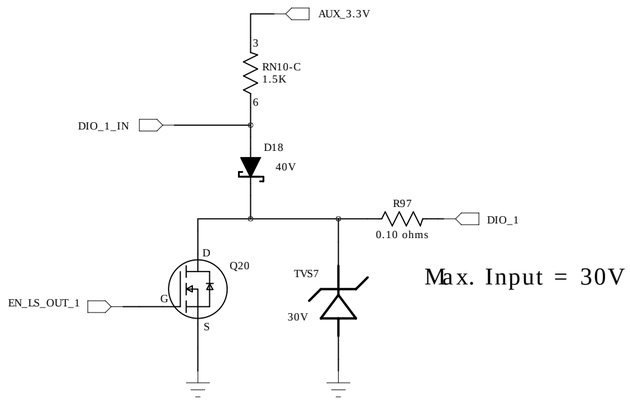


DIO_0



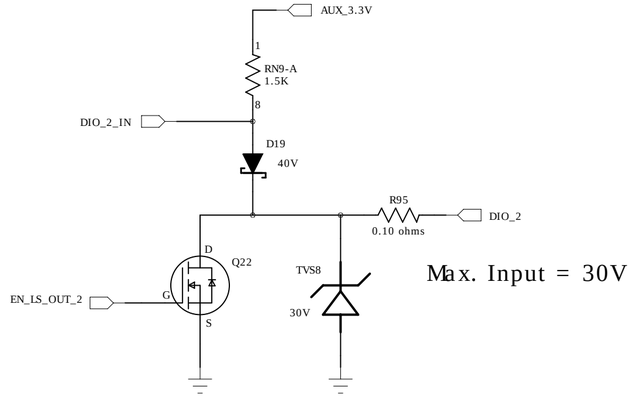
Sinks 500 mA

DIO_1



Sinks 500 mA

DIO_2



Sinks 500 mA

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iCE40 FPGA

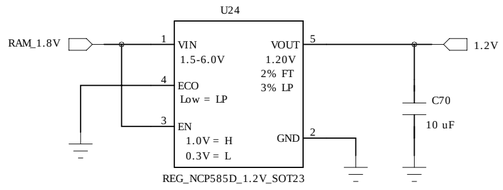
FPGA required for:

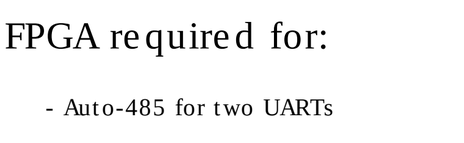
- Auto-485 for two UARTs
- PWMs for DACs
- providing serial port MUXing
- BlueTooth Level Shifting
- Additional I/O
- Daughter Card Functions

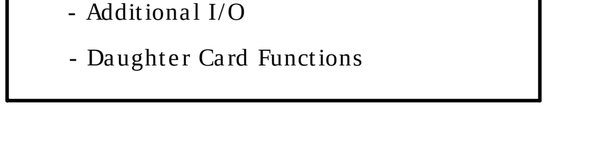
Bank 0 = 1.8V levels

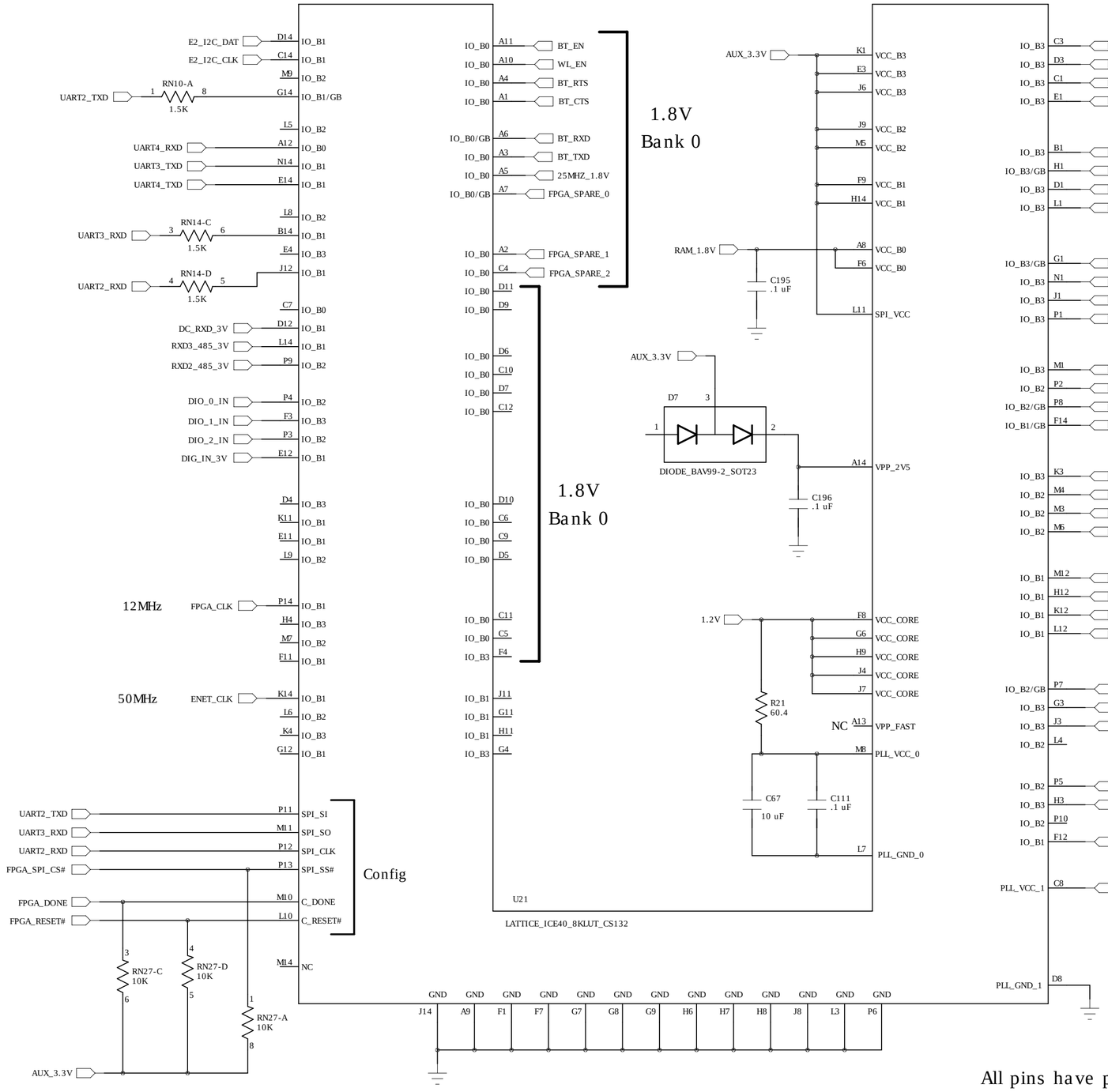
All other Banks = 3.3V

1.2V Regulator









PLL_1 can not be used

If SPI_CS# is high at POR
FPGA configures from NVCM
unless it is blank, then it
tries to load from SPI Flash

If SPI_CS# is low at POR
FPGA waits for external SPI
configuration.
Also used to write to NVCM

All pins have prog. PU resistor
Schmitt Trig. on all Inputs
10 MHz min clock for PLL
No Internal clock

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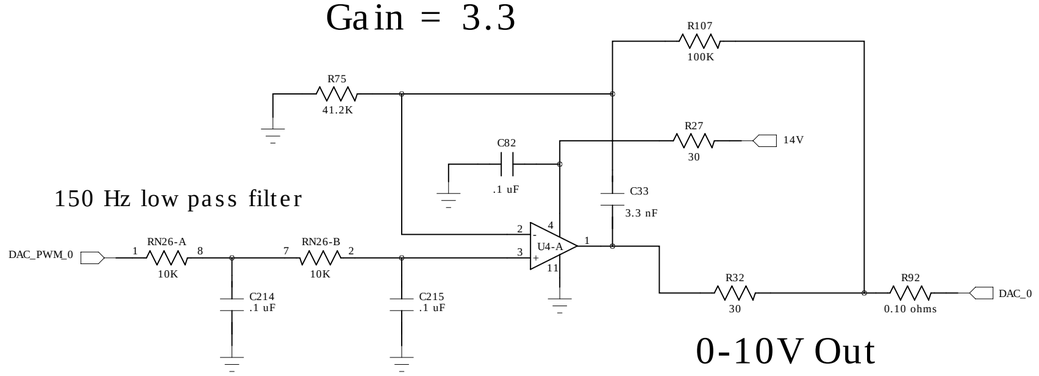
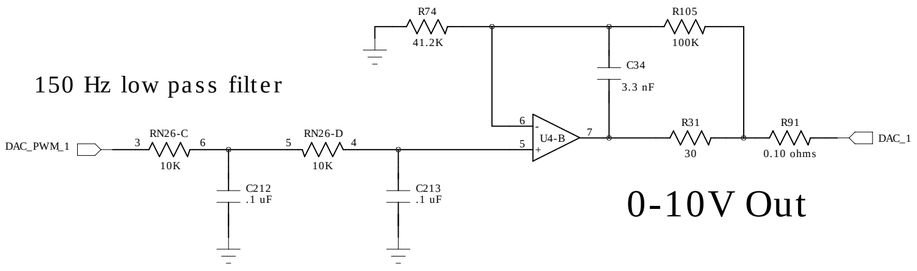
10-bit DACs

Gain = 3.3



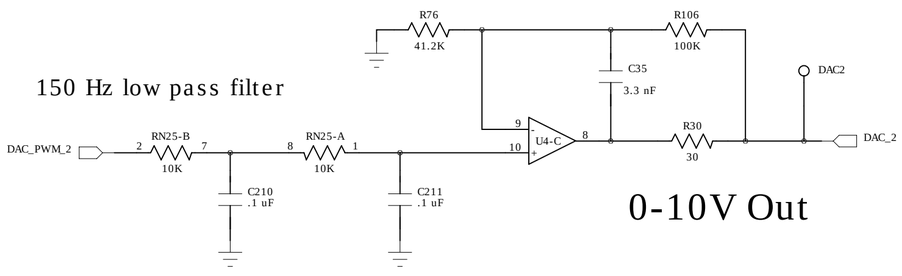
0-10V Out

Gain = 3.3



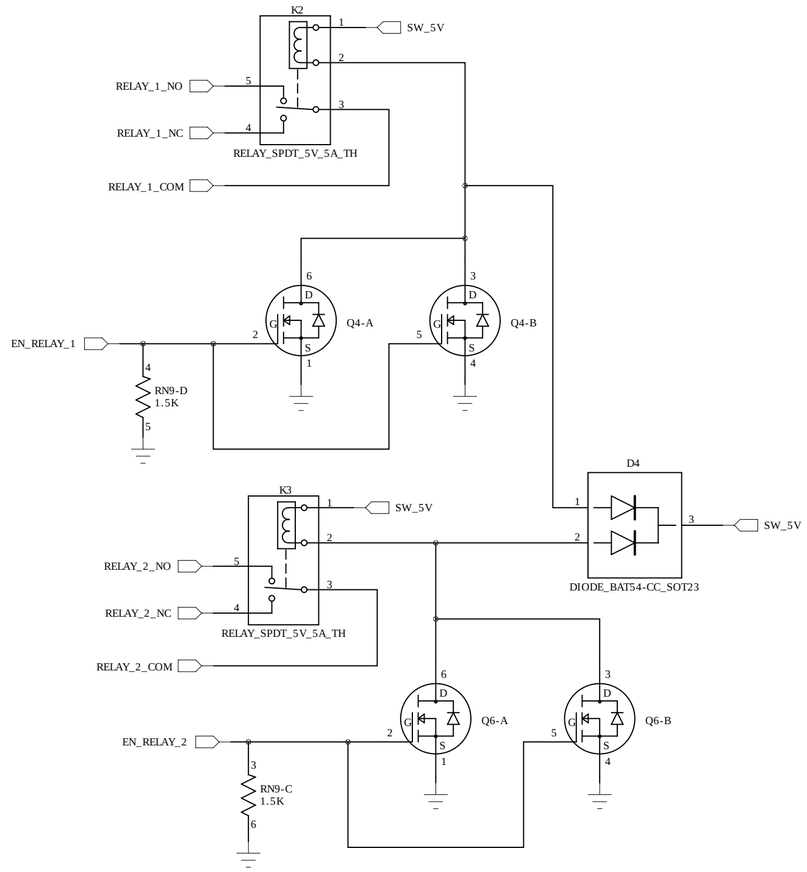
0-10V Out

Gain = 3.3

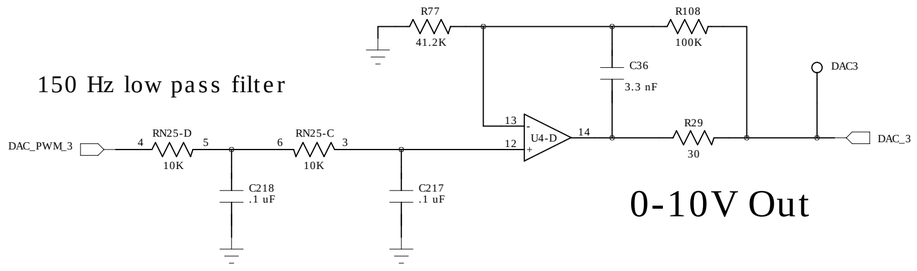


0-10V Out

Relays



Gain = 3.3



0-10V Out

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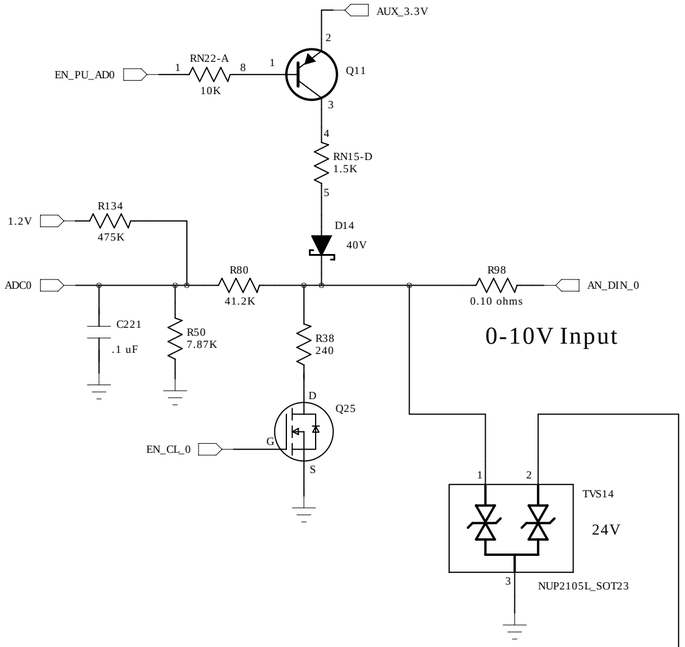
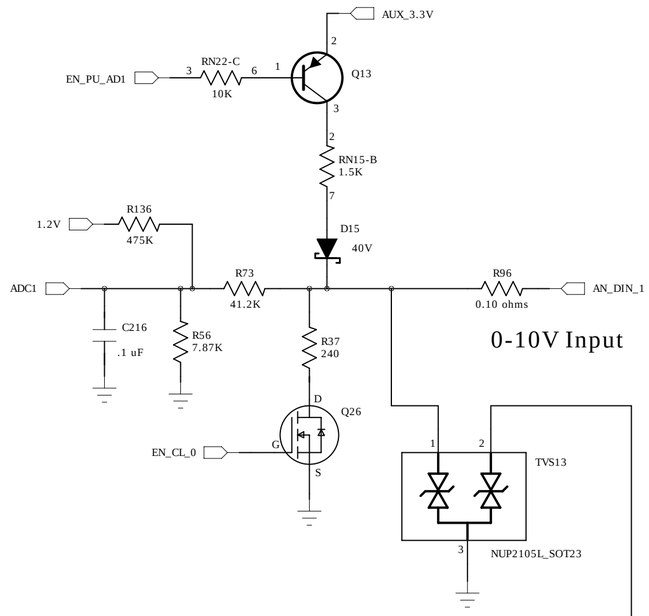
Analog In Channels

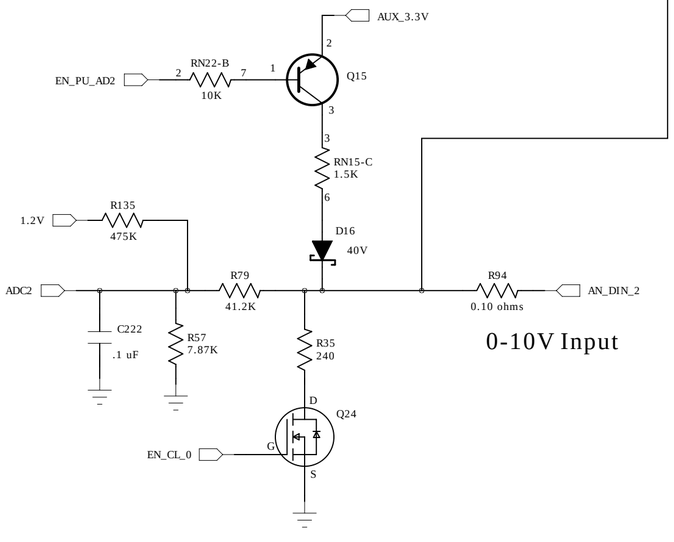


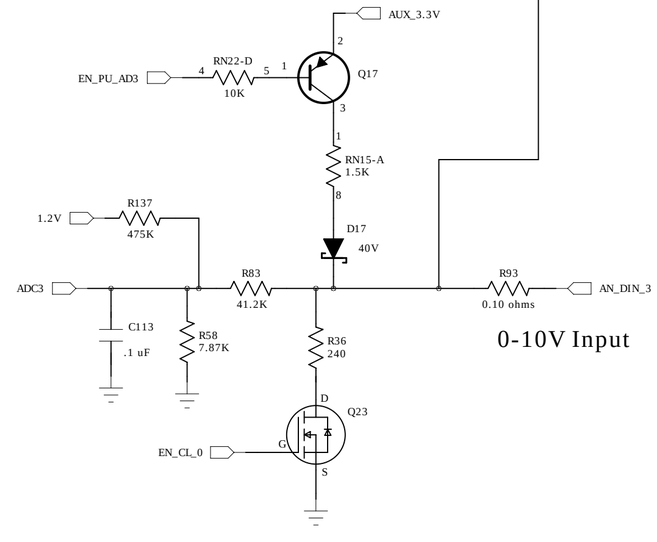


By adjusting resistor values

All A/D Inputs can be converted

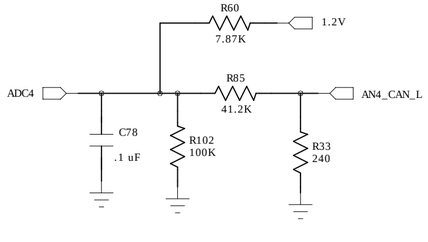
to Bipolar, but must remove FETs

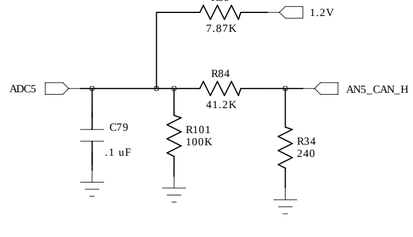




Bipolar Analog Inputs

-5V to +5V Input Range





R33 and R34 not populated

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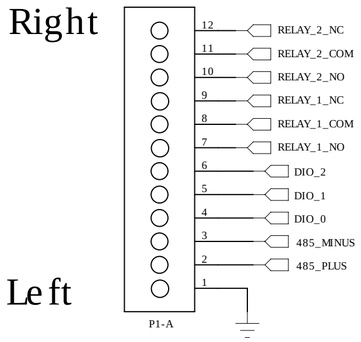
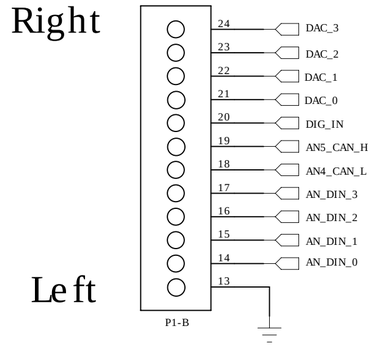
24 Screw Term. Positions

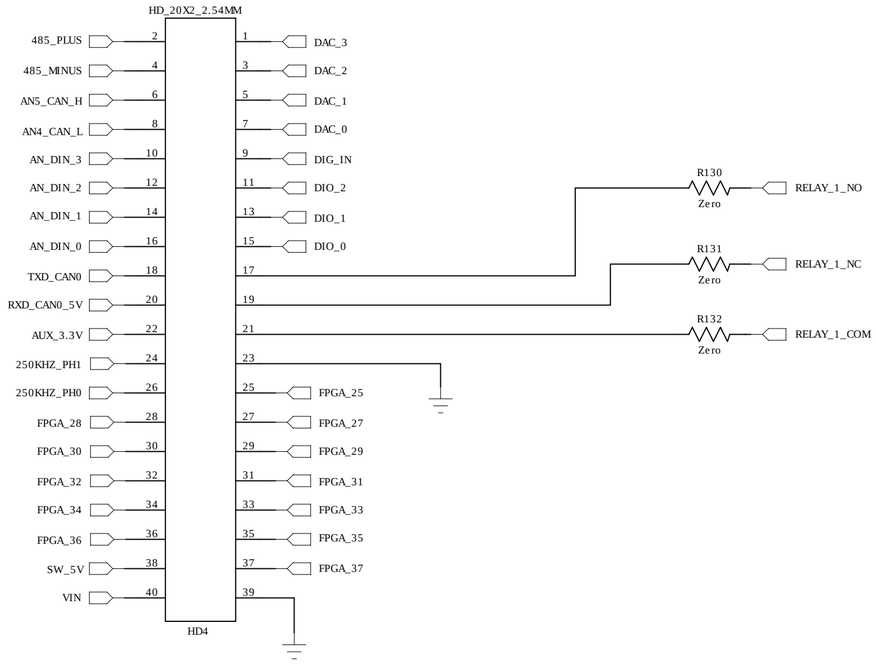
Top Row



Bottom Row



DC STC Header



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