Comments:

Board can be powered by 8-28 VDC or 24VAC
SiLab uC is powered up first, then it controls the MX286 start up
SiLab uC does these functions:
- Controls MX286 power up sequence
- USB Device to Console conversion
- Controls MX286 Sleep mode
- Can read Push Switch for Wake-up
- Measures Analog Power Rails
- Controls SuperCap charging
- Can turn on Blue LED

All Parts are Industrial Temp

Rev. B --> C Changes

1) SiLab pin 30 now controls current to VREF
2) Added Jumper for disabling SuperCap charging
3) TVs4 clamp voltage changed - to avoid false USB 5V Detection
4) Changed SPI Flash to 2MB size
5) Changed SiLab uC to 64K Flash version
6) Moved SD card socket to get more antenna room
7) Added FB8 and 9 to allow Ubiquiti WiFi power
8) Added R129 and 133 for Quickloadz special
USB Device Port and SiLab uC

SiLab 4.7V

USB Device Port

"No Charge" Jumper

Blue LED

Push Switch

Scale = 5.57%
Scale = 44.6%
Scale = 50%
Scale = 50%
Scale = 50%

A/D full scale = 2.50V

24 mA max load

Technologic Systems
Title: TS-7680 SiLab uC and USB Device port
Date Nov. 7, 2015
Rev: C Designer Sheet 2 of 20
Title: Rev: Designer Sheet of TS-7680 MX286 CPU

Date: Nov. 7, 2015

Technologic Systems

UARTs, ADC

- SD Card
- SPI Boot

NAND, PWM

JTAG, I2C

LCD

EN_SPI_BOOT_FLASH is set low by CPU after done booting from SPI
Then SPI signals are changed to UART2 and UART3 functions

All JTAG have 47K internal PU except RTCK
PSWITCH can be driven to 3.3V if a series 10K res is used.
8-40 VDC or 10-28 VAC
Power Input

**5V Power Supply (2000 mA)**

C81 must be very near U17

- **Power Input**: 8-40 VDC or 10-28 VAC
- **Output**: 5V and Switched Power
- **Rise time of both outputs measured at ~1V/ms**

**USB and Daughter Switched Power**

**Switched 5V Power**

FB26 not pop if SCap used

Scale = 44.6%

.063 hole
**Aux. 3.3V Reg**

```
Aux_3.3V YEL_LED#
CPU_3.3V
SW_5V

RAM 1.8V Reg

EN_1.8V_RAIL
DC_DIO_4
DC_DIO_5
USB
VIN
DC_5V
DC_RXD_5V
DC_TXD_3V
POE_TX
POE_RX
POE_45
POE_78
USB_OTG_P
USB_OTG_M

BOOT Strap Bias Res.

Strapped
SPI Boot

Boot Source

Select Boot

3.3V
ETM off
TEST off

Daughter Card Interface"
Auto MDIX is supported
Polarity Correction also supported
Port #0
10/100 MagJack

Port #1
10/100 MagJack
RS-232 Ports and Daughter Card Headers

RS-232 Transceiver

3.3V <-- 5V
Level shifter

RS-232/CAN

RS-232 Transceiver

Dig. Input

STC RS-485 Driver
Mod Bus RS-485 and CAN Ports

Modbus
Power Switch

RS-485 Driver
RJ45

Modbus
RJ45

CAN_0 Tranceiver

CAN_1 Tranceiver
WiFi Radio

All I/O must be 1.8V levels

DAC

14V Supply

DIO_0

Max. Input = 30V

Sinks 500 mA

DIO_1

Max. Input = 30V

Sinks 500 mA

DIO_2

Max. Input = 30V

Sinks 500 mA
FPGA required for:
- Auto-485 for two UARTs
- PWMs for DACs
- MUX for all UARTs
- BlueTooth Level Shifting
- Additional I/O
- HD4 Daughter Card (Future)

UART2 and UART3 changed to SPI when Booting from SPI
Analog In Channels
0-10V or 4-20mA Inputs

enables 4-20mA Input

enables 4-20mA Input

enables 4-20mA Input

enables 4-20mA Input

enables 4-20mA Input

enables 4-20mA Input

enables 4-20mA Input

enables 4-20mA Input

enables 4-20mA Input

enables 4-20mA Input
SuperCap 20 Second Power Hold

20 seconds assumes 3 watt load
SuperCaps charged to 4.8V
Functions down to SuperCap = 2.8V
V_INT is normally 5V
But when Mains fail, and in Power Hold, it will range from 4.5V down to 2.0V
24 Screw Term. Positions

Top Row

Bottom Row

DC Header

FPGA_21, 23, 25, 27, 29 go to MX286 (S)
FPGA_22 thru FPGA_35 go to FPGA (14)
FPGA_29 to SiLab uC

17 STC positions go to HD4