Board can be powered from USB
or by 8-28VDC, or by 24VAC

Cortex M0 is powered up first, then it controls MX286 start up

Cortex M0 does these functions:
- Controls MX286 power up sequence
- Controls MX286 Boot Strapping
- USB Device to Console conversion
- Controls Blue LED
- Can read Push Switch
- Measures Analog Vin value
- Reads SD_BOOT Jumper
- Board ID

Notes:

1) Check Ethernet LEDs
   RAM_1.8V rail turns on later than TS-7670
   Test 24VAC power

   For Modbus 1042K baud operation - use DMA?

2) Serial Port RX DMA on MX286 says "must be multiples of 4 bytes"
   TX DMA does not say restricted to 4 byte multiples

3) BOM Warning:
   R33, R34 and HD3 not pop
   JP1 thru JP5 is 5x2 header = 15-3070-7
   CAN ports are options
   128MB and 256MB RAM sizes

Warning: 1.8V Levels

- SD2 signals
- WIFI_IRQ
- FPGA_SPARE_0
- FPGA_SPARE_1
- FPGA_SPARE_2

UART2 and UART3 changed to SPI
when programming FPGA

Serial Port Usage

UART0 = RS-232
UART1 = RS-232
UART2 = Modbus
UART3 = STC RS-485
UART4 = Blue or DC
Debug = Console/DC
DC = Daughter Card
STC = Screw Term. Conn.

I/O Diff from TS-7670

UART0_RTS -> E2_I2C_CLK
UART0_CTS -> E2_I2C_DAT
UART1_CTS -> WIFI_IRQ (1.8V)
DC_DIO_9 -> DISABLE_TXEN2#
EN_232_TRANS = No Connect
EN_ETH_3.3V# = No Connect

GPS_PPS_OUT -> FPGA_DONE
U3.R3 = FPGA_RESET#
U3.U4 = FPGA_SPI_CS#
U3.T4 = FPGA_IRQ
UART1_RTS = FPGA_SPARE_0 (1.8V)
U3.U5 = FPGA_SPARE_1 (1.8V)
DC_DIO_8 = FPGA_SPARE_2 (1.8V)

Changed VIN A/D scaling!
USB Device Port and Cortex M0

Cortex M0

USB Device Port

3.3V Reg. for M0

Blue LED

Push Switch

Brown out Detect

Technologic Systems
Title: TS-7680 Cortex M0 Controller
Rev: P1
Designer
Sheet 2 of 18

Date: April 21, 2014
Battery pin supplies current to charge battery.

DCDC_BAT pin is power input for DCDC converters -- connect direct to battery.

PSWITCH can be driven to 3.3V if a series 10K resistor is used.
DDR2 SDRAM (128 or 256 MByte)

Length of this trace is equal to [CLK + Data] lengths
Data = Average length of all data traces
5V Power Supply (2000 mA)

Power Input

For 24VAC power
C99 must be installed
JMP must not be pop.

Test on MAC104
470uF = 4Vpp ripple
with 1A load on 5V

USB and MX286
Switched Power

Rise time of both outputs
measured at ~1V/ms

D11 allows USB to power MX286
This will only work if 3.7V
Reg (U7) is powering MX286
**Aux. 3.3V Reg**

- **Boot Strap Bias Res.**
  - Defaults to NAND
  - Boot Source
    - LCD[0]: 0 0 0 0 LCD[3]
    - EIM off
    - TEST off
    - Select Boot

**RAM 1.8V Reg**

- **CPU BATT 3.7V**
  - This Reg only required for extra low power mode
  - FB7 not installed when this reg. is used
  - Requires a positive pulse on PSWITCH

---

**Title:** TS-7680 AUX Power Reg, Boot Strap

**Date:** April 21, 2014

**Rev:** P1

---
10/100 Ethernet 4-Port Switch

Auto MDIX is supported
Polarity Correction also supported
Port #0
10/100 MagJack

Test LEDs on Prototype

Port #1
10/100 MagJack

Pin 16 deleted from GND for layout purposes

Board ID

<table>
<thead>
<tr>
<th>M0 Board ID</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin 22</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>1</td>
</tr>
</tbody>
</table>

Assumes weak PU on these 3 pins
Flash Memory

Micro SD Card Socket

SD Boot Jumper

M0 Program Header

NAND Flash

Daughter Card Interface
RTC and Host USB

RTC and Temp. Sensor

External Host USB Port

SMT RA LEDs

EEPROM 1 Kbyte

Warning

There is a I2C address conflict between the RTC RAM and the EEPROM. EEPROM must use separate I2C bus.
RS-232 Ports and Daughter Card Headers

RS-232 Transceiver

3.3V <-- 5V
Level shifter

RS-232/ CAN

Dig. Input

Do not use

STC RS-485 Driver
WiFi Radio

All I/O must be 1.8V levels

VBAT must power up first

1.8V Levels

DAC

14V Supply

Max. Input = 30V
Sinks 500 mA

DIO_0

Max. Input = 30V
Sinks 500 mA

DIO_1

Max. Input = 30V
Sinks 500 mA

DIO_2

Sinks 500 mA
iCE40 FPGA

Bank 0 = 1.8V levels
All other Banks = 3.3V

1.2V Regulator

FPGA required for:
- Auto-485 for two UARTs
- PWMs for DACs
- providing serial port MUXing
- BlueTooth Level Shifting
- Daughter Card Functions

1.2V Regulator

PLL_1 can not be used

If SPI_CS# is high at POR
FPGA configures from NVCM
unless it is blank, then it
tries to load from SPI Flash

If SPI_CS# is low at POR
FPGA waits for external SPI
configuration.
Also used to write to NVCM

Technologic Systems

Title: TS-7680 FPGA

Rev: P1  Designer  Sheet: 15 of 18

Date: April 21, 2014
10-bit DACs

Gain = 3.3

150 Hz low pass filter

0-10V Out

Relays

Gain = 3.3

150 Hz low pass filter

0-10V Out

Gain = 3.3

150 Hz low pass filter

0-10V Out

Gain = 3.3

150 Hz low pass filter

0-10V Out
Analog In Channels

By adjusting resistor values
All A/D Inputs can be converted
to Bipolar, but must remove FETs

Bipolar Analog Inputs

-5V to +5V Input Range

R33 and R34 not populated
24 Screw Term. Positions

Top Row

Bottom Row

DC STC Header