Termination
Resistors

FPGA 1.2V Reg.

3.3V --> 5V
Level Shifter
LAN8710i can power sequence in any order

Ethernet 1.2V Reg can be turned off by having LED1 high
Using SW. 1.2V Reg saves 13 mA @ 5V
Total chip power: 160mw → 100 mw

<table>
<thead>
<tr>
<th>Pin</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>RXD0/ MODE0</td>
</tr>
<tr>
<td>2</td>
<td>RXD1/ MODE1</td>
</tr>
<tr>
<td>3</td>
<td>RXD2/ MODE2</td>
</tr>
<tr>
<td>4</td>
<td>RXD3/ MODE3</td>
</tr>
<tr>
<td>5</td>
<td>TXD0/ INT1</td>
</tr>
<tr>
<td>6</td>
<td>TXD1/ INT2</td>
</tr>
<tr>
<td>7</td>
<td>TXD2/ INT3</td>
</tr>
<tr>
<td>8</td>
<td>TXD3/ INT4</td>
</tr>
<tr>
<td>9</td>
<td>MDC</td>
</tr>
<tr>
<td>10</td>
<td>MIO</td>
</tr>
<tr>
<td>11</td>
<td>TXEN</td>
</tr>
<tr>
<td>12</td>
<td>TX_CLK</td>
</tr>
<tr>
<td>13</td>
<td>TX_R</td>
</tr>
</tbody>
</table>
FPGA with 8000 LUTs

SMC Data Bus

SMC Bus from CPU

SMC BE2#
SMC BE1#
SMC CLA#
SMC CLB#
SMC D[00: 15]
SMC D01
SMC D02
SMC D03
SMC D04
SMC D05
SMC D06
SMC D07
SMC D08
SMC D09
SMC D10
SMC D11
SMC D12
SMC D13
SMC D14
SMC D15

USB_DEV_M
USB_DEV_P

CPU_UART_TXD
FPGA_JTAG_DOUT
FPGA_JTAG_CLK
FPGA_JTAG_TM S
FPGA_25M HZ
FPGA_JTAG_DIN

SM C_CS1#
SM C_L UA#
SM C_RDY
SM C_IRQ
SM C_CLK
SM C_WE#
SM C_D[00: 15]
SM C_D01
SM C_D02
SM C_D03
SM C_D04
SM C_D05
SM C_D06
SM C_D07
SM C_D08
SM C_D09
SM C_D10
SM C_D11
SM C_D12
SM C_D13
SM C_D14
SM C_D15

103 IO_B2
143 IO_B0
141 IO_B0
144 IO_B0
142 IO_B0
138 IO_B0
120 IO_CL K_B0
28 IO_CL K_B6
19 IO_B7
22 IO_CL K_B7
79 JTAG_TM S_B8
81 JTAG_CL K_B8
80 JTAG_DIN_B8
82 JTAG_DOUT_B8
20 IO_INIT# _B7
90 IO_B2
30 IO_CL K_B6
13 OUT_CSSPIN_B7
17 IO_B7
15 IO_B7
16 IO_CCL K_B7
21 IO_CL K_B7
29 IO_B6
11 IN_CSSPIS_B7
2 IO_B7
8 IO_DONE_B7
1 IO_B7
7 IN_PROGRAM # _B7
9 IN_CFG1_B7
6 IO_B7

Input
IN
3 GND1
12 GND2
34 GND3
41 GND4
51 GND5
64 GND6
68 GND7
GND8
GND9
GND10
GND11
GND12
GND13
GND14
GND15

L ATTICE_XP2_144_8K_LUT

The drive s CPU_RESET#

After FPGA_RESET is deasserted
Assert EN_AVDD_OTG#
Then wait another 10-20 mS
before "Un-resetting" CPU

SD Cards

ACT_LED#
SD_POWER#
SD_D3
SD_D1
SD_CL K1
SD_CM D
SD_D0
SD_D2

EN_USB_5V
EN_AVDD_OTG#
RED_L ED#
GREEN_LED#
UN-RESET

Reset
Latch

This drives CPU_RESET#

Page 37 of Data Sheet (Hot Socketing)
Power Supplies can be sequenced in any order
but must be monotonic
All I/O lines are tri-stated during power cycling

i2c bus: 5V tolerant
5V or 3.3V logic
3 modes of 16x16 Block RAM
12 18x18 Multipliers
100 I/O with 144 pin package
I/O ports: 5 PWR, 30 Rx, 20 Tx
Input PLL clock: 10 MHz

Pull-up and pull-down resistors
are 6 to 30K ohm

Rev: A  Date: April 2, 2013
Title: TS-7700 FPGA  Designer
Technologic Systems  Sheet 5 of 9
Micro SD Card Sockets

RTC and Temp. Sensor

CPU Debug UART

Reboot Flag

SD Card LEDs

BAT must be > 2.7V for temp comp to work

Temp takes 68 uA for 22 ms
Once every 1 or 10 min.

Keep normally at logic zero
44-Pin DIO Header

MODE1 and MODE2 states are latched when CPU_RESET# is deasserted

Logic '0' on MODE2 signal forces Boot from SD card

MODE1 and MODE2 have 4.7K resistor pull-ups on TS-7500

Logic '0' on MODE1 forces Console to the TXD and RXD lines

MODE1 and MODE2 states are latched when CPU_RESET# is deasserted

26-Pin DIO Header

USB Host Ports

LED...