1.2V or 1.42V Power Supply

When FETs are on, use a Regulator at 1.2V (JP3 ON)

3.3V Regulator

1.2V Power Supply up to 1000 mA

2.5V Power Supply

Interface to Buck Reg.

5V Switch

USB_AVDD, S_AVDD, T_AVDD

SATA_SVDD, PEX_AVDD

VDD_CPU

VDD_CORE

VDD_M, VDD_3.3V

VDD_O, PCI_VIO

60 ohm typ ON resistance

220 ohm @100mHz
50 microhenry DC
Must enable pull-up resistors for these pins:
SD card DO-D3
SD Power#
SD card WP

Full-Size SD Card Socket

Micro SD Card Socket

5 Channel 10-bit A/D

NV 3.3V Regulator for AVR

SV needed when programming AVR needs 20mA

Vout = 1.24 + (1 - Rtop/Rbot) 70 uA quiescent
DIO Port

- All DIO lines are 5V tolerant.
- DIO_01 thru DIO_15 (odds) are always open drain outputs, initialized to high. They can be used as inputs.
- DIO_08 initializes to an input when output, active high-low. It is programmable in or out.
- DIO_04 is always input. AVR drives pull-up on this pin.
- Pull-up resistors for the open drain outputs.
- Open drain outputs can sink 8 mA, but only source current thru resistor.

LCD Port

- All LCD lines are 5V tolerant.
- LCD03, LCD05, LCD06 init to input when outputs, active high-low. These are programmable I/O.
- LCD07 thru LCD0A are always open drain outputs, initialized to high. They can be used as inputs.
- LCD04 is always output active high-low, init to zero.
- Pull-up resistors for the open drain outputs.
- Open drain outputs can sink 8 mA, but only source current thru resistor.

PC/104 64-pin Connector

Warning:
All I/O and data lines are 5V tolerant, but all other signals must use 3.3V levels.
IR03 must be 3.3V levels.

PC/104 40-pin Connector

51 lines directly into FPGA plus 4 more into CPLD (read only).