TS-7800-V2 P1

Options:

1) MicroChip WiFi radio

2) CN44 (Mini-PCIe)

SATA Conn. CN10 must be removed when CN44 installed

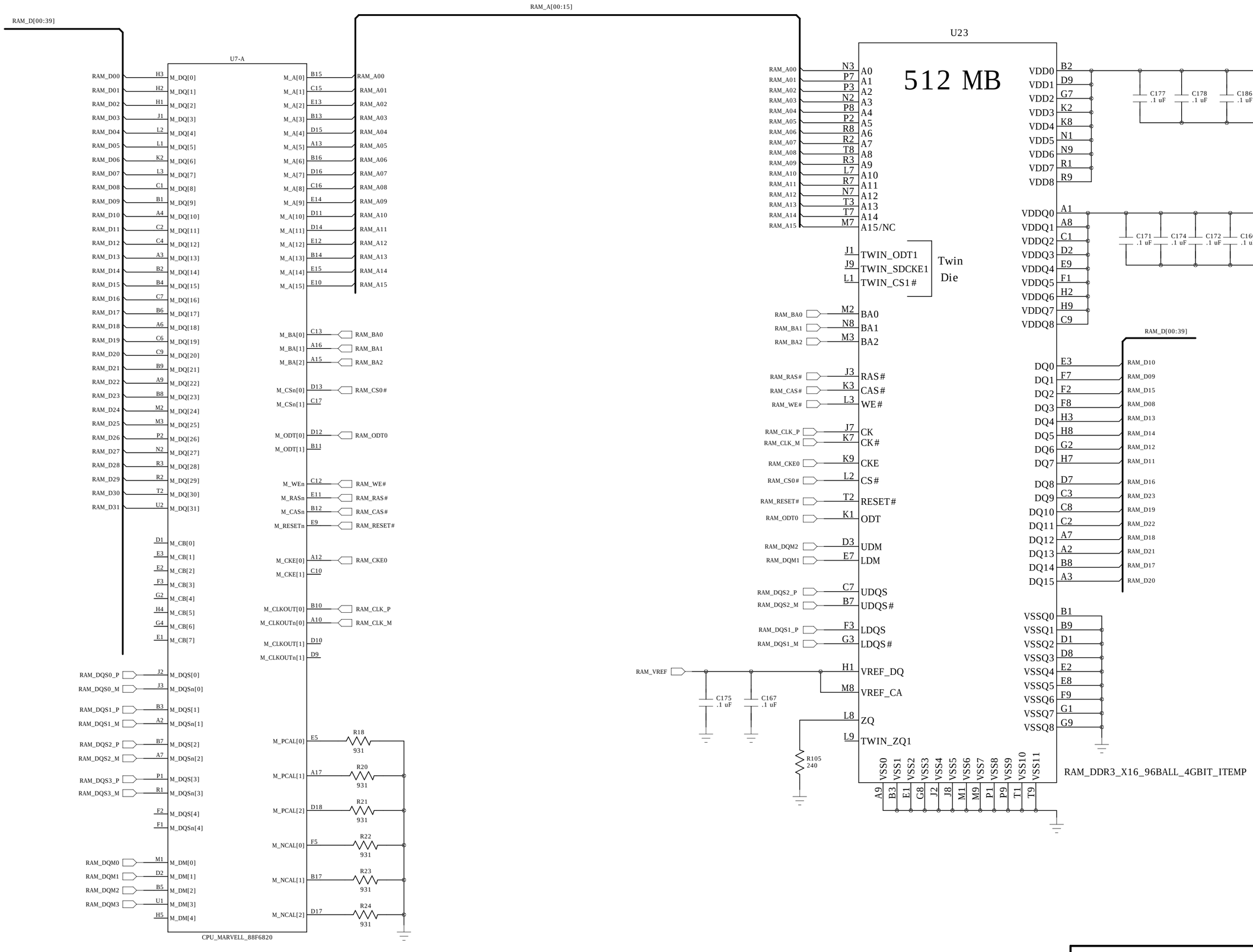
3) TS-781 8-28V Power daughter board

PEM Mounts for CN44 can not be populated if TS-781 used.

4) Heat sink on CPU

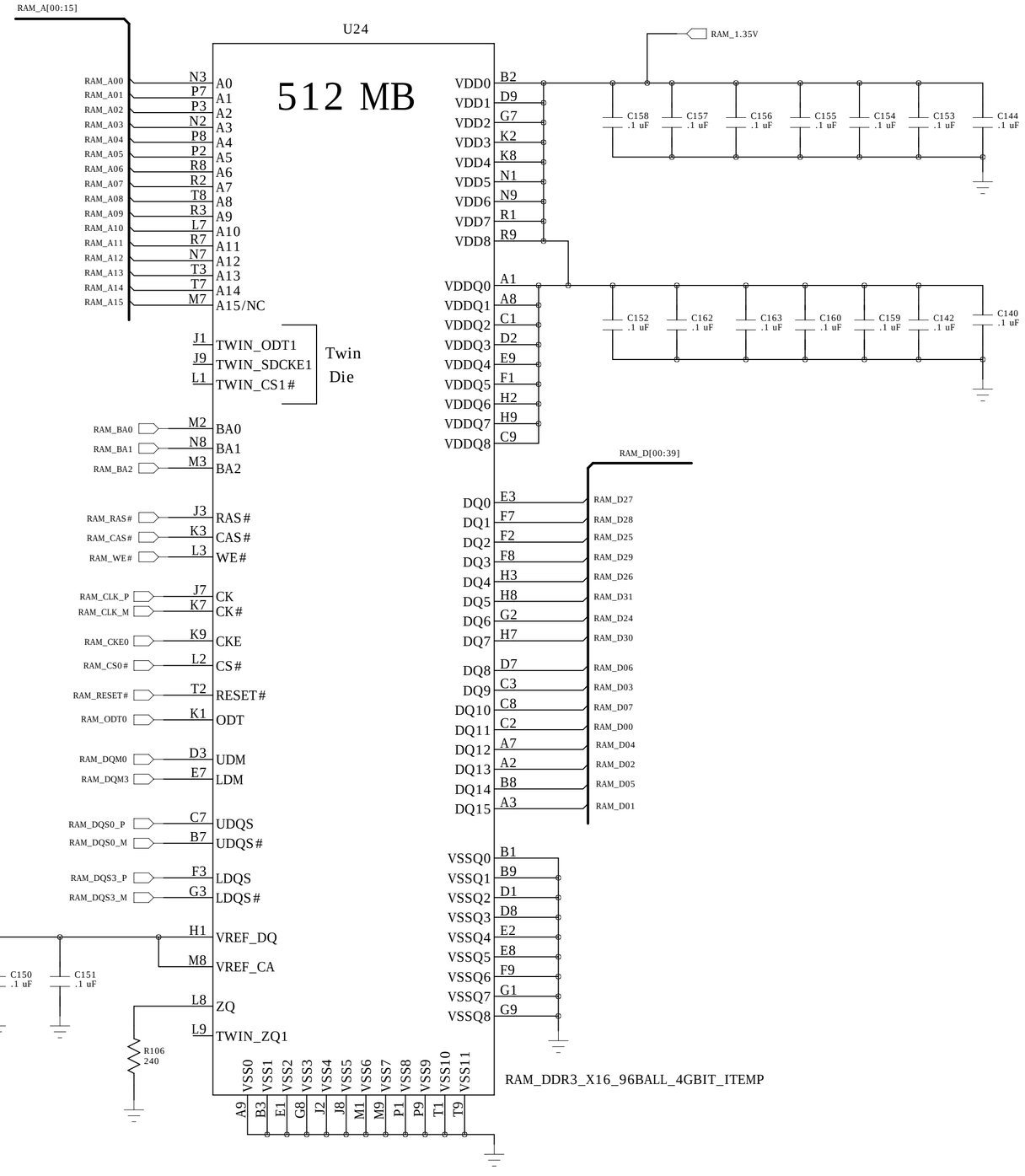
5) Accelerometer (U26)

DDR3 RAM



Technologic Systems		Date Jan. 30, 2017
Title: TS-7800-V2 CPU DDR		
Rev: P1	Designer	Sheet 3 of 26

DDR3 RAM



Technologic Systems		Date Jan. 30, 2017
Title: TS-7800-V2		
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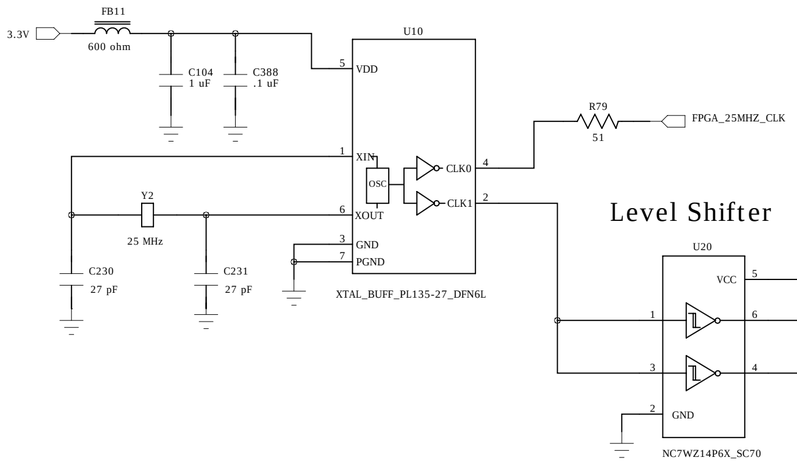
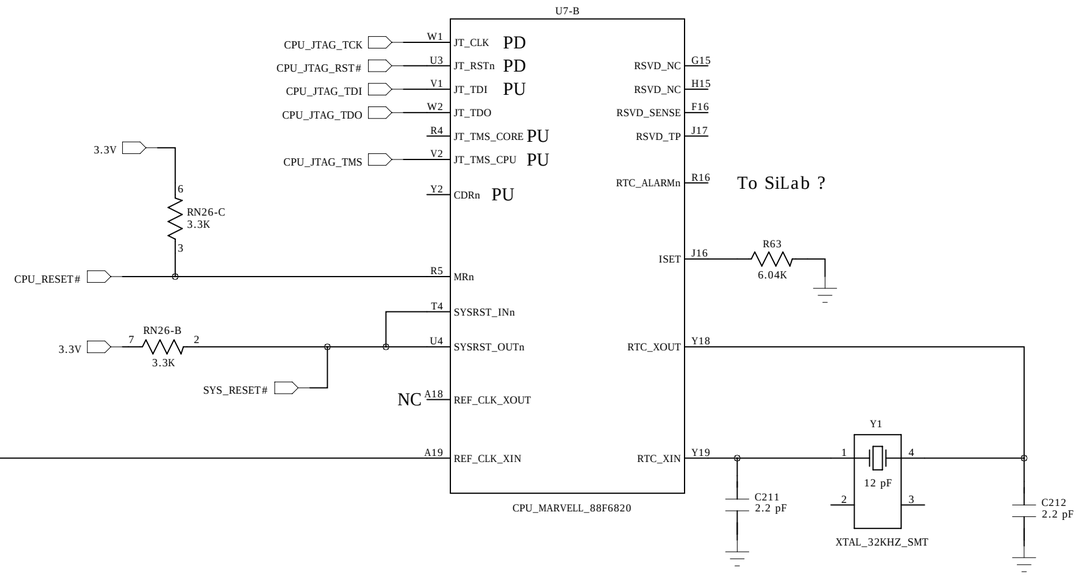
25 MHz Osc.

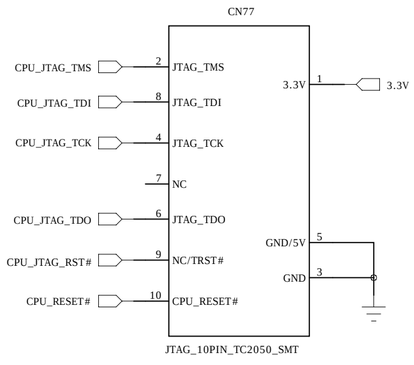


Level Shifter

CPU

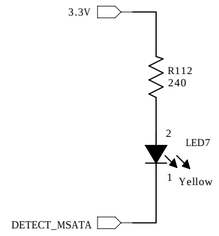


CPU JTAG

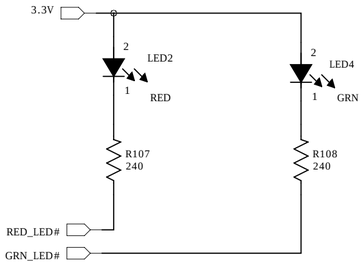


Tag-Connect

Boot Progress



CPU LEDs



Technologic Systems		Date Jan. 30, 2017
Title: TS-7800-V2 CPU Misc		
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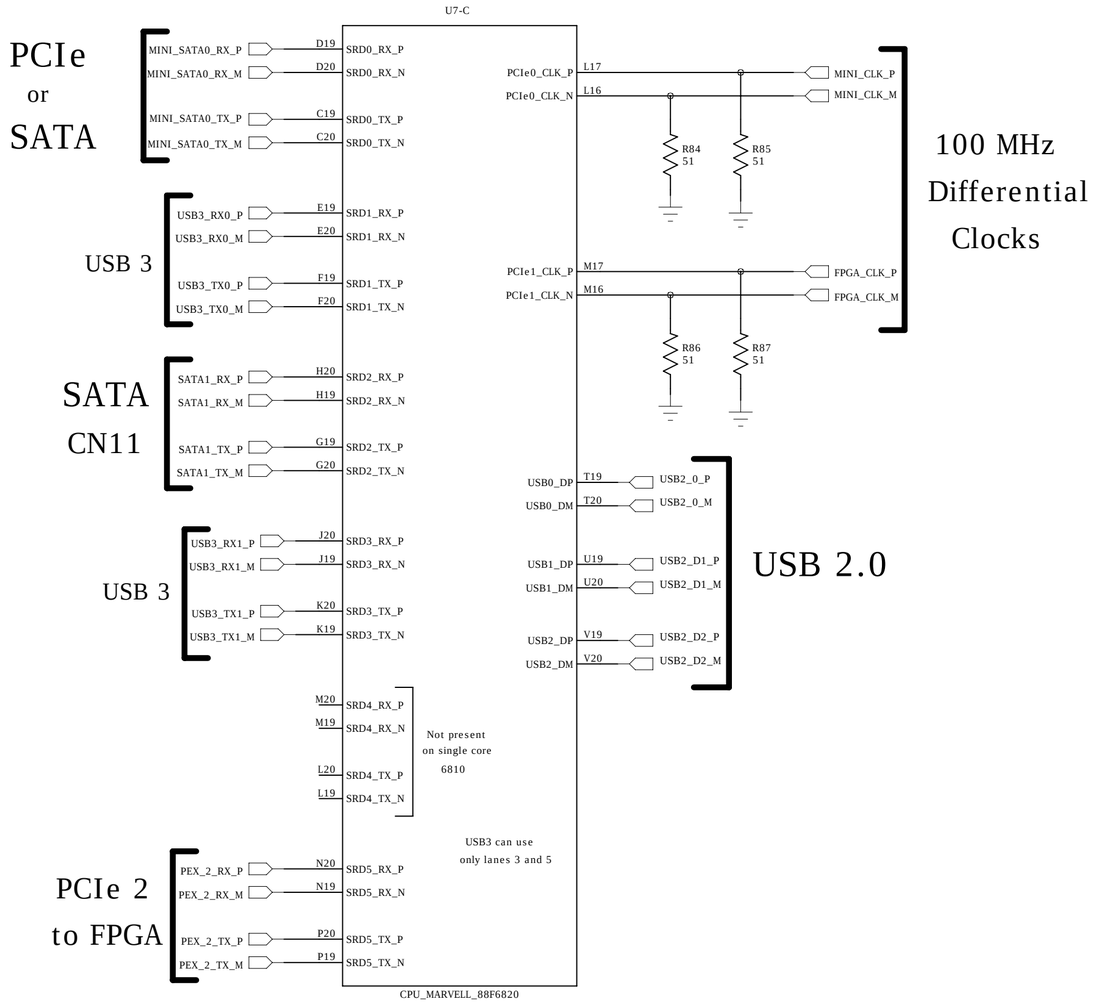
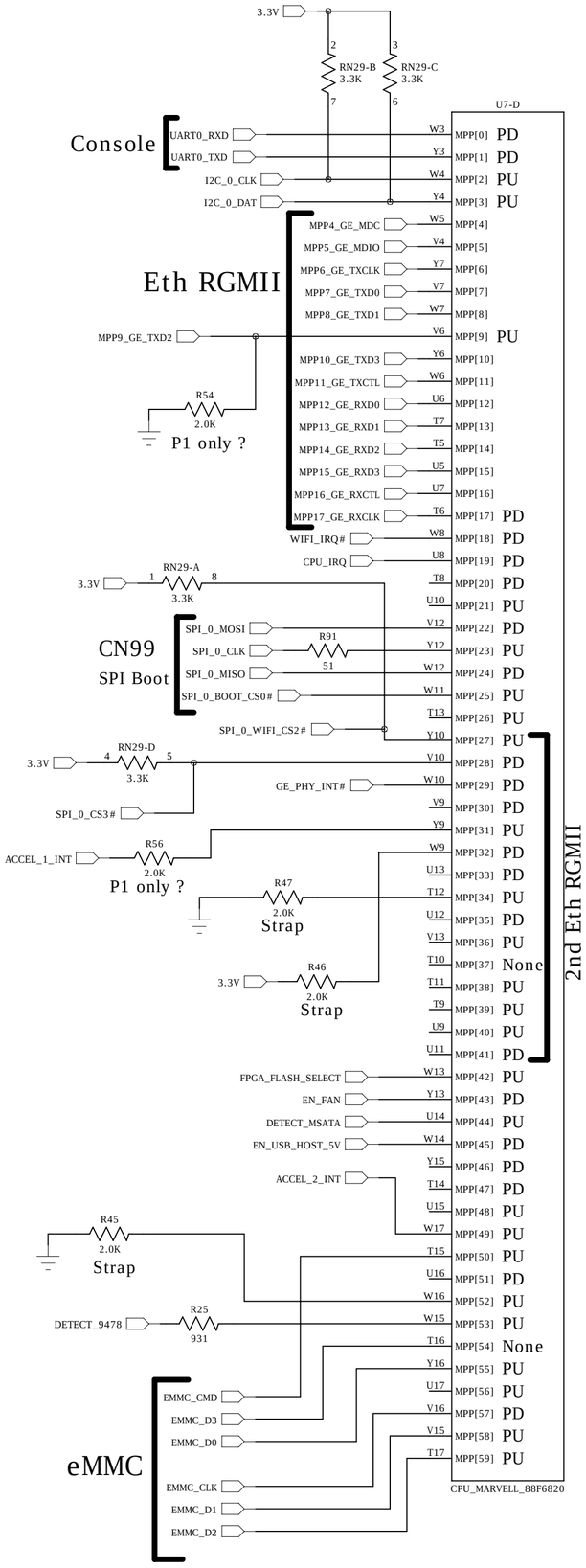
CPU SERDES



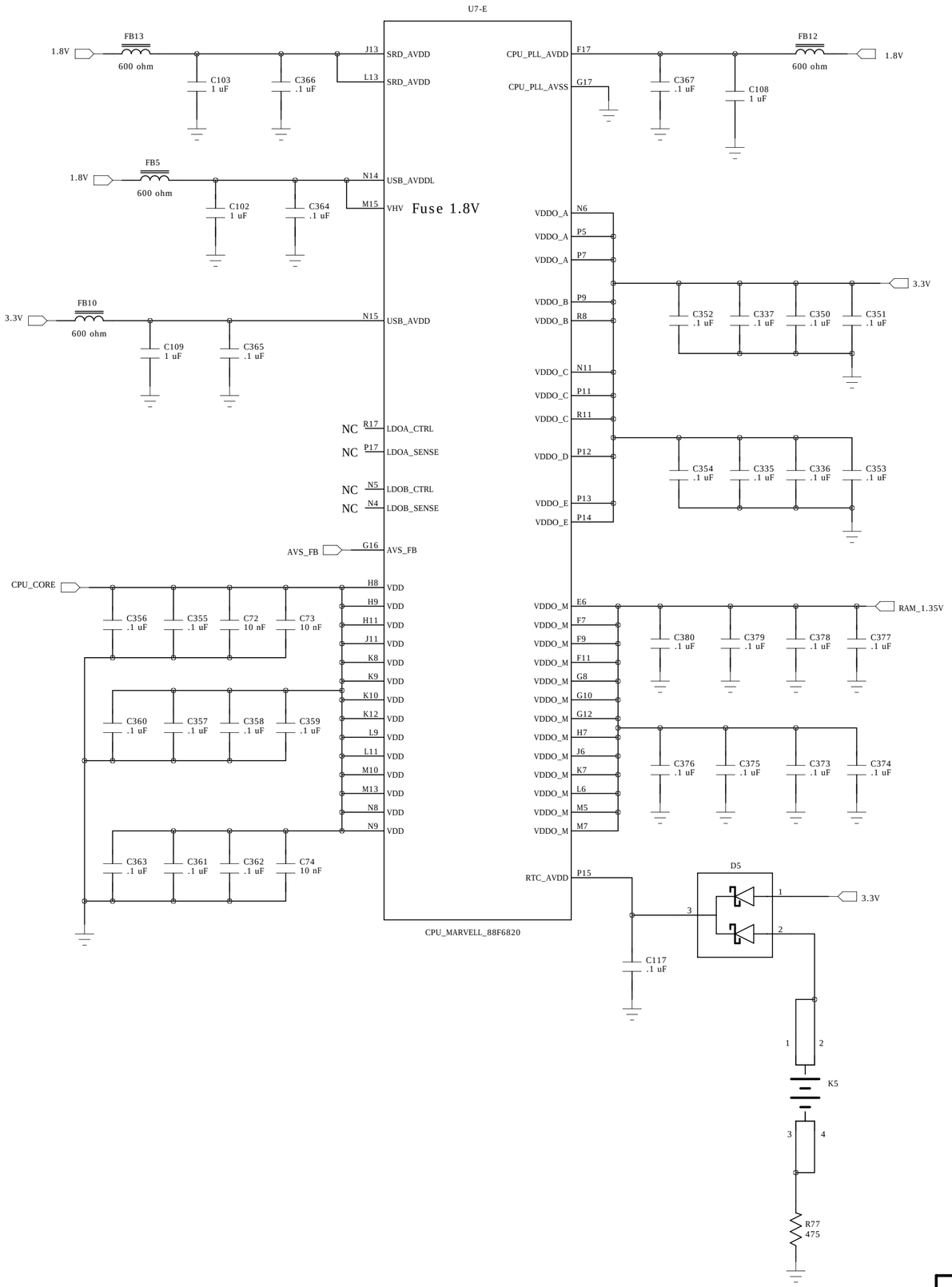
Technologic Systems	Date	Jan. 30, 2017
Title: TS-7800-V2 CPU SerDes		
Rev: P1	Designer	Sheet 7 of 26

CPU DIO



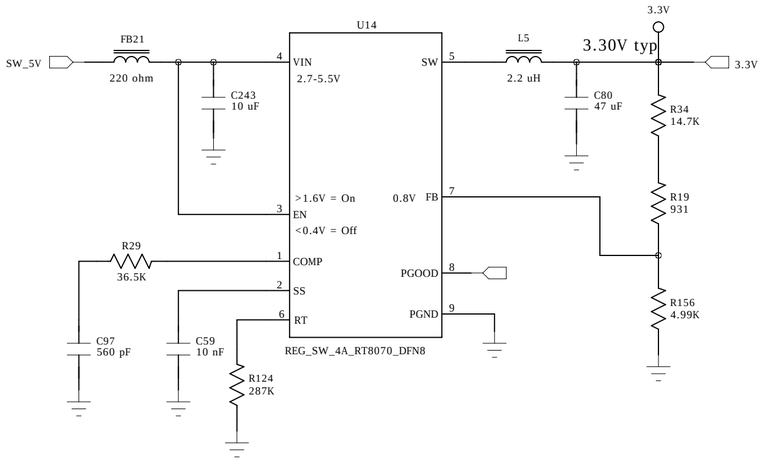
Technologic Systems	Date	Jan. 30, 2017
Title: TS-7800-V2 CPU I/O		
Rev: P1	Designer	Sheet 8 of 26

CPU

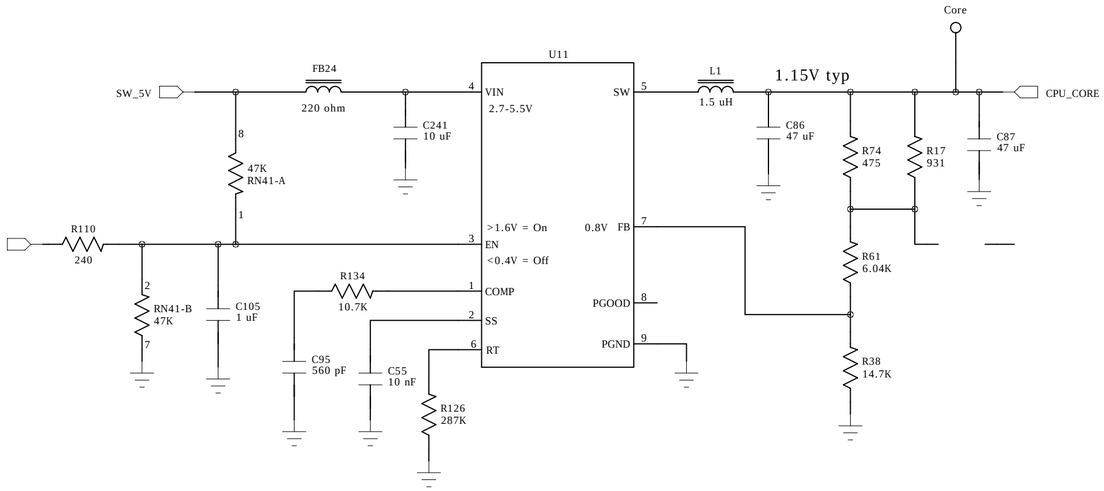


Technologic Systems		Date Jan. 30, 2017
Title: TS-7800-V2	CPU Power & Ground	
Rev: P1	Designer	Sheet 9 of 26

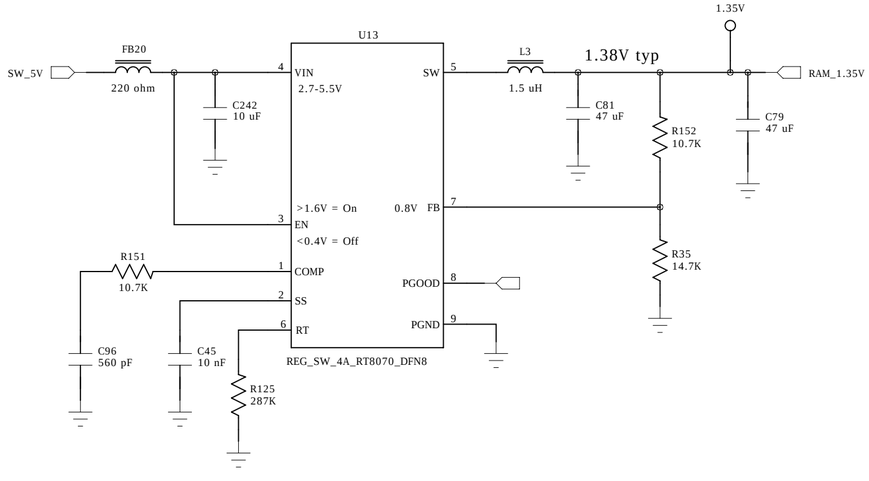
3.3V Reg.



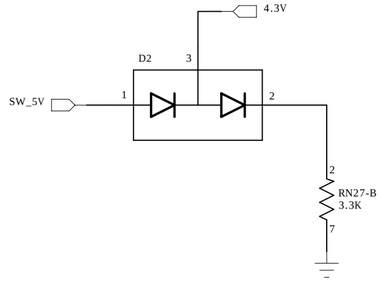
CPU Core Rail



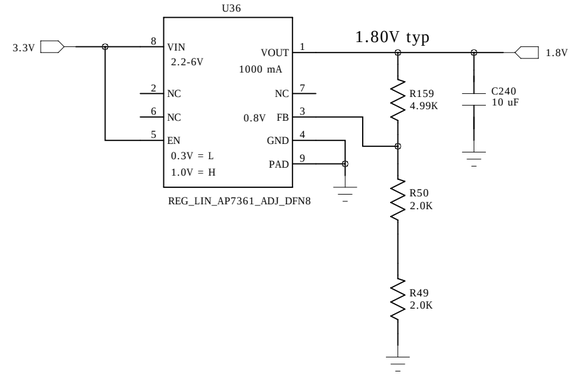
DDR3 1.35V Reg.



4.3V Rail



1.8V Reg.



Technologic Systems	Date Jan. 30, 2017	
Title: TS-7800-V2		
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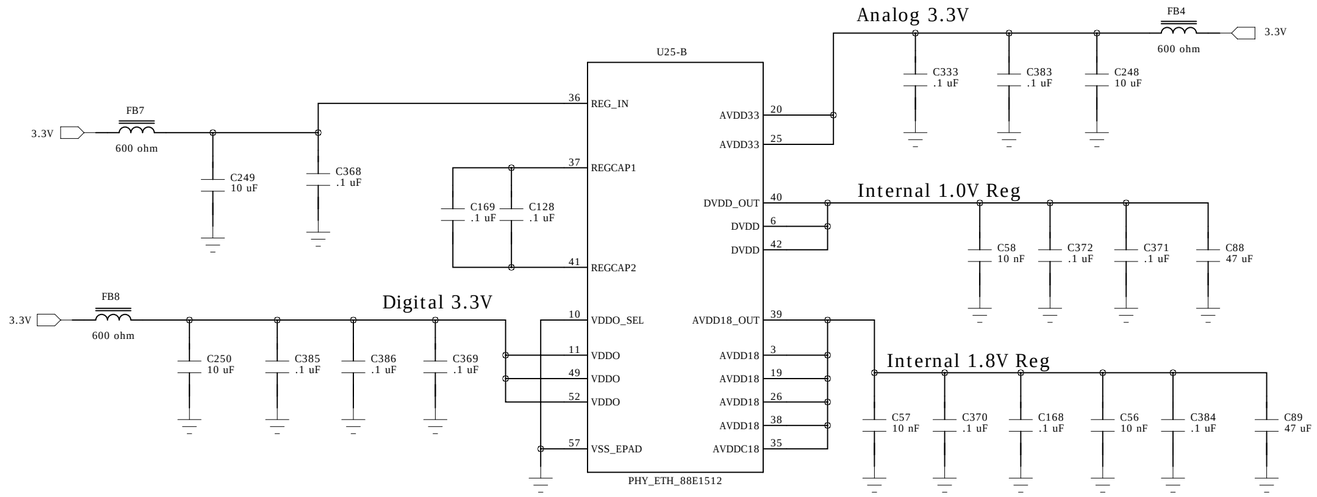
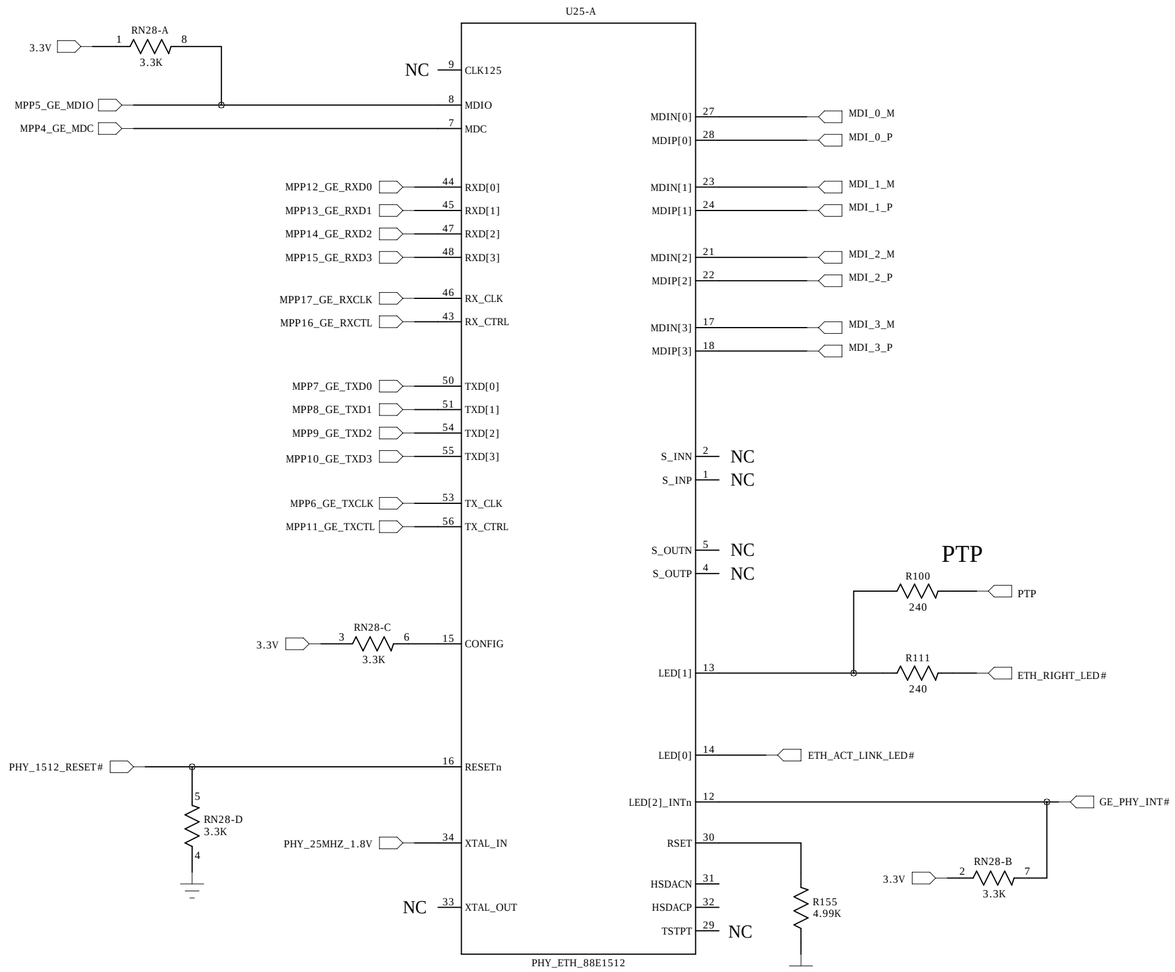
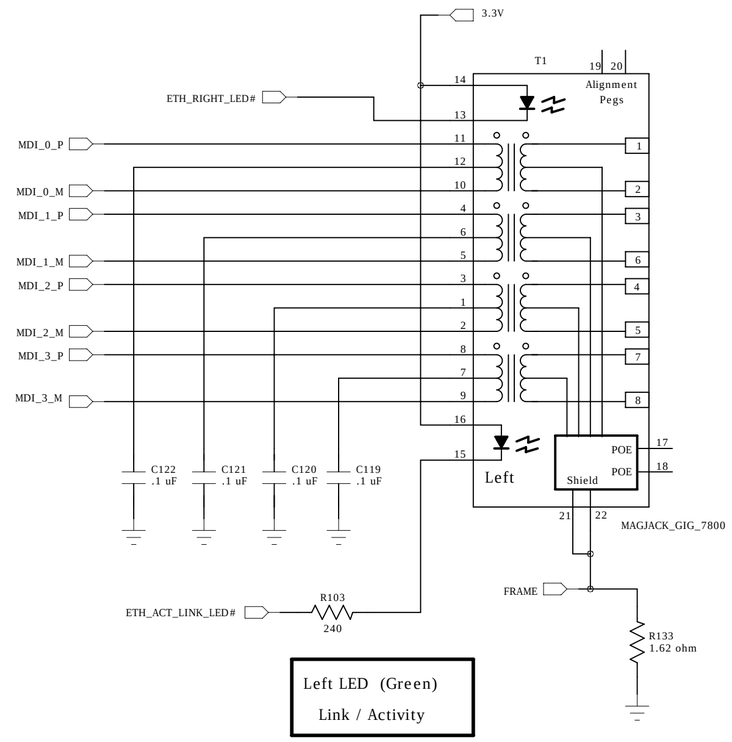
10/100/1000 Marvell 88E1512 PHY





Strapped for PHY
address = 1

Gig MagJack



Left LED (Green)
Link / Activity

Technologic Systems		Date Jan. 30, 2017
Title: TS-7800-V2	Ethernet PHY	
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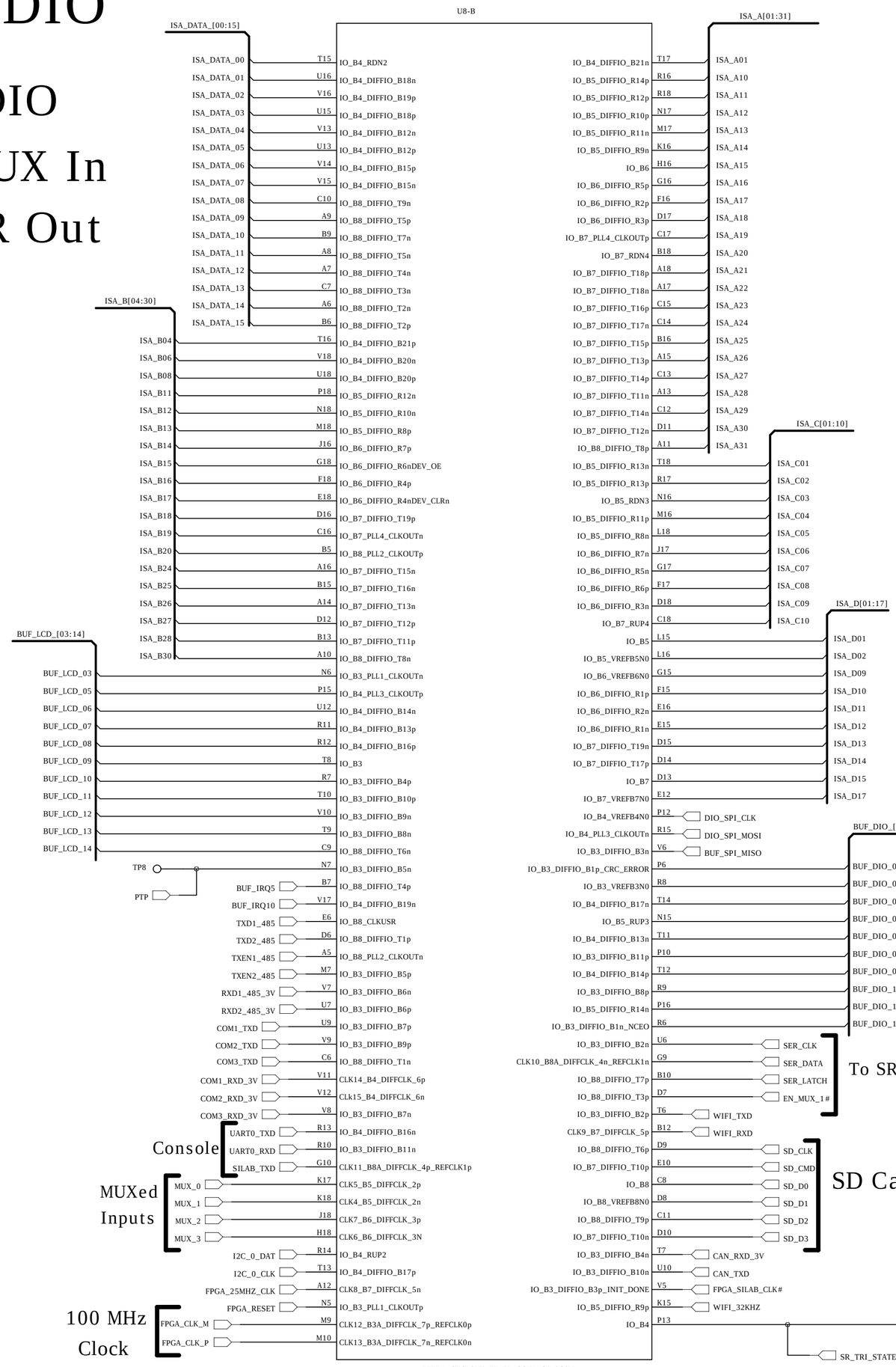
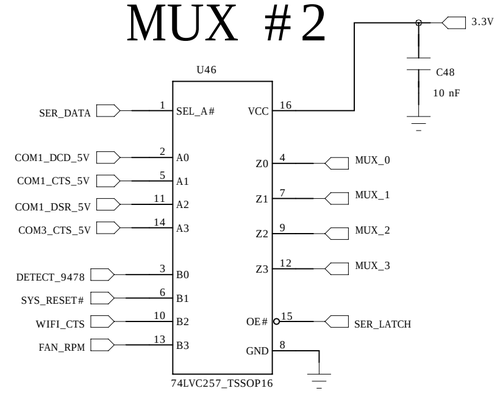
FPGA DIO

145 DIO
+ 16 MUX In
+ 16 SR Out

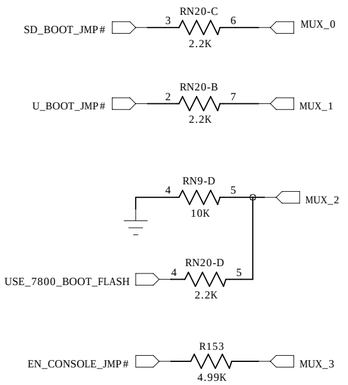


MUX #2

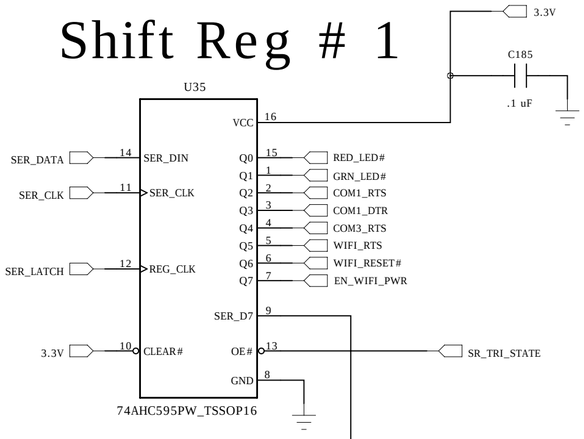


Provides 5V Tolerance

MUX Bias

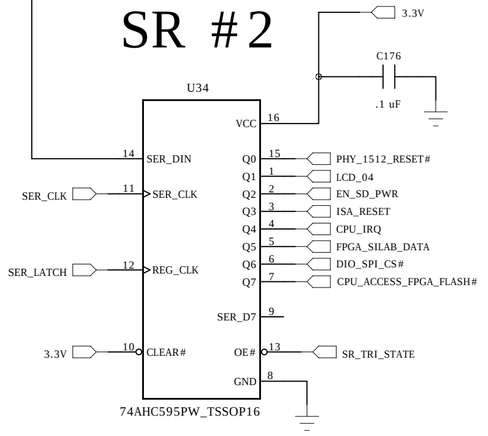


Shift Reg # 1



Shift Reg + Latch

SR #2



Shift Reg + Latch

Technologic Systems	Date Jan. 30, 2017	
Title: TS-7800-V2		
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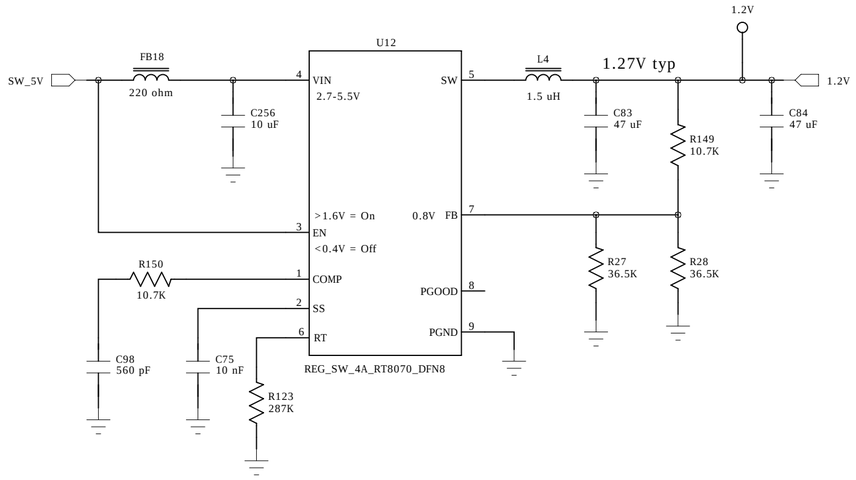
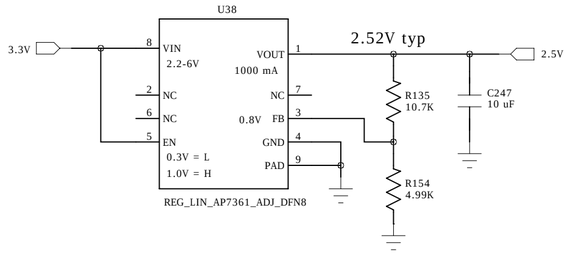
FPGA Stuff

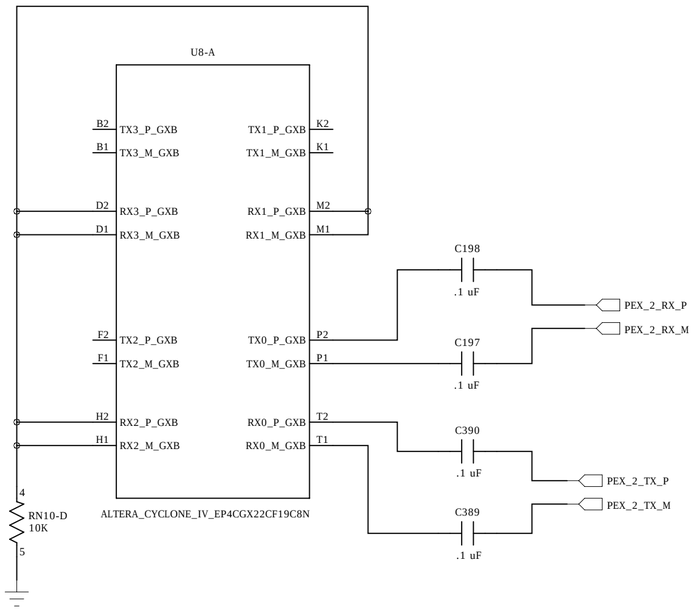
FGPA Core 1.2V Reg.



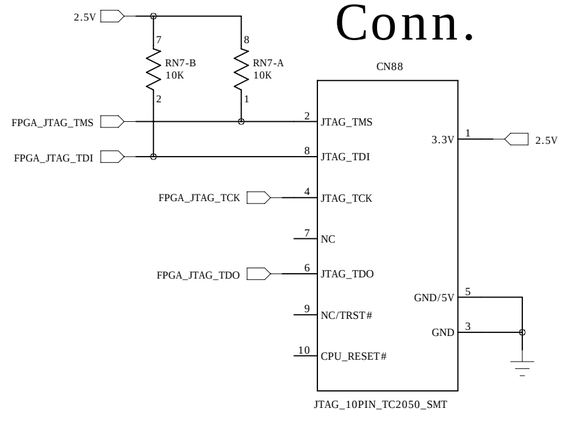
FPGA 2.5V Reg.



Cyclone Transceivers



FPGA JTAG Conn.



Tag-Connect

MSEL and JTAG must use 2.5V power

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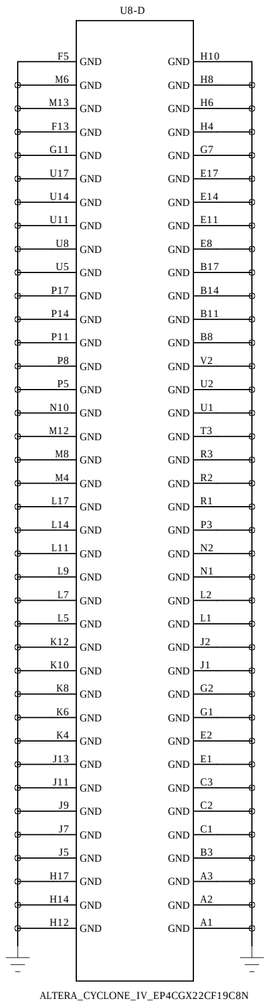
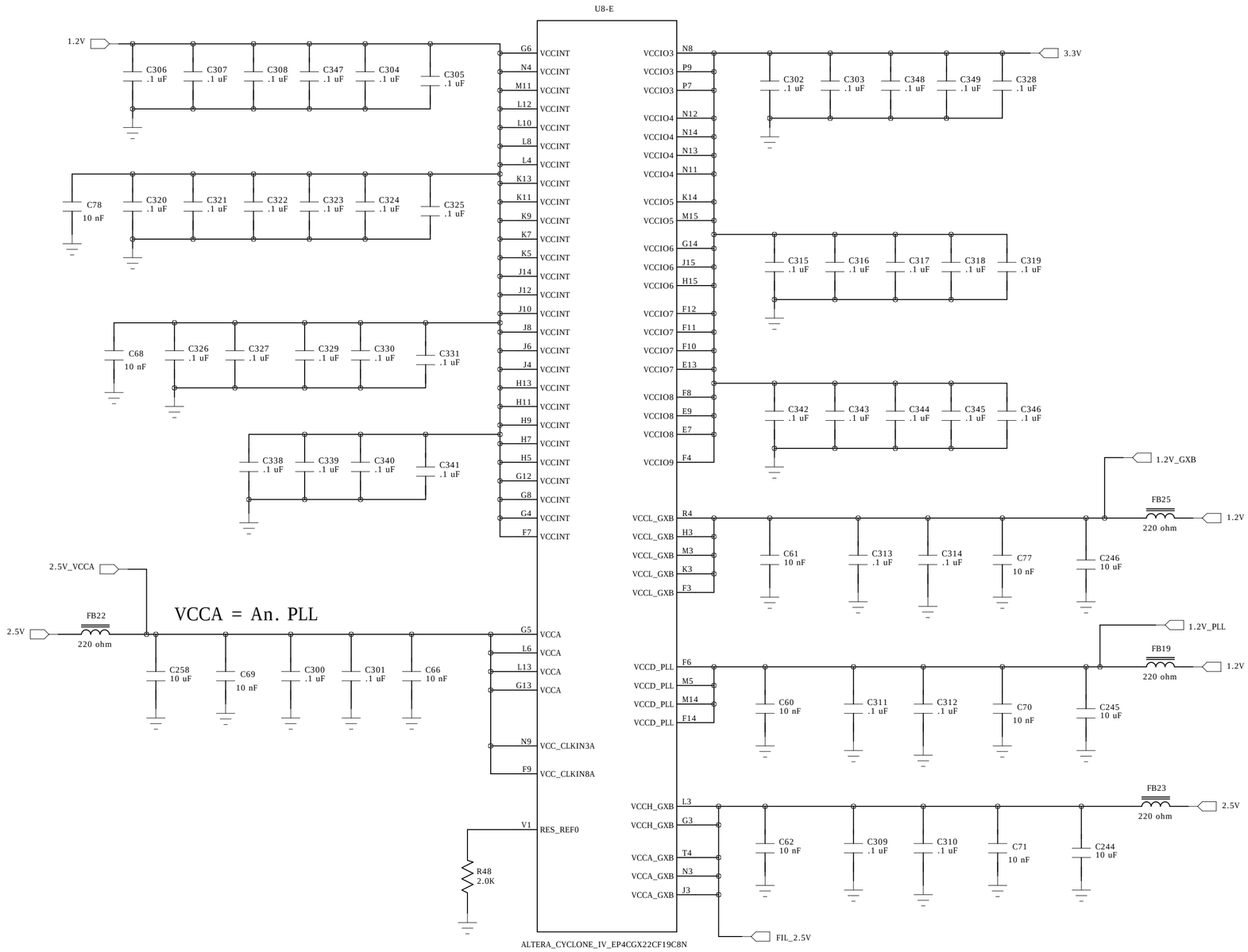
FPGA GND



FPGA Power



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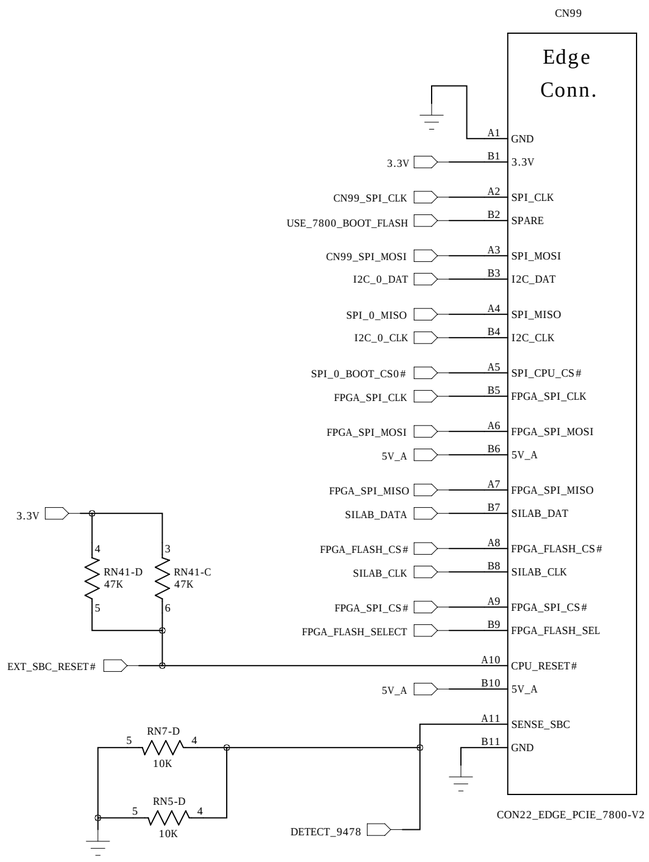
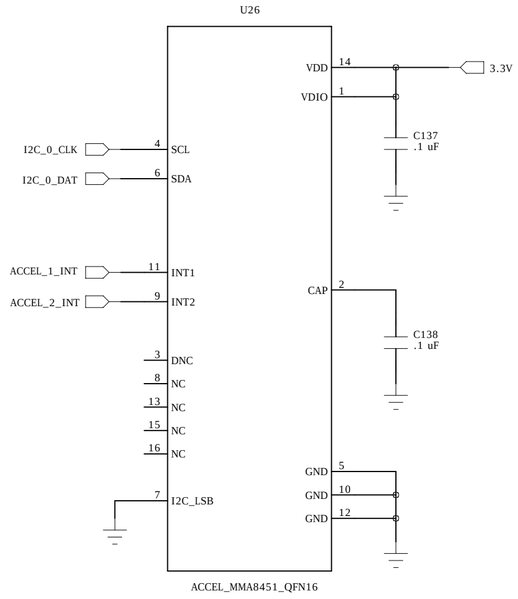
CN99
Edge Conn.



For Factory Programing boards use CN99 SPI Flash for both CPU Boot, and FPGA load

Accelerometer



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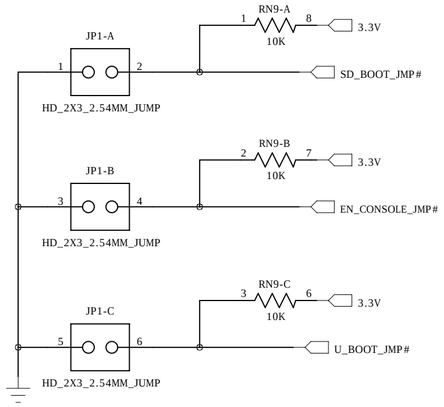
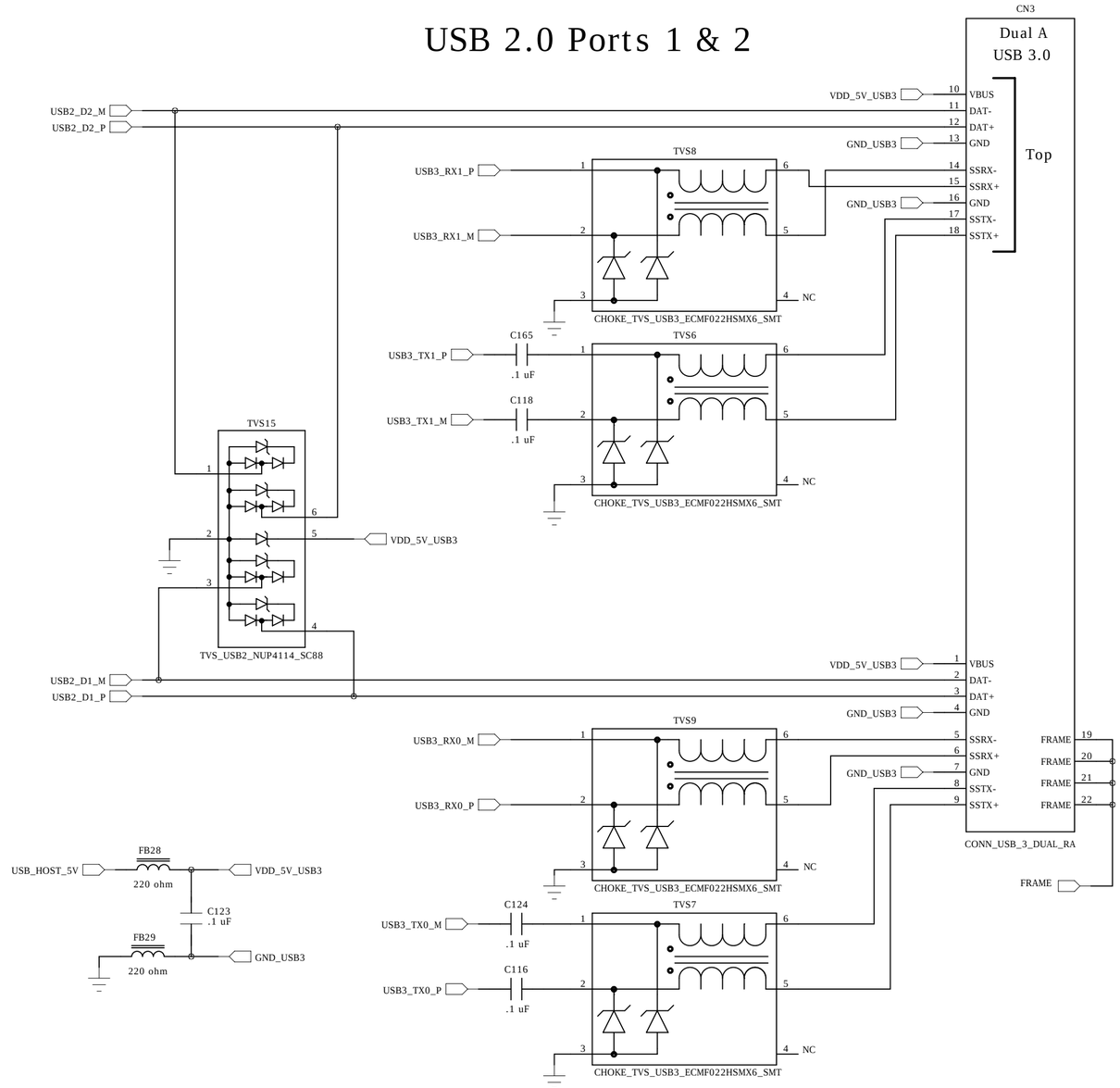
Jumpers



Dual Host USB 3.0

USB 3.0 Ports 0 & 1

USB 2.0 Ports 1 & 2



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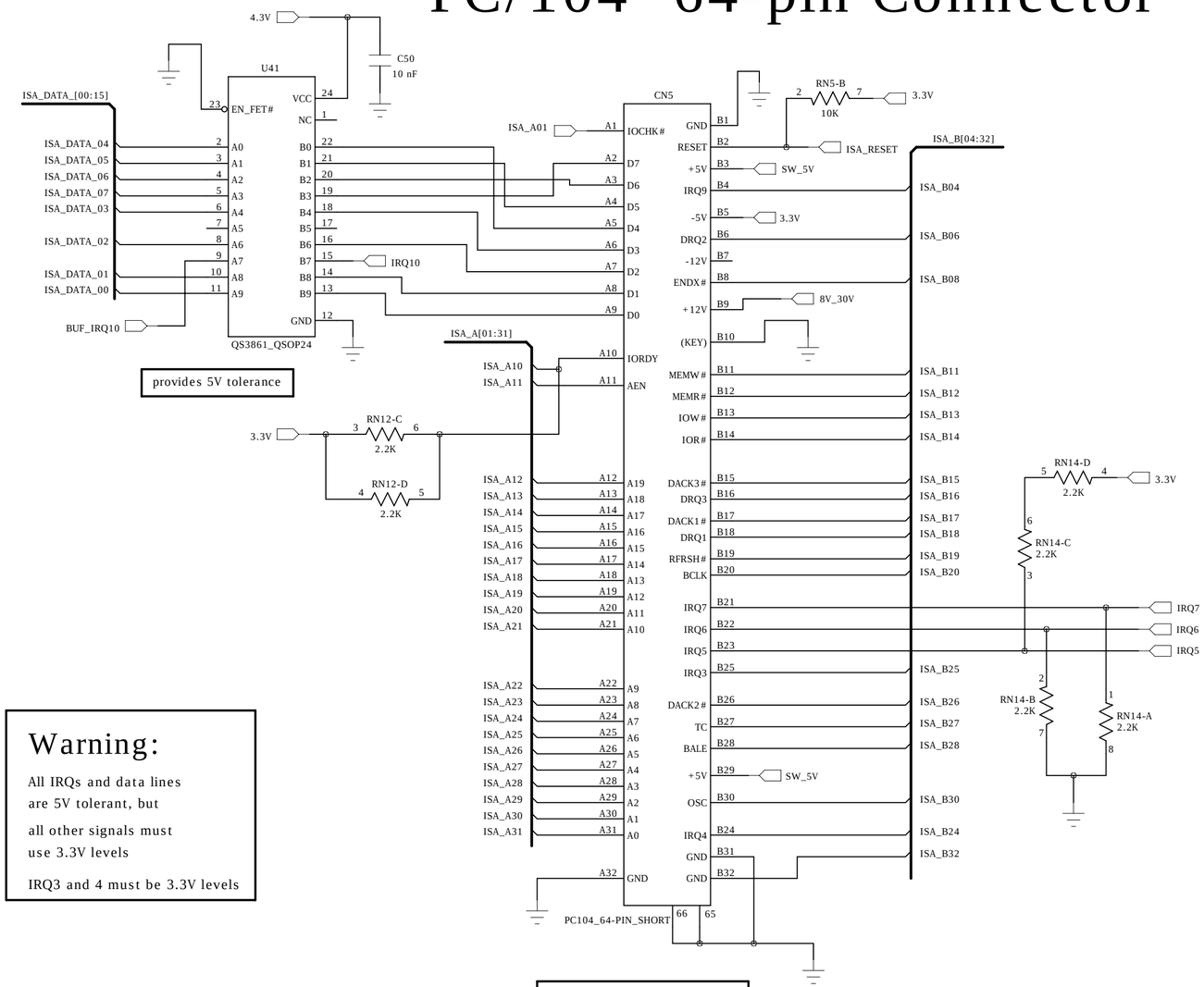
PC/104 64-pin Connector



Warning:

All IRQs and data lines are 5V tolerant, but

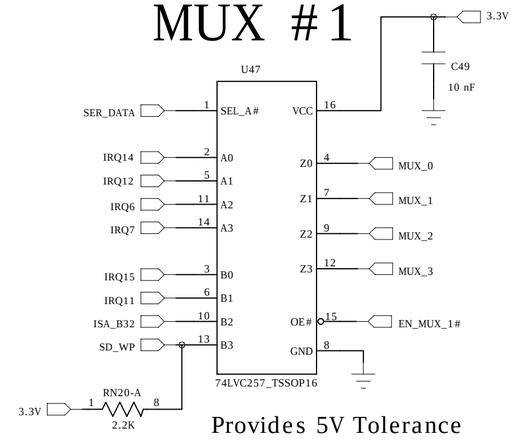
all other signals must use 3.3V levels

IRQ3 and 4 must be 3.3V levels

50 lines directly into FPGA
plus 3 more read only:
(IRQ6, IRQ7 and ISA_32)

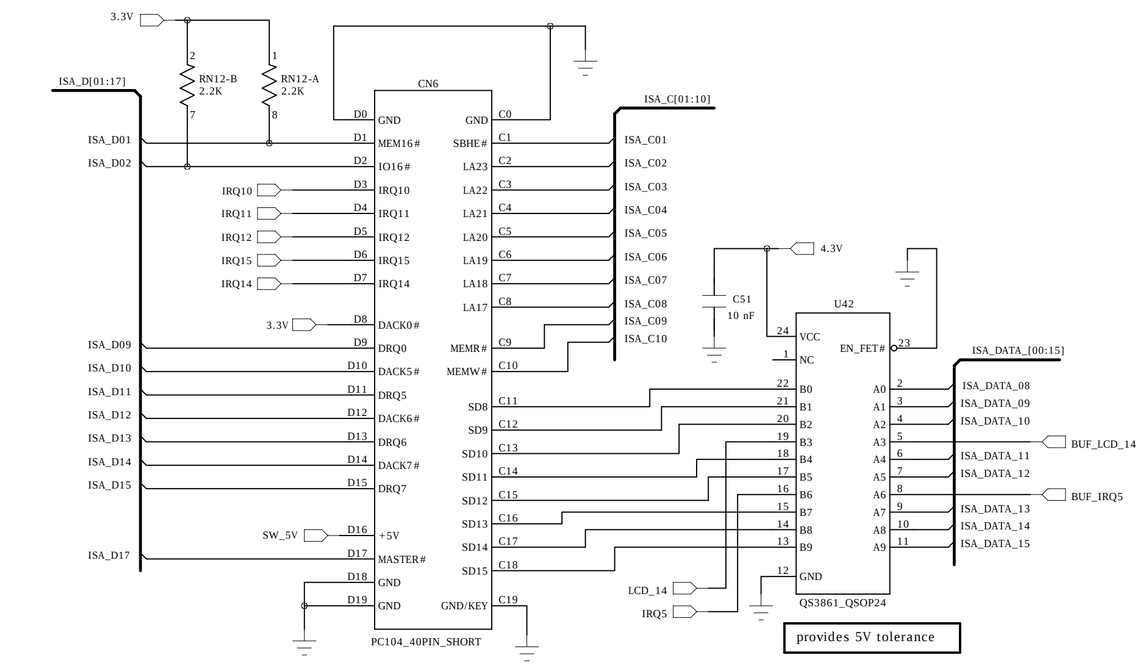
ISA_RESET is output only

MUX #1



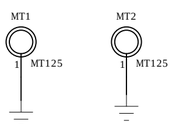
Provides 5V Tolerance

PC/104 40-pin Connector



29 lines directly into FPGA (bi-directional)

IRQ11 thru IRQ15 are read only



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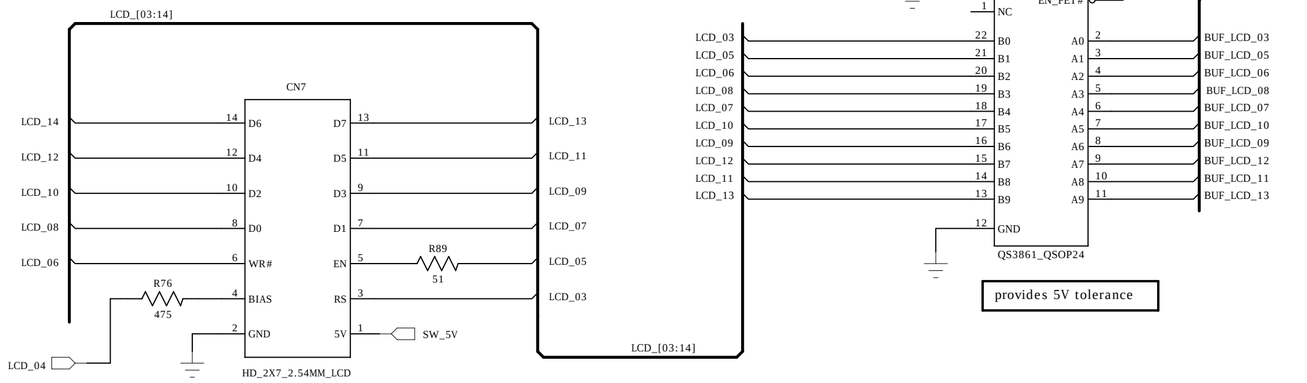
LCD Port



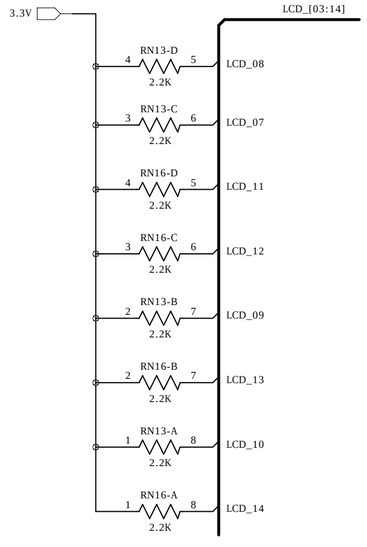
provides 5V tolerance

LCD03, LCD05, LCD06 init to inputs
when outputs, active high-low
These are programmable I/O

LCD07 thru LCD14 are always open
drain outputs, initialized to high
They can be used as inputs

All LCD lines are 5V tolerant

LCD04 is always output
active high-low, init to zero



Pull-up resistors for
the open drain outputs

Open drain outputs can
sink 8 mA, but only source
current thru resistor

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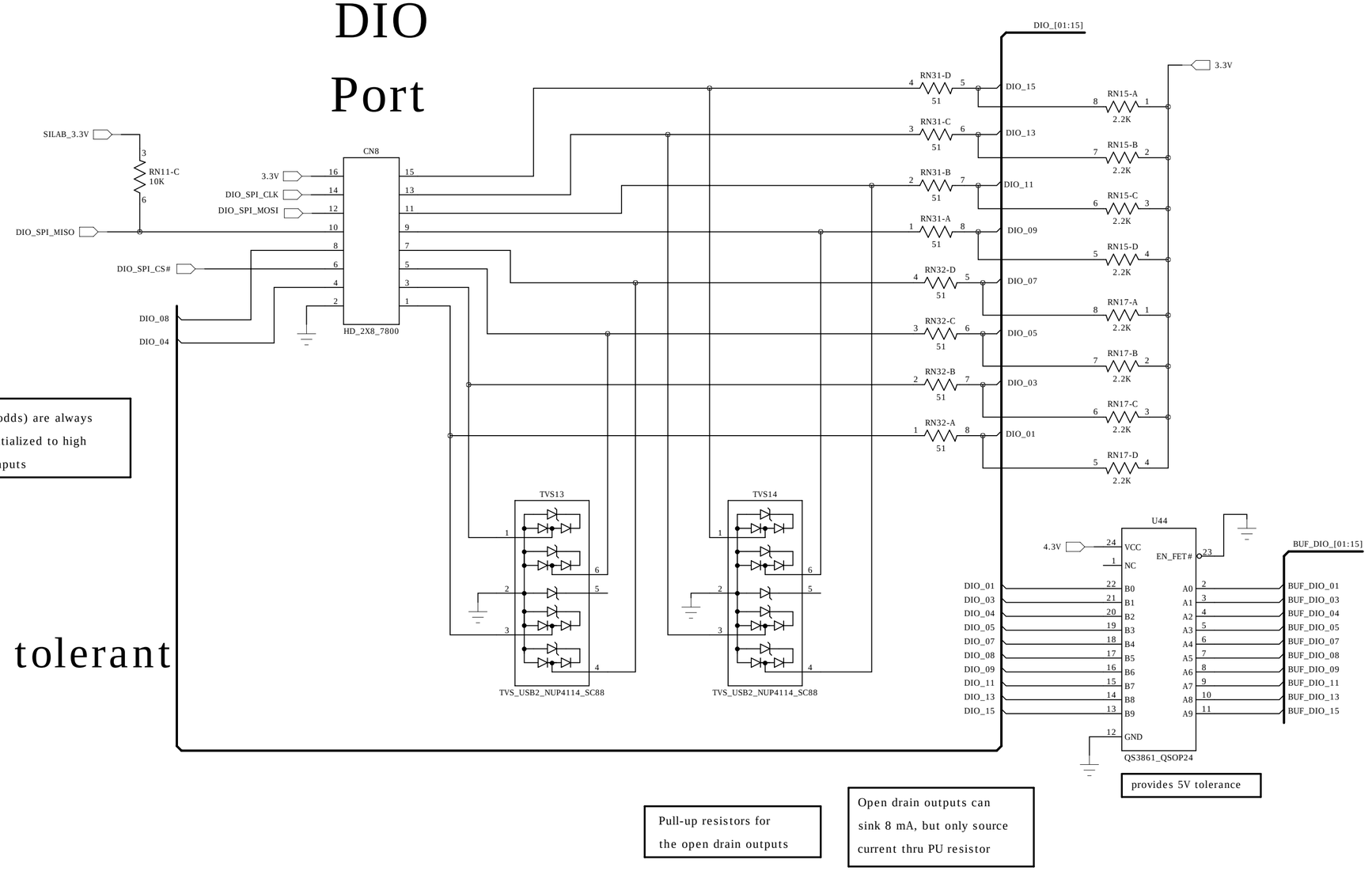
DIO Port



SPI_MISO is 5V tolerant
SPI_MOSI, CLK, and Frame
are 3.3V level outputs

DIO_01 thru DIO_15 (odds) are always
open drain outputs, initialized to high
They can be used as inputs

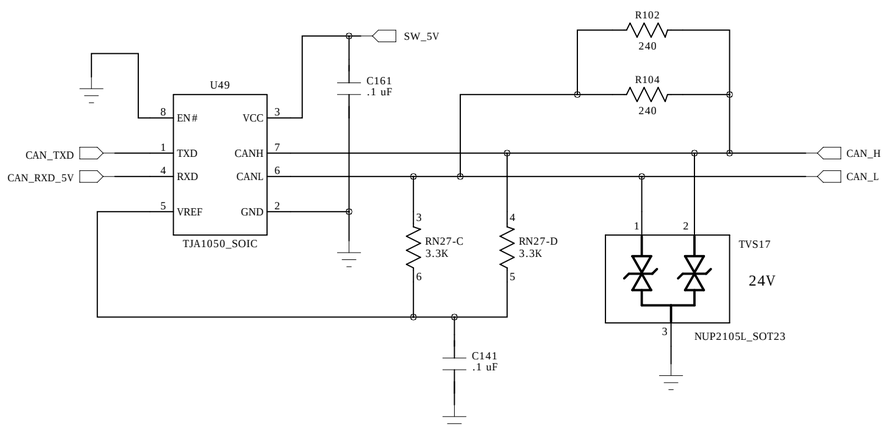
DIO_04 and DIO_08 initialize to inputs
when output, active high-low
They are programmable In or out

All DIO lines are 5V tolerant

Pull-up resistors for
the open drain outputs

Open drain outputs can
sink 8 mA, but only source
current thru PU resistor

CAN Transceiver



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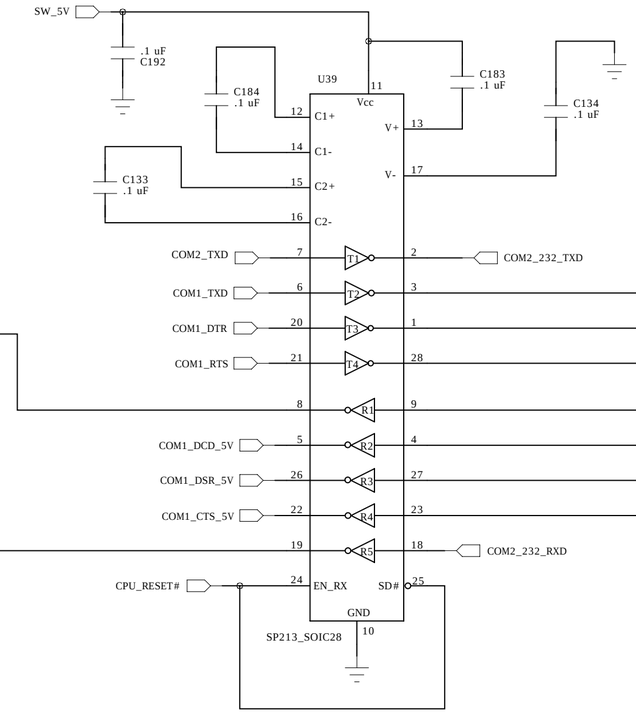
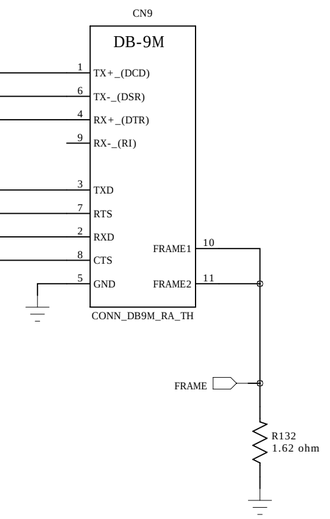
COM1

RS-232 Transceiver



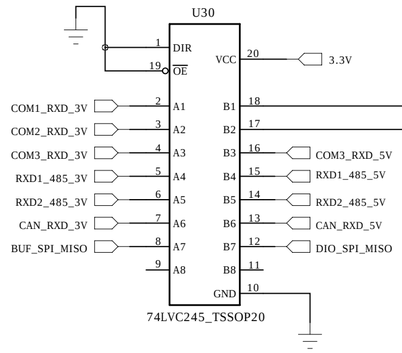
COM1

DB9M

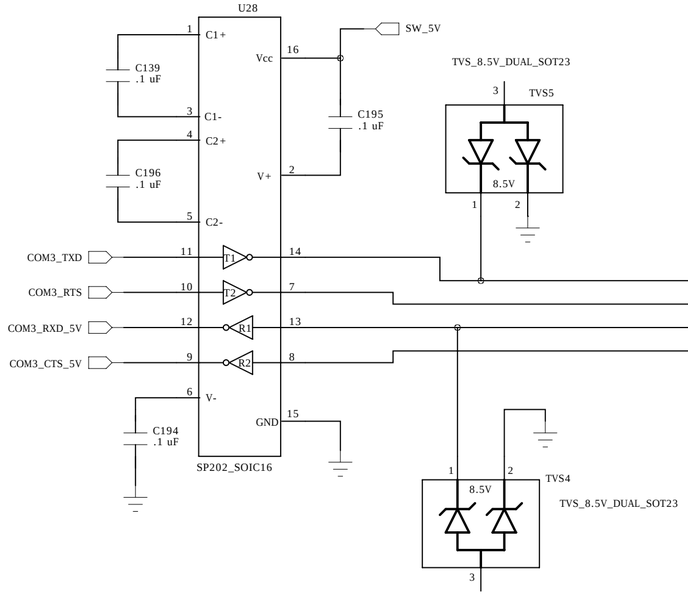


3.3V <-- 5V

Level shifter

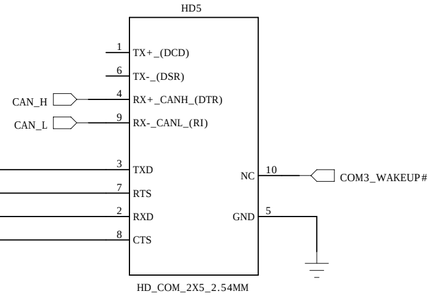


RS-232 Transceiver

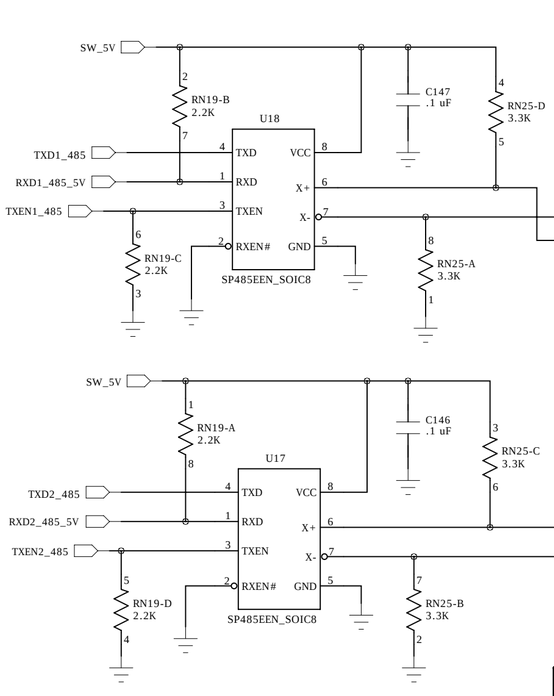


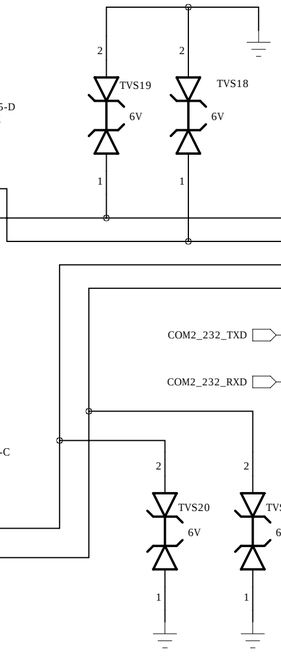
COM3

Header



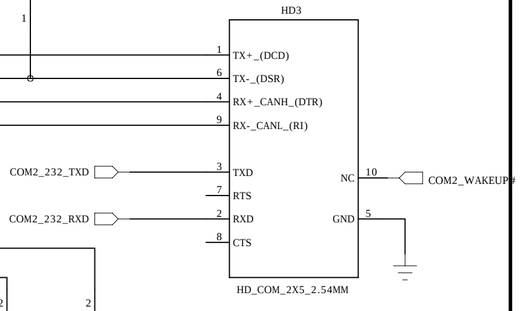
RS-485 Drivers





COM2

Header



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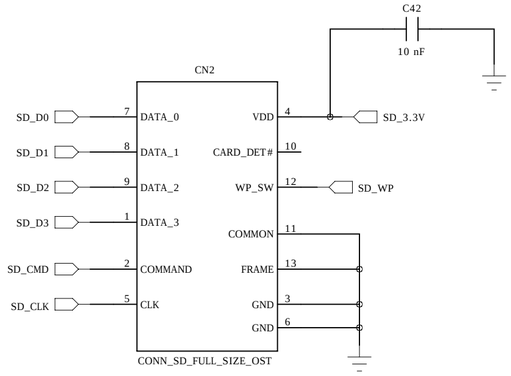
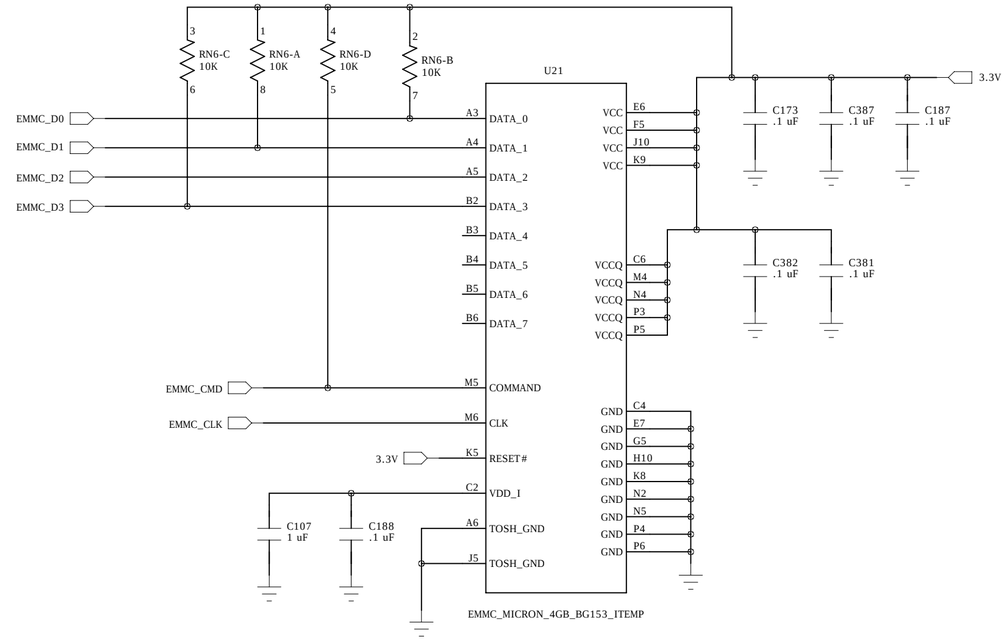
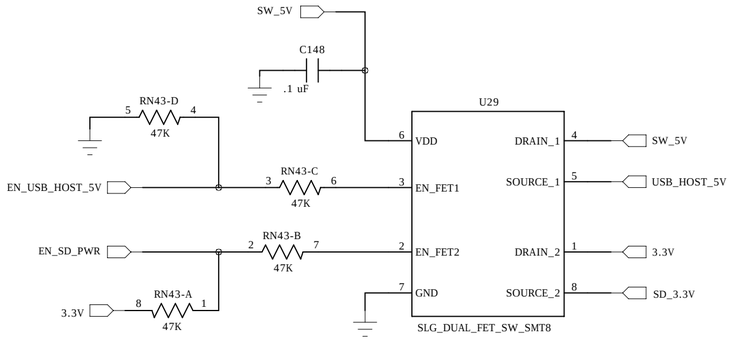
Full-Size SD Card Socket



eMMC 4GB
Optionally up to 64GB

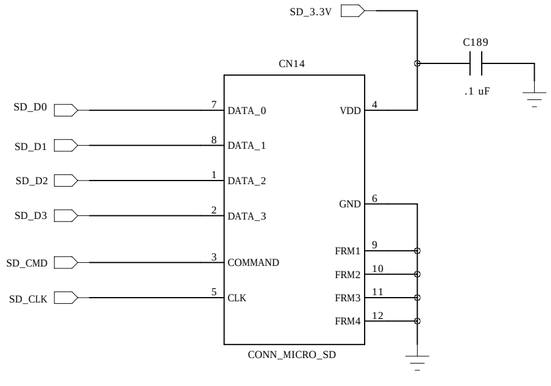


SD Card and USB Power Switch



Rise time of both outputs measured at ~1V/ms

Micro SD Card Socket



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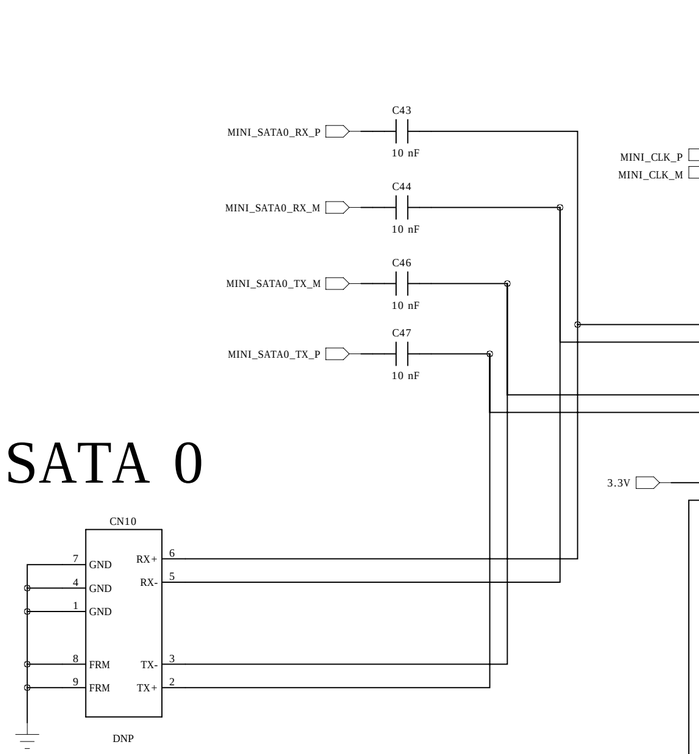
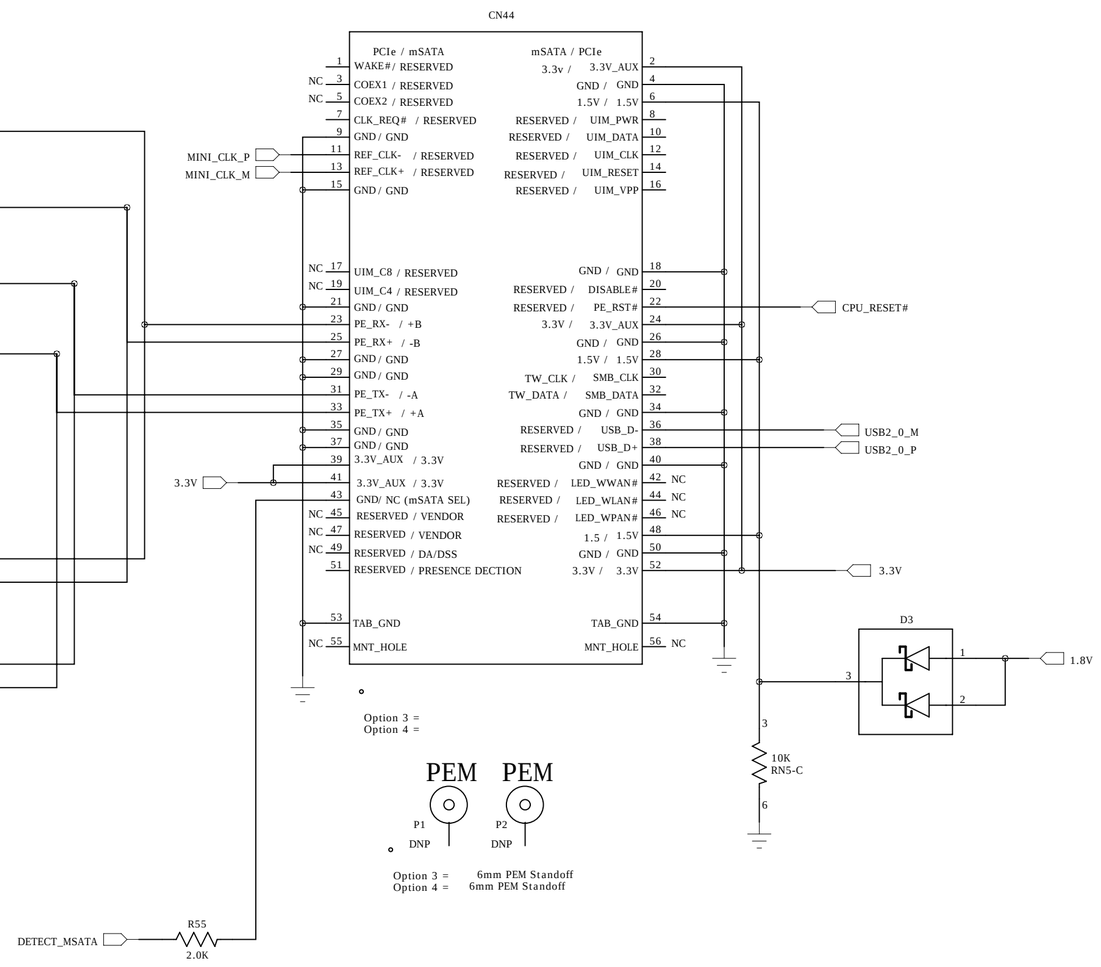
Mini-PCIe/mSATA

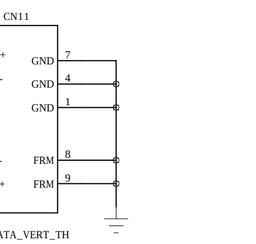
7mm Stack Height to center of bd.

SATA 0



Not pop when CN44 present





SATA 1

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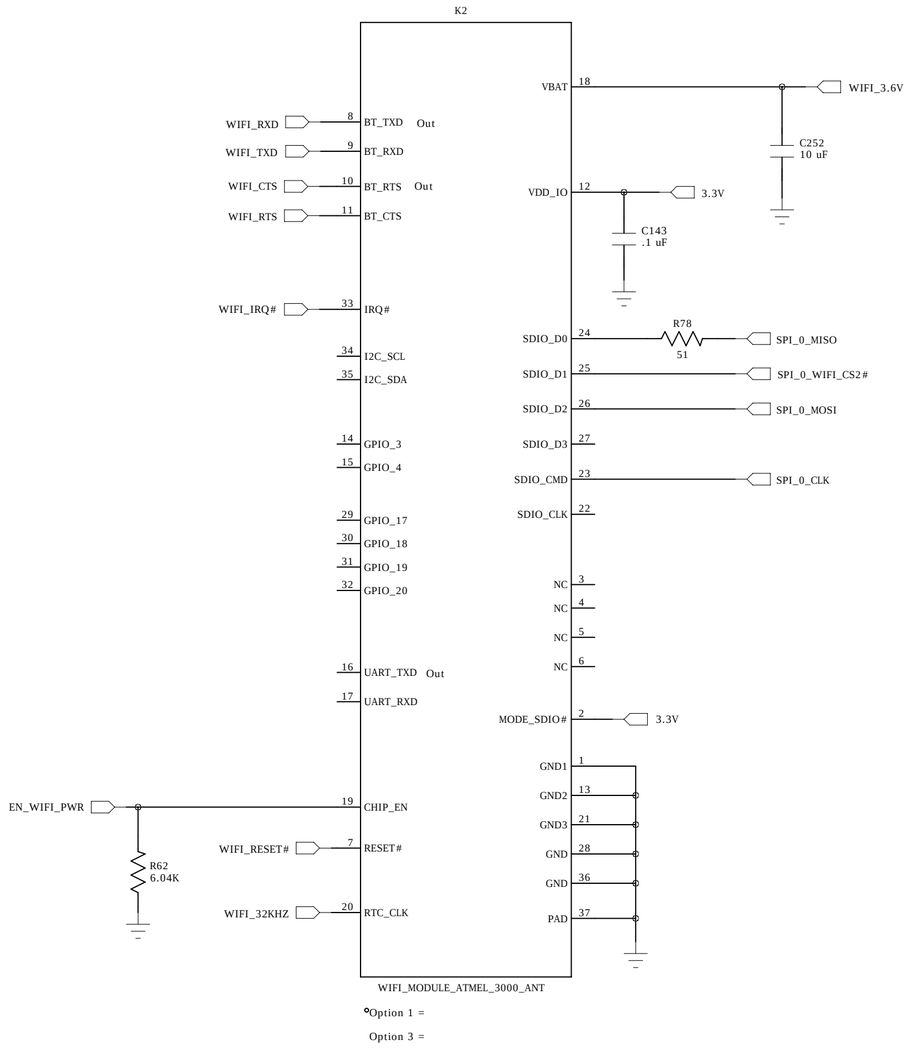
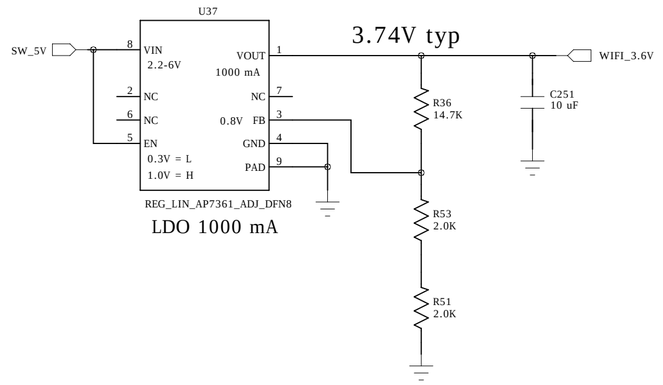
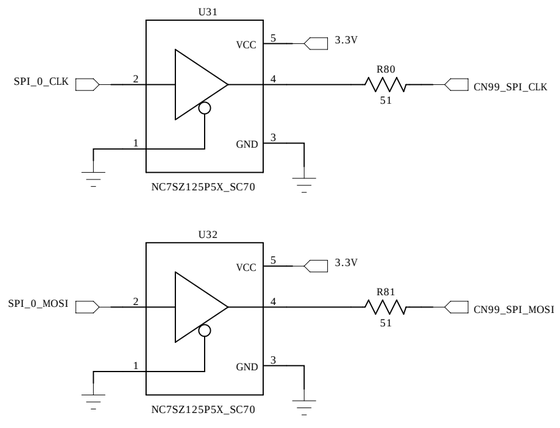
WiFi / Blutooth Radio Module



WiFi 3.6V Regulator



SPI Buffers



Place near WiFi radio

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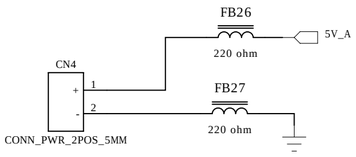
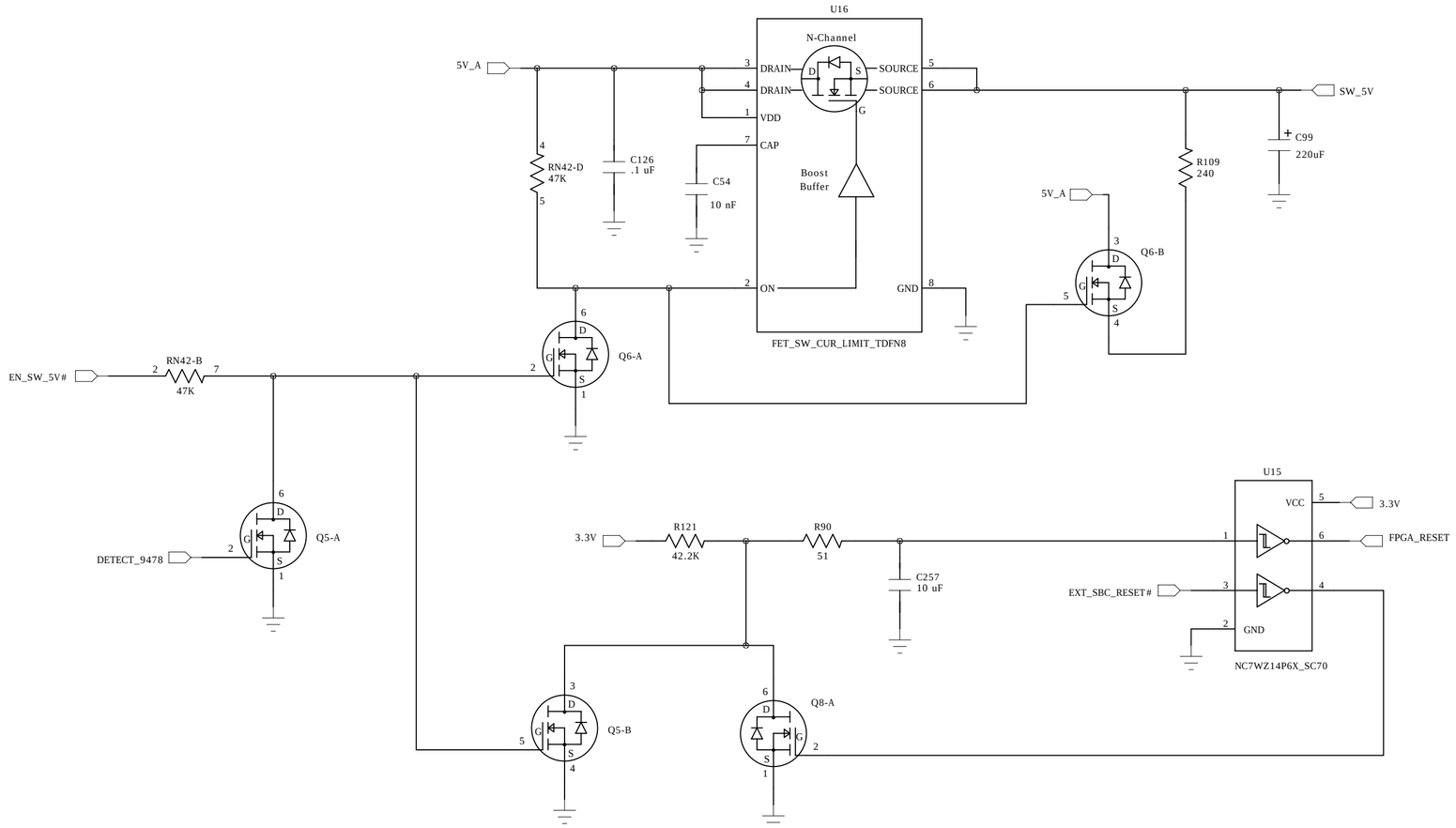
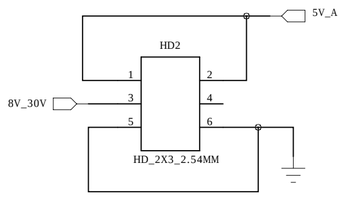
5V Power In



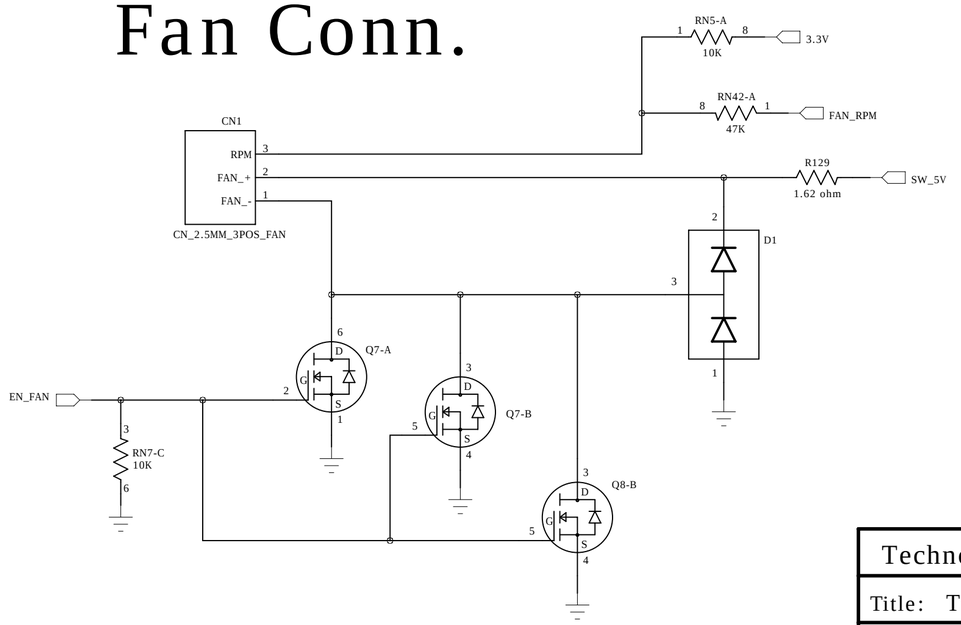
Main 5V Power Sw.



Interface to TS-781 Buck Reg.



Fan Conn.



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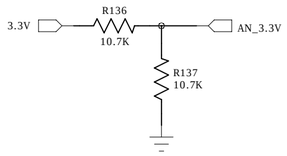
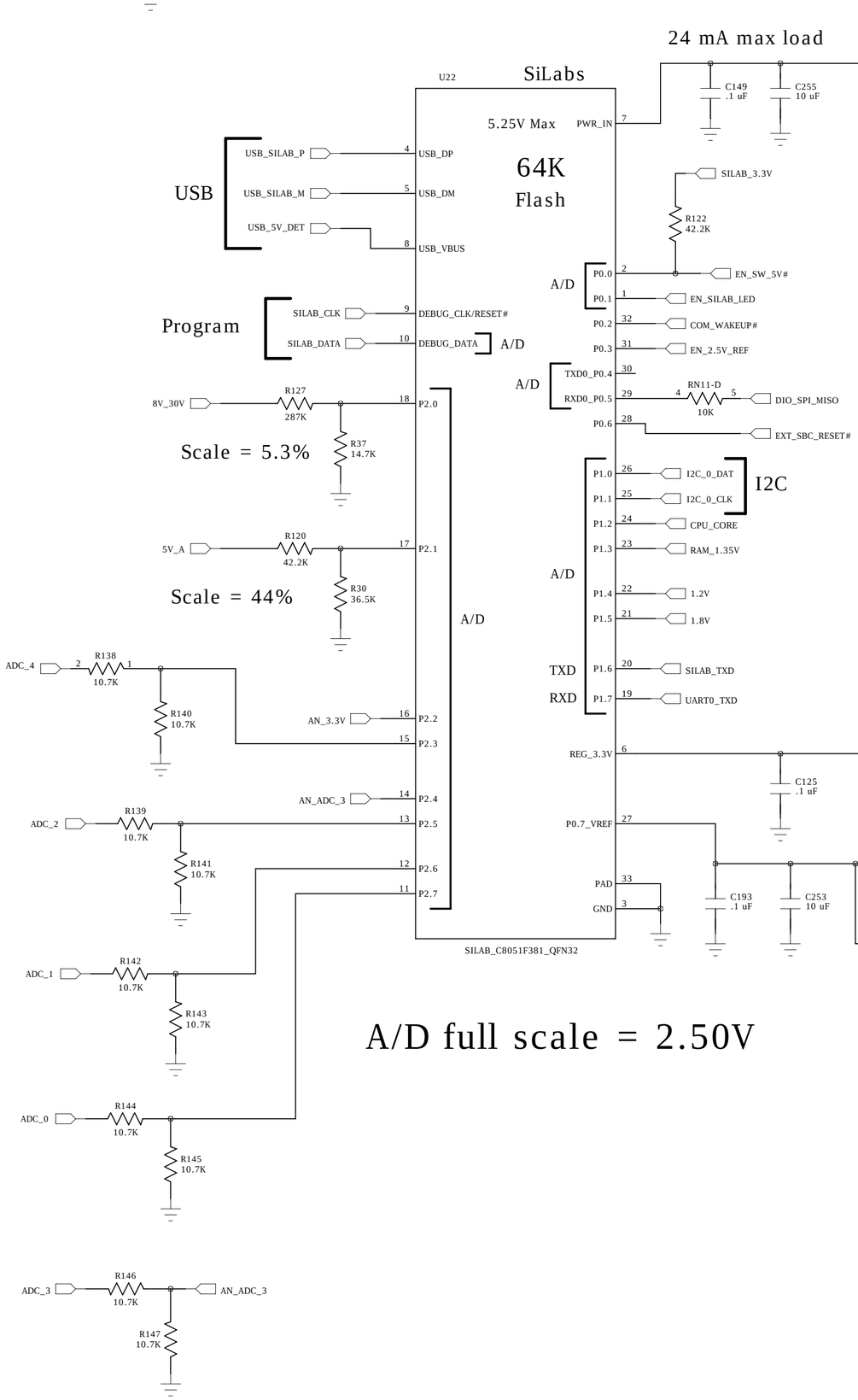
USB Device Port and SiLab uC





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