TS-7800-V2 Standard Options

XOPP1 — NC — ASSEMBLY_OPTIONS

Option 1	TS-7800-V2-DMN1I	Marvell Armada 385 1.33 GHz ARM Cortex A9 1G DDR3 RAM, 4GB eMMC Flash, Temp Sensor, Real Time Clock, Full-Duplex RS-485(-40C to 85C)
Option 2	TS-7800-V2-DMW2I	Marvell Armada 385 1.33 GHz ARM Cortex A9 1G DDR3 RAM and 4GB eMMC Flash, WiFi, Temp Sensor, Real Time Clock, Full-Duplex RS-485(-40C to 85C)
Option 3	TS-7800-V2-DMW3I	Marvell Armada 385 1.33 GHz ARM Cortex A9 1G DDR3 RAM, 4GB eMMC Flash, mPCIe, WiFi, Accelerometer, Temp Sensor, RTC, Full-Duplex RS-485(-40C to 85C)

Optional Components/Features Summary

All Parts are Industrial Temp

WiFi/Bluetooth Option

w/ Chip Antenna

U.FL available on request

Included only on xxWxx Standard Options

ADD: K2 (chip antenna). U37

(alternate: U.FL antenna connector)

CPU Heat Sink

Included on ALL Standard Options

ADD: Alpha Novatech S08CHL0A

Available Accesories

Included on NO Standard Options

TS-781 "8-28V Power daughter board"

Compatable ONLY with xxx1x, xxx2x Standard Option

Accelerometer Option

Included only on xxx3x Standard Option

ADD: U26

mini-PCIe/mSATA Option

Included only on xxx3x Standard Option

ADD: CN44, P1, P2

REMOVE: CN10, HD2

Rev.P2 --> Rev.A Changes:

Added new RTC (U41 = M41T00) on I2C bus

Add PD on MPP_10 (R57) - this disables clocks on MPP_45 and 46

Removed D7, connected SYS_RESET# to Silab pin 32

CN44 (Mini-PCIe) pin 22 needs to use DIO (use CPU_TYPE_1)

Change "CPU_TYPE_1" to be biased low (R46) to indicate Rev.A

PTP Ethernet timing will not be supported

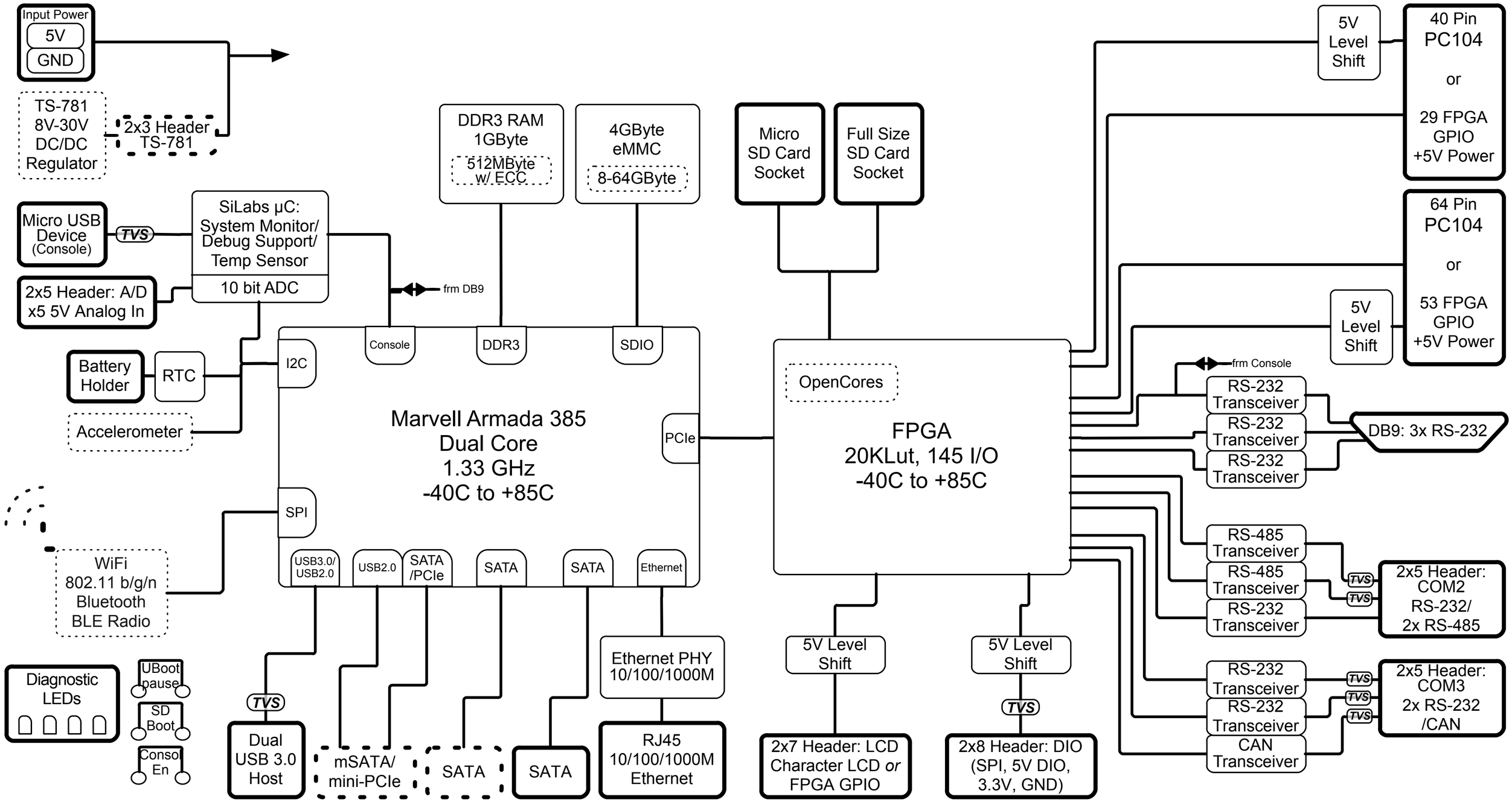
Moved SATA Conn (CN10) away from PC/104 Conn 0.3mm

Made FPGA_RESET longer = 680 ms

Web Schematic: Some proprietary information has been withheld.

Technologic Systems	Date Jan. 20, 2018	
Title: TS-7800-V2		
Rev: A	Designer	Sheet 2 of 27

TS-7800-V2 Block Diagram



Technologic Systems	Date Jan. 20, 2018	
Title: TS-7800-V2		
Rev: A	Designer	Sheet 2 of 27

DDR3 RAM

RAM_D[00:39]

RAM_A[00:15]

U7-A

RAM_D00	H3	M_DQ[0]	
RAM_D01	H2	M_DQ[1]	
RAM_D02	H1	M_DQ[2]	
RAM_D03	J1	M_DQ[3]	
RAM_D04	L2	M_DQ[4]	
RAM_D05	L1	M_DQ[5]	
RAM_D06	K2	M_DQ[6]	
RAM_D07	L3	M_DQ[7]	
RAM_D08	C1	M_DQ[8]	
RAM_D09	B1	M_DQ[9]	
RAM_D10	A4	M_DQ[10]	
RAM_D11	C2	M_DQ[11]	
RAM_D12	C4	M_DQ[12]	
RAM_D13	A3	M_DQ[13]	
RAM_D14	B2	M_DQ[14]	
RAM_D15	B4	M_DQ[15]	
RAM_D16	C7	M_DQ[16]	
RAM_D17	B6	M_DQ[17]	
RAM_D18	A6	M_DQ[18]	
RAM_D19	C6	M_DQ[19]	
RAM_D20	C9	M_DQ[20]	
RAM_D21	B9	M_DQ[21]	
RAM_D22	A9	M_DQ[22]	
RAM_D23	B8	M_DQ[23]	
RAM_D24	M2	M_DQ[24]	
RAM_D25	M3	M_DQ[25]	
RAM_D26	P2	M_DQ[26]	
RAM_D27	N2	M_DQ[27]	
RAM_D28	R3	M_DQ[28]	
RAM_D29	R2	M_DQ[29]	
RAM_D30	T2	M_DQ[30]	
RAM_D31	U2	M_DQ[31]	

	D1	M_CB[0]	
	E3	M_CB[1]	
	E2	M_CB[2]	
	F3	M_CB[3]	
	G2	M_CB[4]	
	H4	M_CB[5]	
	G4	M_CB[6]	
	E1	M_CB[7]	

RAM_DQS0_P	J2	M_DQS[0]	
RAM_DQS0_M	J3	M_DQSn[0]	
RAM_DQS1_P	B3	M_DQS[1]	
RAM_DQS1_M	A2	M_DQSn[1]	
RAM_DQS2_P	B7	M_DQS[2]	
RAM_DQS2_M	A7	M_DQSn[2]	
RAM_DQS3_P	P1	M_DQS[3]	
RAM_DQS3_M	R1	M_DQSn[3]	
	F2	M_DQS[4]	
	F1	M_DQSn[4]	

RAM_DQM0	M1	M_DM[0]	
RAM_DQM1	D2	M_DM[1]	
RAM_DQM2	B5	M_DM[2]	
RAM_DQM3	U1	M_DM[3]	
	H5	M_DM[4]	

	B15	M_A[0]	RAM_A00
	C15	M_A[1]	RAM_A01
	E13	M_A[2]	RAM_A02
	B13	M_A[3]	RAM_A03
	D15	M_A[4]	RAM_A04
	A13	M_A[5]	RAM_A05
	B16	M_A[6]	RAM_A06
	D16	M_A[7]	RAM_A07
	C16	M_A[8]	RAM_A08
	E14	M_A[9]	RAM_A09
	D11	M_A[10]	RAM_A10
	D14	M_A[11]	RAM_A11
	E12	M_A[12]	RAM_A12
	B14	M_A[13]	RAM_A13
	E15	M_A[14]	RAM_A14
	E10	M_A[15]	RAM_A15

	C13	M_BA[0]	RAM_BA0
	A16	M_BA[1]	RAM_BA1
	A15	M_BA[2]	RAM_BA2

	D13	M_CSn[0]	RAM_CS0#
	C17	M_CSn[1]	

	D12	M_ODT[0]	RAM_ODT0
	B11	M_ODT[1]	

	C12	M_WEn	RAM_WE#
	E11	M_RASn	RAM_RAS#
	B12	M_CASn	RAM_CAS#
	E9	M_RESETn	RAM_RESET#

	A12	M_CKE[0]	RAM_CKE0
	C10	M_CKE[1]	

	B10	M_CLKOUT[0]	RAM_CLK_P
	A10	M_CLKOUTn[0]	RAM_CLK_M
	D10	M_CLKOUT[1]	
	D9	M_CLKOUTn[1]	

	E5	M_PCAL[0]	R18 931
	A17	M_PCAL[1]	R20 931
	D18	M_PCAL[2]	R21 931

	F5	M_NCAL[0]	R22 931
	B17	M_NCAL[1]	R23 931
	D17	M_NCAL[2]	R24 931

RAM_1.35V

CPU_MARVELL_88F6820

U23

512 MB

RAM_A00	N3	A0
RAM_A01	P7	A1
RAM_A02	P3	A2
RAM_A03	N2	A3
RAM_A04	P8	A4
RAM_A05	P2	A5
RAM_A06	R8	A6
RAM_A07	R2	A7
RAM_A08	T8	A8
RAM_A09	R3	A9
RAM_A10	L7	A10
RAM_A11	R7	A11
RAM_A12	N7	A12
RAM_A13	T3	A13
RAM_A14	T7	A14
RAM_A15	M7	A15/NC

Twin Die

	J1	TWIN_ODT1
	J9	TWIN_SDCKE1
	L1	TWIN_CS1#

RAM_BA0	M2	BA0
RAM_BA1	N8	BA1
RAM_BA2	M3	BA2

RAM_RAS#	J3	RAS#
RAM_CAS#	K3	CAS#
RAM_WE#	L3	WE#

RAM_CLK_P	J7	CK
RAM_CLK_M	K7	CK#

RAM_CKE0	K9	CKE
RAM_CS0#	L2	CS#
RAM_RESET#	T2	RESET#
RAM_ODT0	K1	ODT

RAM_DQM2	D3	UDM
RAM_DQM1	E7	LDM

RAM_DQS2_P	C7	UDQS
RAM_DQS2_M	B7	UDQS#
RAM_DQS1_P	F3	LDQS
RAM_DQS1_M	G3	LDQS#

RAM_VREF	H1	VREF_DQ
	M8	VREF_CA
	L8	ZQ
	L9	TWIN_ZQ1

C175 .1 uF

C167 .1 uF

R105 240

VDD0	B2	RAM_1.35V
VDD1	D9	
VDD2	G7	
VDD3	K2	
VDD4	K8	
VDD5	N1	
VDD6	N9	
VDD7	R1	
VDD8	R9	

C177 .1 uF, C178 .1 uF, C186 .1 uF, C179 .1 uF, C180 .1 uF, C181 .1 uF

VDDQ0	A1	RAM_1.35V
VDDQ1	A8	
VDDQ2	C1	
VDDQ3	D2	
VDDQ4	E9	
VDDQ5	F1	
VDDQ6	H2	
VDDQ7	H9	
VDDQ8	C9	

C171 .1 uF, C174 .1 uF, C172 .1 uF, C166 .1 uF, C170 .1 uF, C190 .1 uF, C191 .1 uF, C199 .1 uF

RAM_D[00:39]

DQ0	E3	RAM_D10
DQ1	F7	RAM_D09
DQ2	F2	RAM_D15
DQ3	F8	RAM_D08
DQ4	H3	RAM_D13
DQ5	H8	RAM_D14
DQ6	G2	RAM_D12
DQ7	H7	RAM_D11
DQ8	D7	RAM_D16
DQ9	C3	RAM_D23
DQ10	C8	RAM_D19
DQ11	C2	RAM_D22
DQ12	A7	RAM_D18
DQ13	A2	RAM_D21
DQ14	B8	RAM_D17
DQ15	A3	RAM_D20

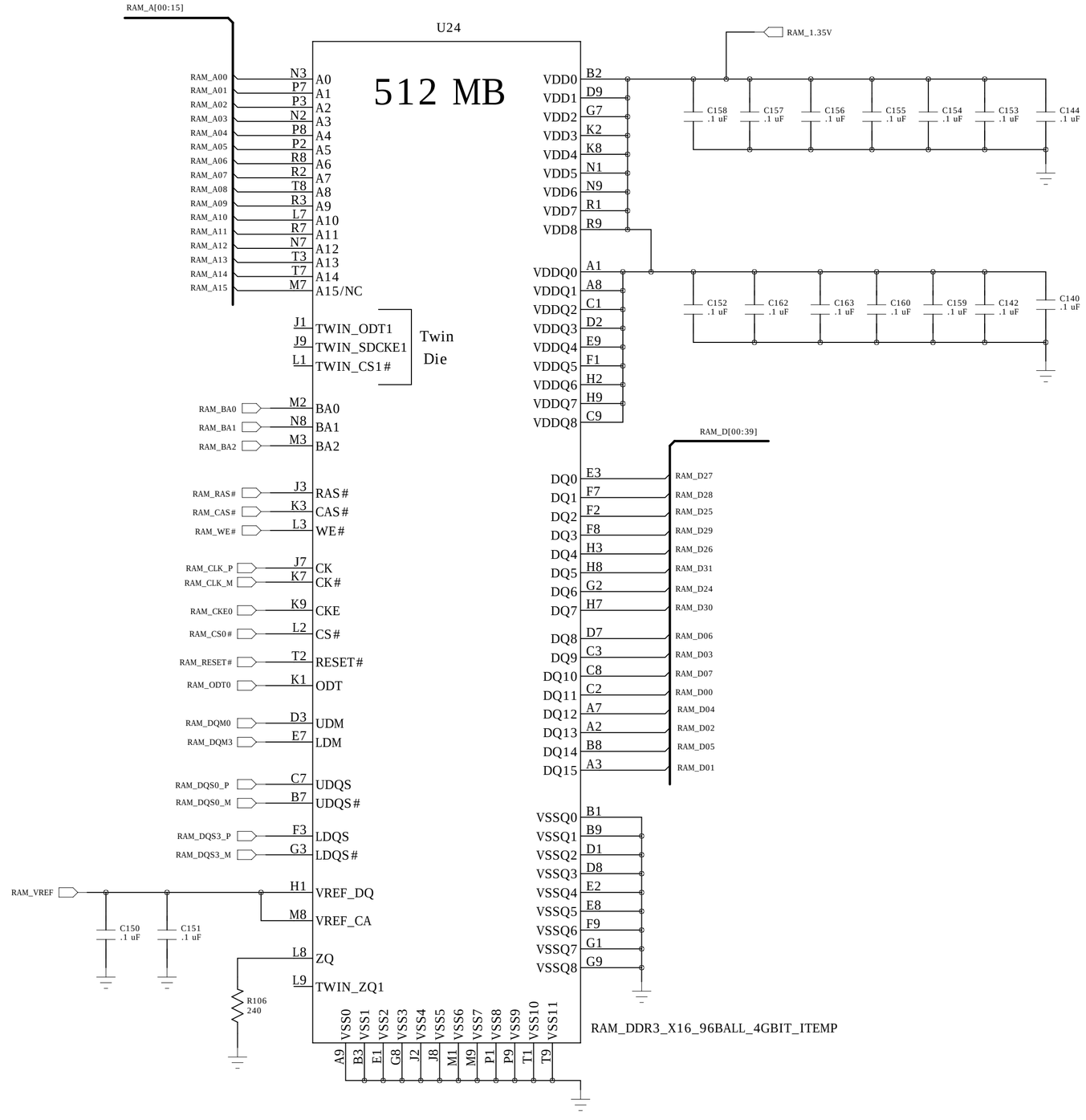
VSSQ0	B1	
VSSQ1	B9	
VSSQ2	D1	
VSSQ3	D8	
VSSQ4	E2	
VSSQ5	E8	
VSSQ6	F9	
VSSQ7	G1	
VSSQ8	G9	

VSS0	A9	
VSS1	B3	
VSS2	E1	
VSS3	G8	
VSS4	J2	
VSS5	J8	
VSS6	M1	
VSS7	M9	
VSS8	P1	
VSS9	P9	
VSS10	T1	
VSS11	T9	

RAM_DDR3_X16_96BALL_4GBIT_ITEMP

Technologic Systems	Date	Jan. 20, 2018
Title: TS-7800-V2 CPU DDR		
Rev: A	Designer	Sheet 4 of 27

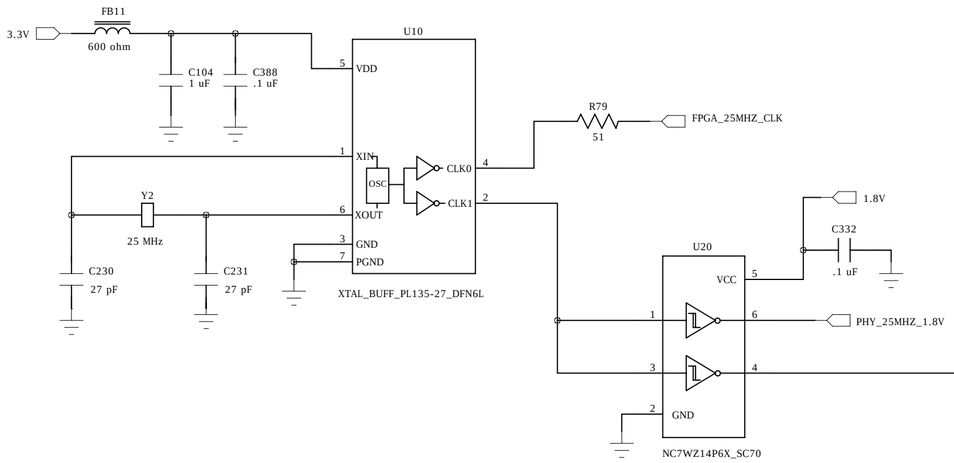
DDR3 RAM

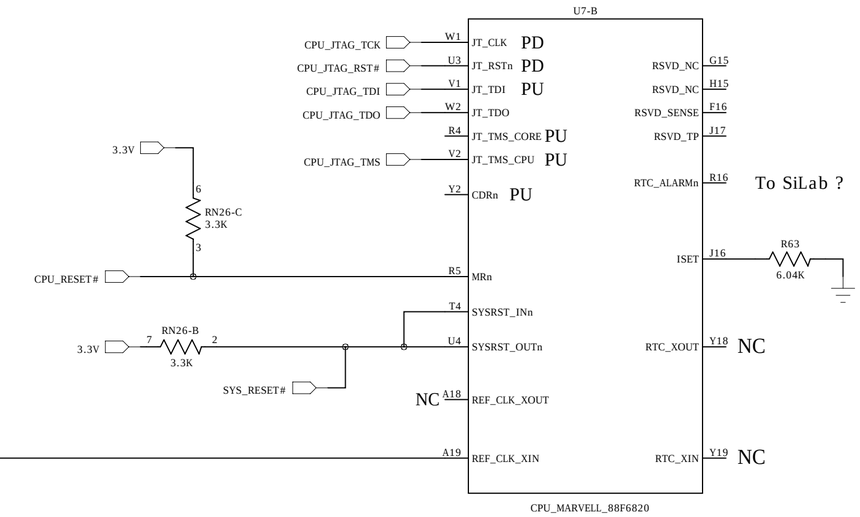


Technologic Systems	Date Jan. 20, 2018	
Title: TS-7800-V2		
Rev: A	Designer	Sheet 5 of 27

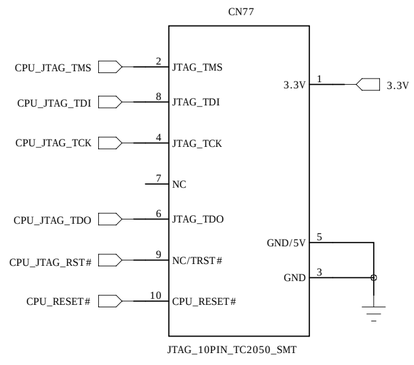
CPU

25 MHz Osc.



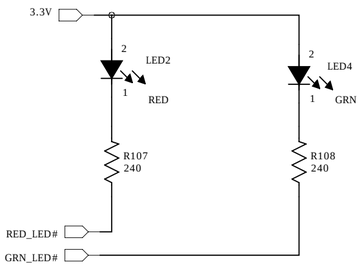


CPU JTAG



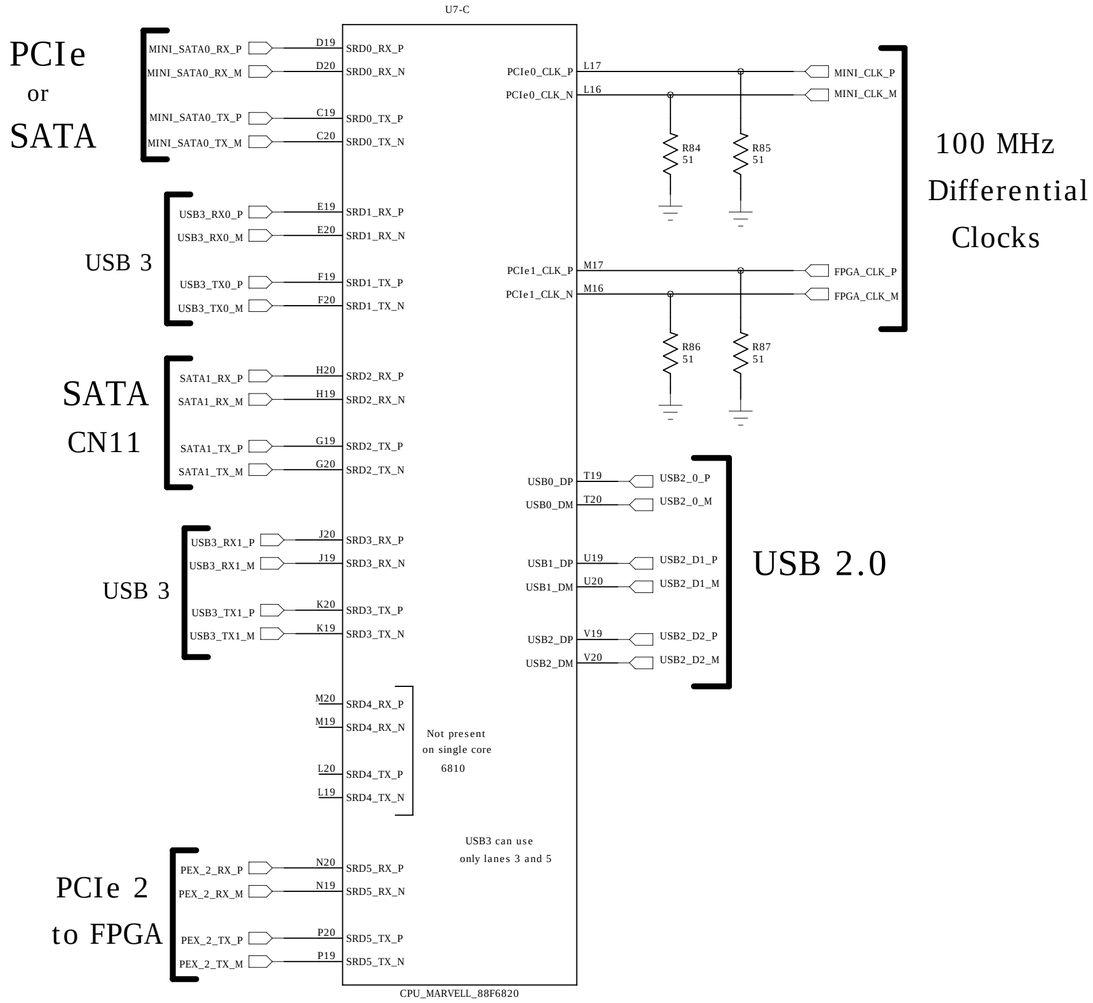
Tag-Connect

CPU LEDs



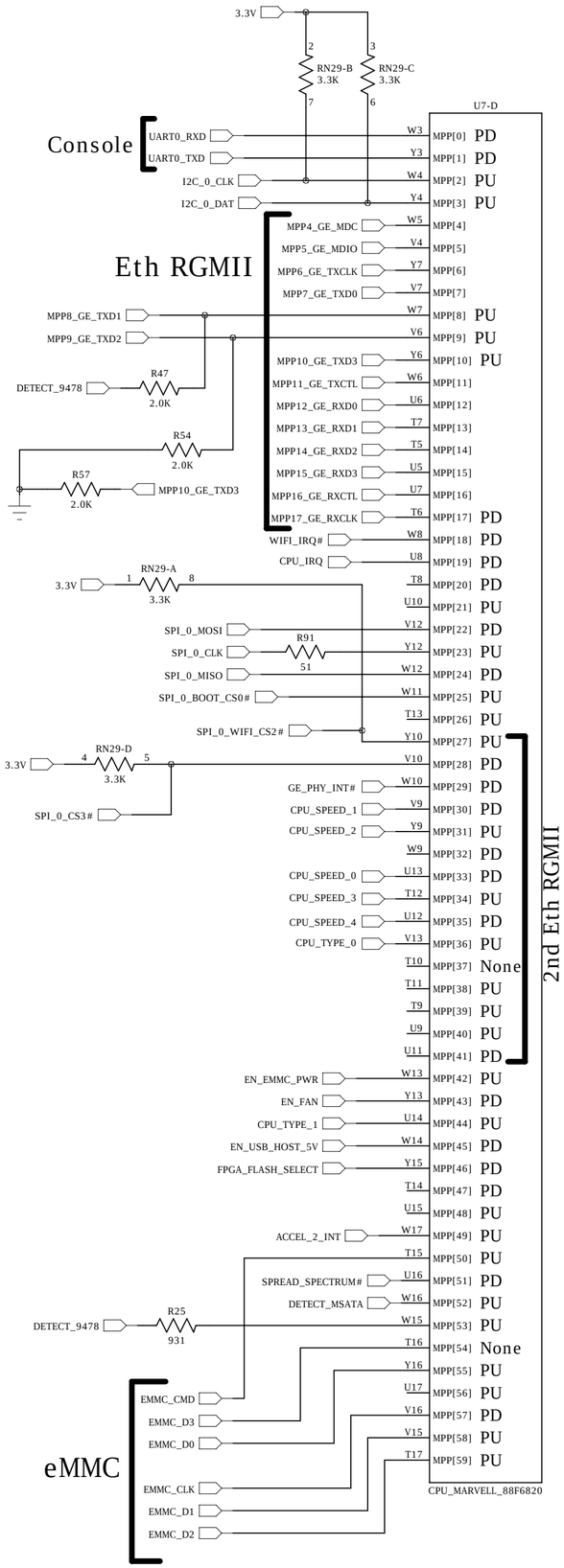
Technologic Systems	Date Jan. 20, 2018	
Title: TS-7800-V2 CPU Misc		
Rev: A	Designer	Sheet 7 of 27

CPU SERDES

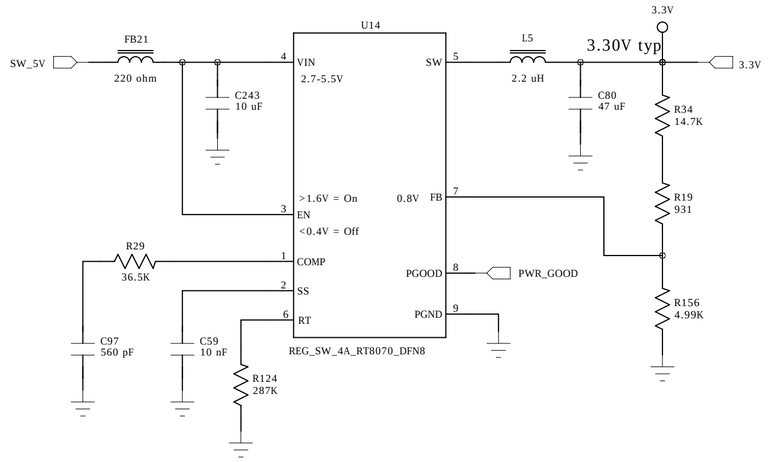


Technologic Systems	Date	Jan. 20, 2018
Title: TS-7800-V2 CPU SerDes		
Rev: A	Designer	Sheet 8 of 27

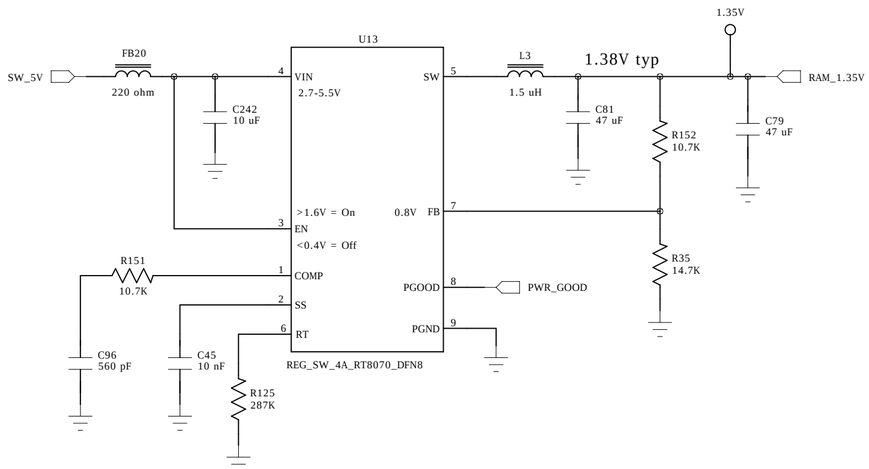
CPU DIO



3.3V Reg.

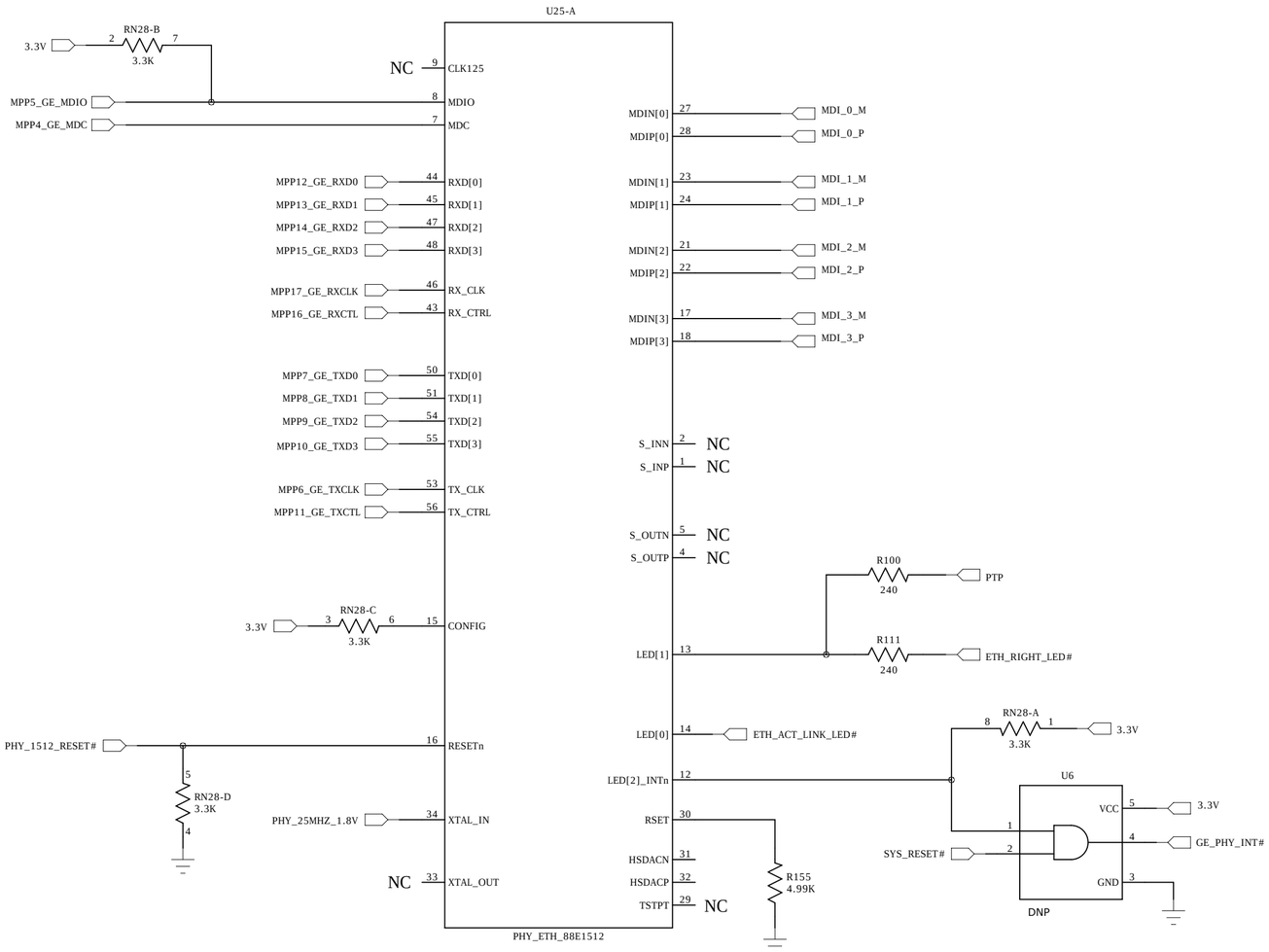


DDR3 1.35V Reg.



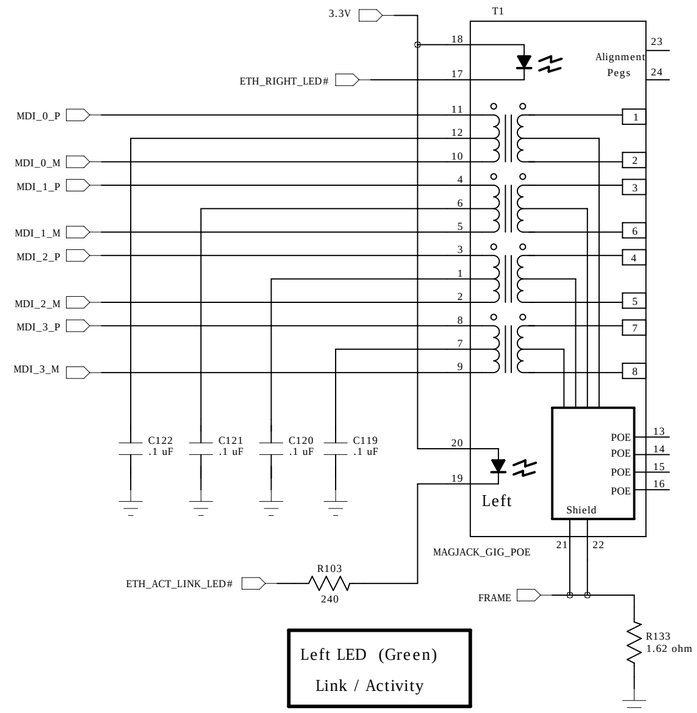
Technologic Systems		Date Jan. 20, 2018
Title: TS-7800-V2 CPU I/O		
Rev: A	Designer	Sheet 9 of 27

10/100/1000 Marvell 88E1512 PHY



Strapped for PHY
address = 1

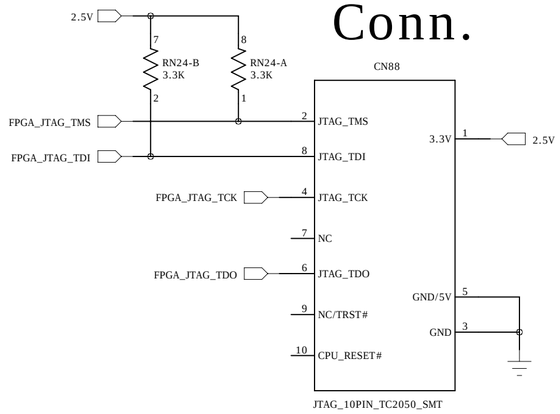
Gig MagJack



Left LED (Green)
Link / Activity

Technologic Systems		Date Jan. 20, 2018
Title: TS-7800-V2	Ethernet PHY	
Rev: A	Designer	Sheet 12 of 27

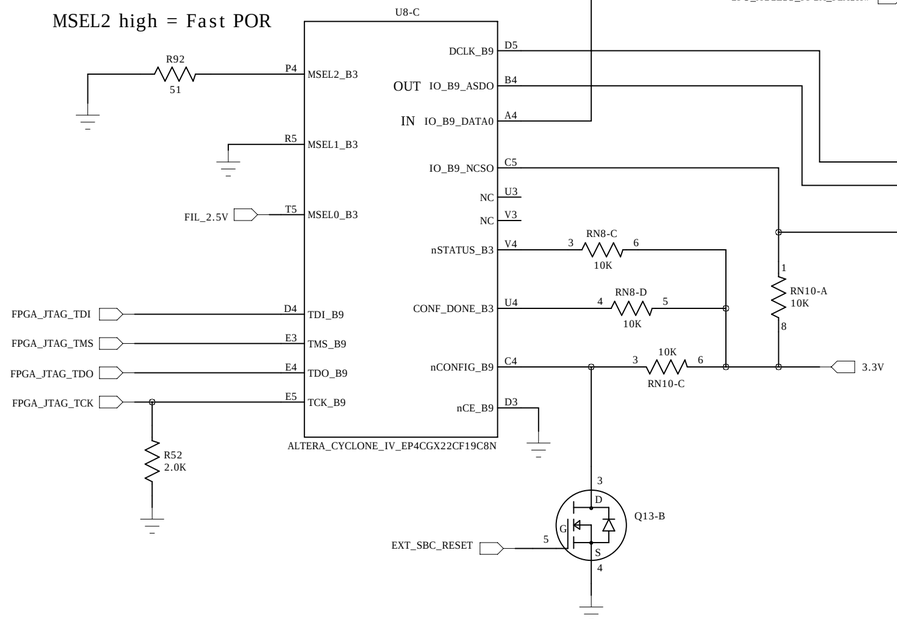
FPGA JTAG Conn.



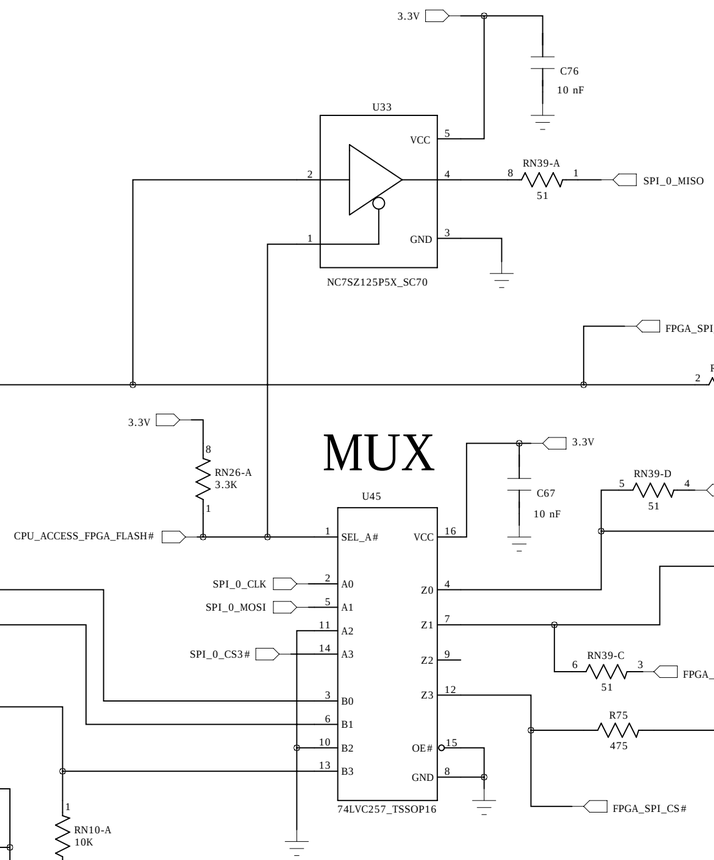
Tag-Connect

FPGA

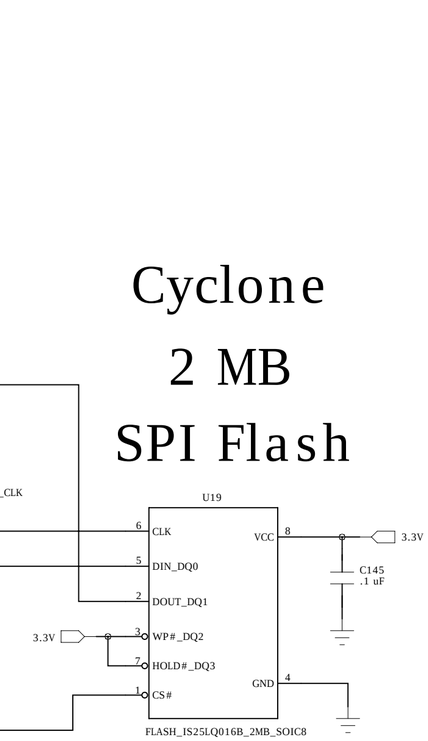
MSEL2 high = Fast POR



MUX



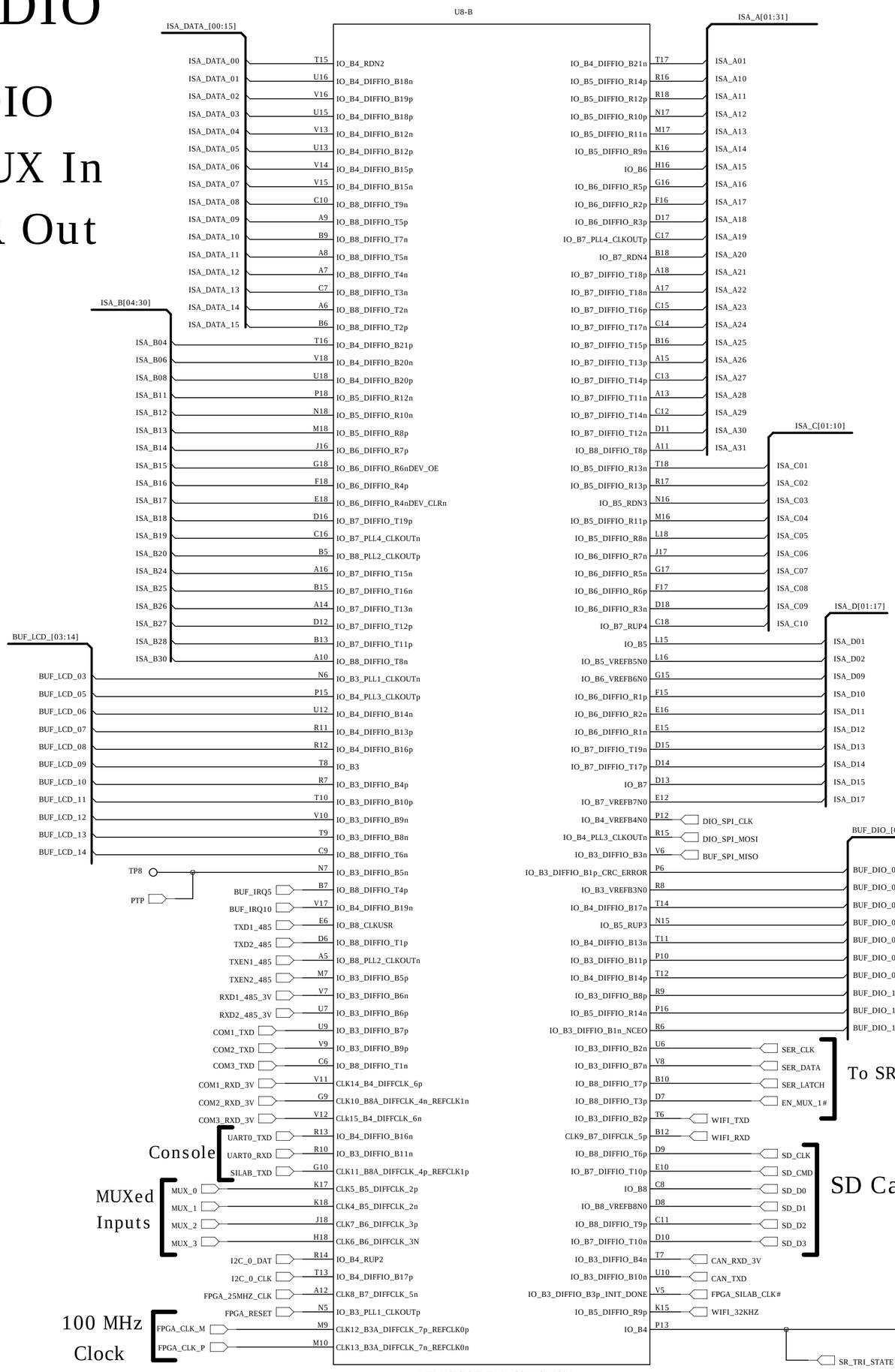
Cyclone 2 MB SPI Flash



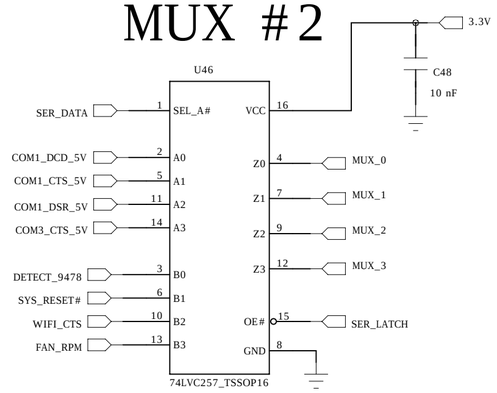
Technologic Systems	Date Jan. 20, 2018	
Title: TS-7800-V2		
Rev: A	Designer	Sheet 13 of 27

FPGA DIO

145 DIO
+ 16 MUX In
+ 16 SR Out

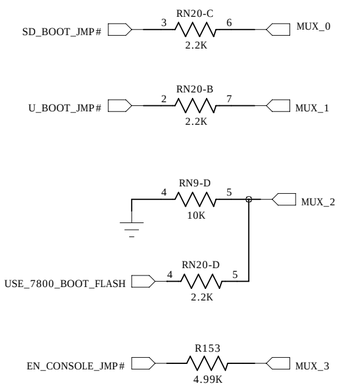


MUX #2

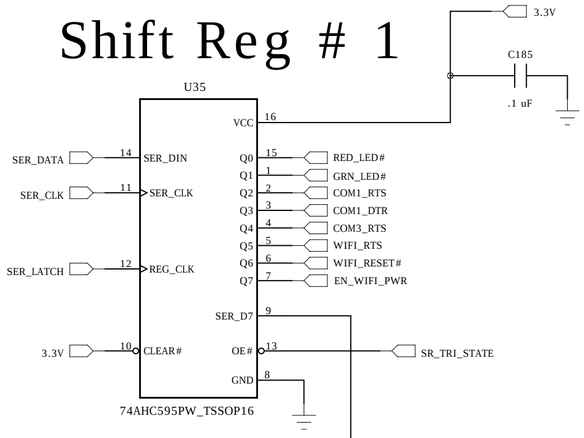


Provides 5V Tolerance

MUX Bias

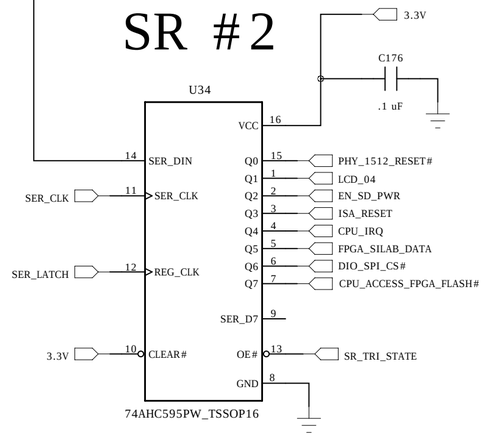


Shift Reg # 1



Shift Reg + Latch

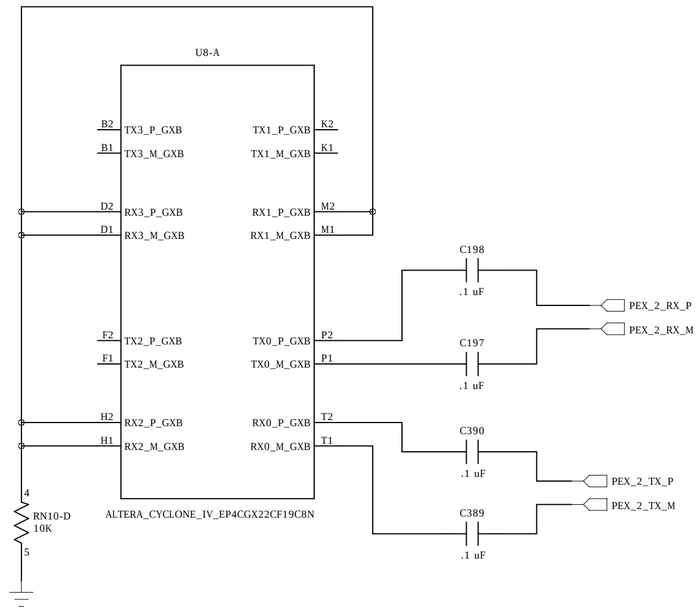
SR #2



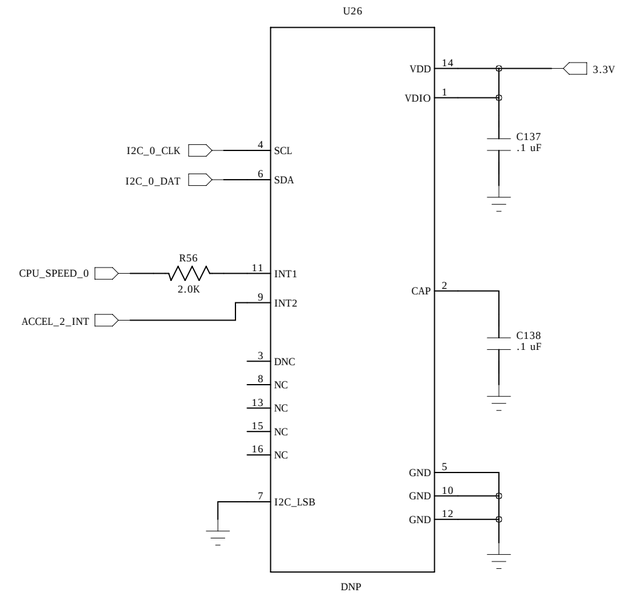
Shift Reg + Latch

Technologic Systems	Date Jan. 20, 2018	
Title: TS-7800-V2		
Rev: A	Designer	Sheet 14 of 27

Cyclone Transceivers



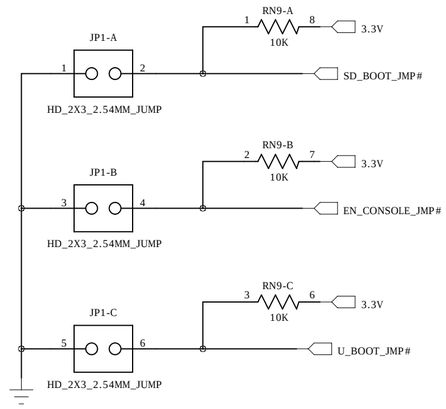
Accelerometer



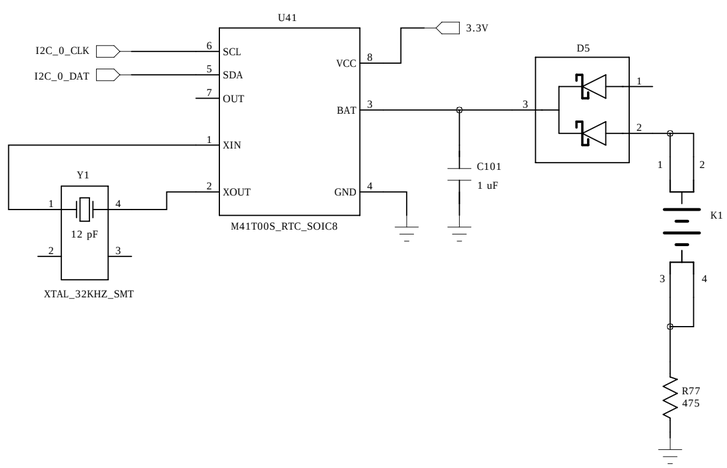
Option 3 = Accelerometer MMA8451

Technologic Systems	Date Jan. 20, 2018	
Title: TS-7800-V2		
Rev: A	Designer	Sheet 17 of 27

Jumpers



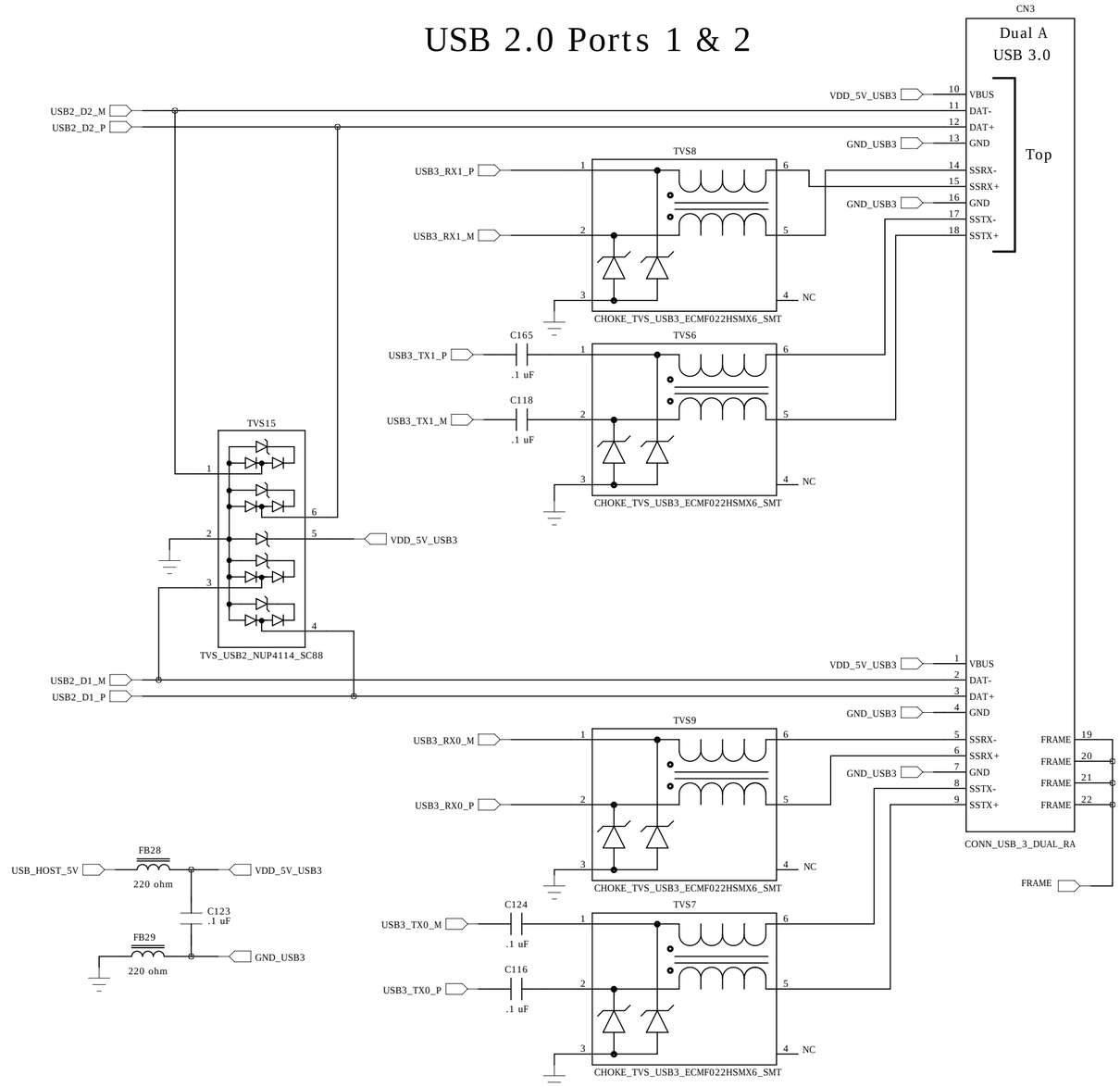
ST Micro RTC



Dual Host USB 3.0

USB 3.0 Ports 0 & 1

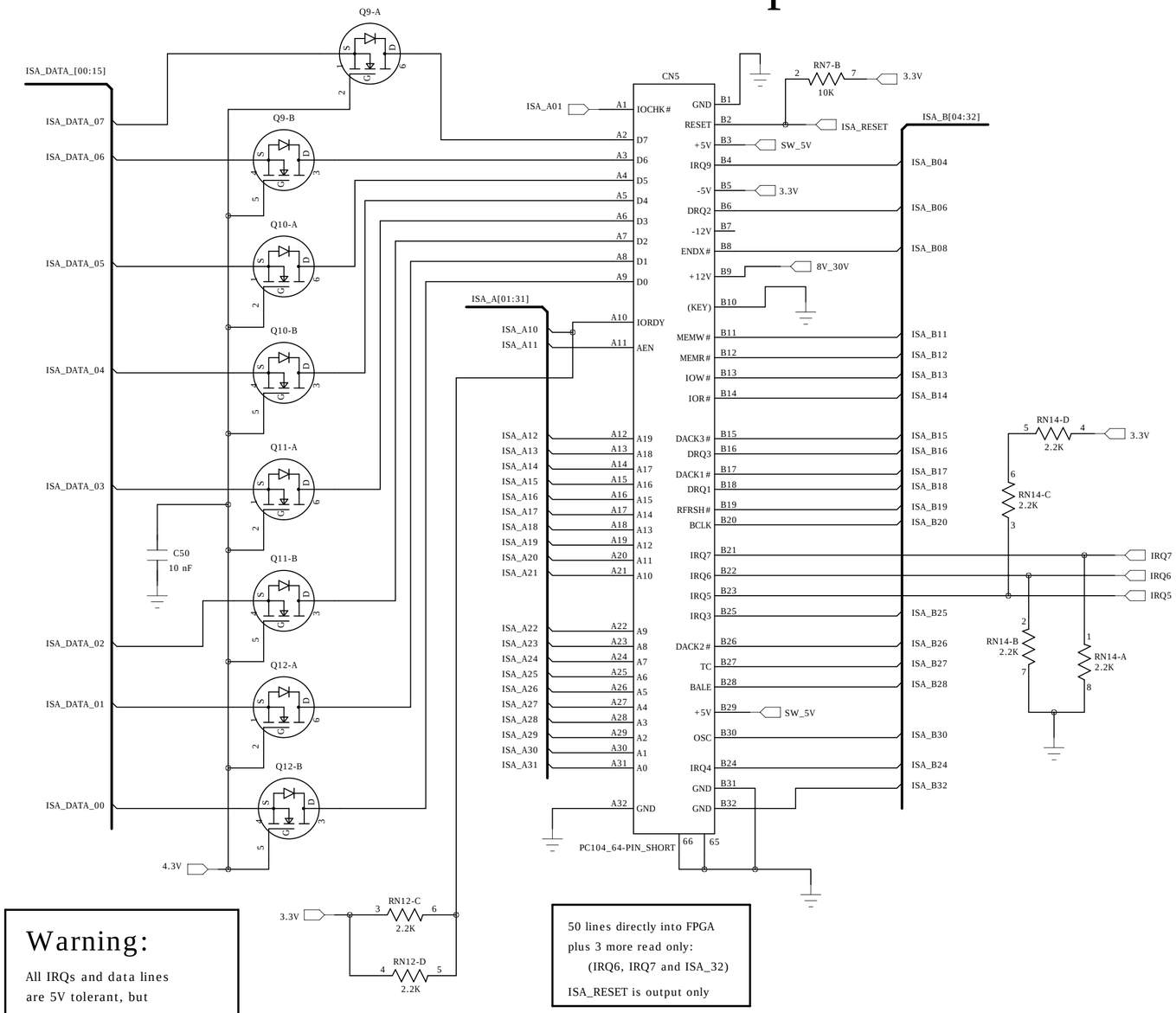
USB 2.0 Ports 1 & 2



Technologic Systems	Date Jan. 20, 2018	
Title: TS-7800-V2		
Rev: A	Designer	Sheet 18 of 27

FETs provide 5V tolerance

PC/104 64-pin Connector



Warning:

All IRQs and data lines are 5V tolerant, but

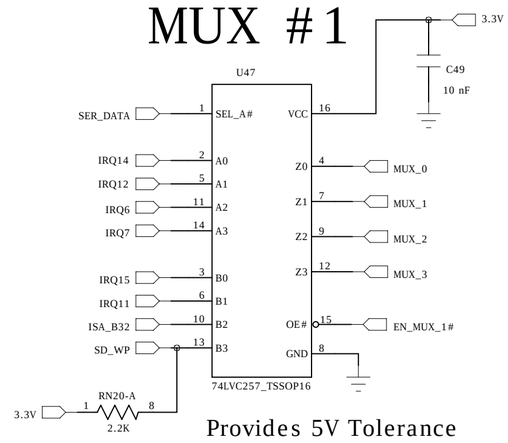
all other signals must use 3.3V levels

IRQ3 and 4 must be 3.3V levels

50 lines directly into FPGA plus 3 more read only:
(IRQ6, IRQ7 and ISA_32)

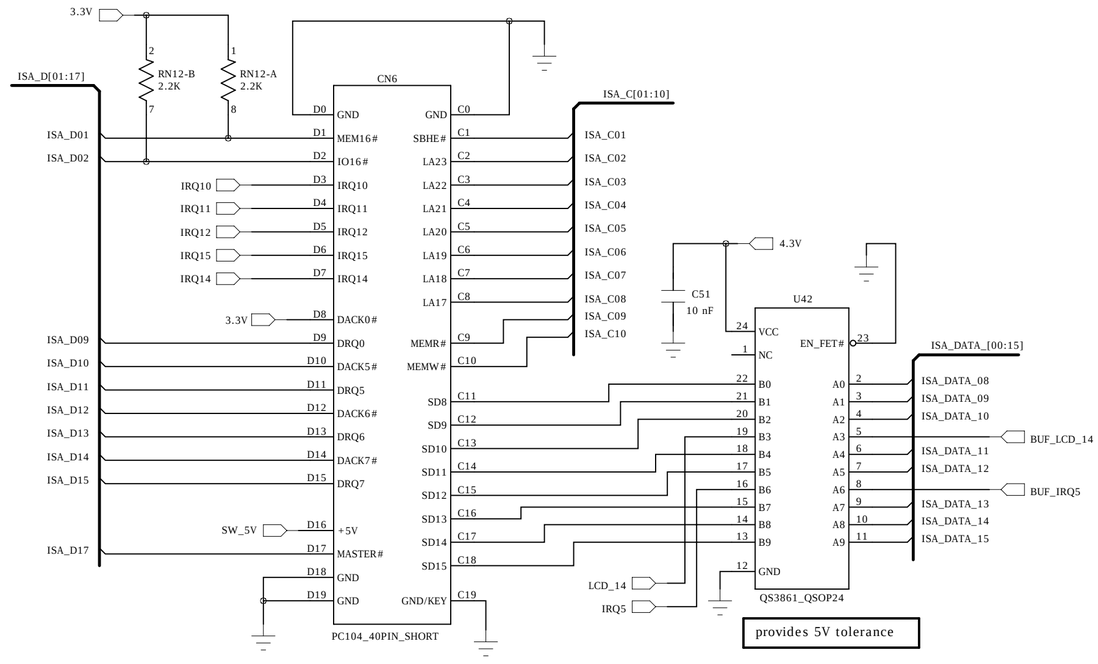
ISA_RESET is output only

MUX #1



Provides 5V Tolerance

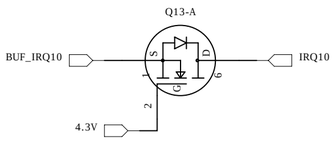
PC/104 40-pin Connector

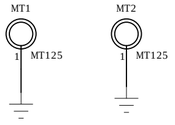


provides 5V tolerance

29 lines directly into FPGA (bi-directional)

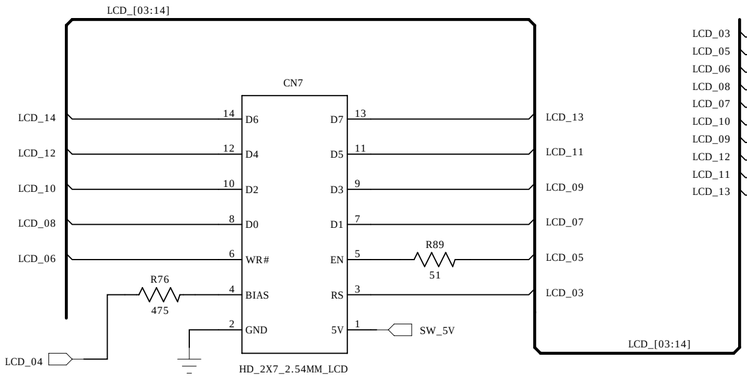
IRQ11 thru IRQ15 are read only

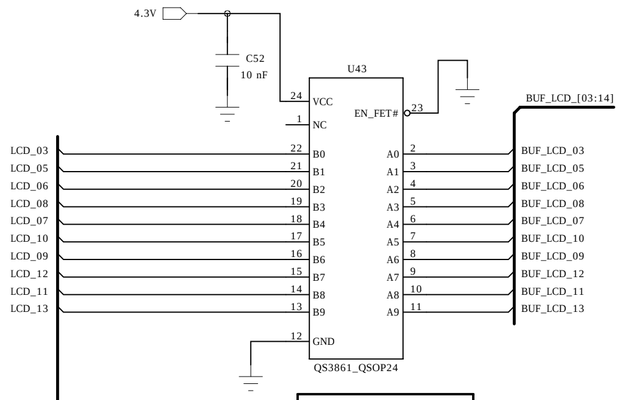




Technologic Systems	Date Jan. 20, 2018	
Title: TS-7800-V2		
Rev: A	Designer	Sheet 19 of 27

LCD Port





provides 5V tolerance

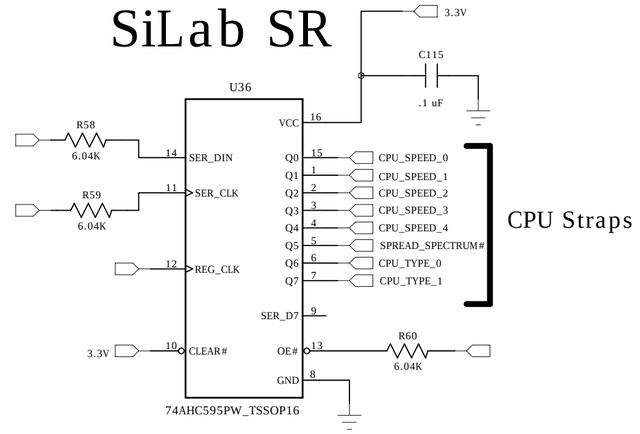
LCD03, LCD05, LCD06 init to inputs
when outputs, active high-low
These are programmable I/O

LCD07 thru LCD14 are always open
drain outputs, initialized to high
They can be used as inputs

All LCD lines are 5V tolerant

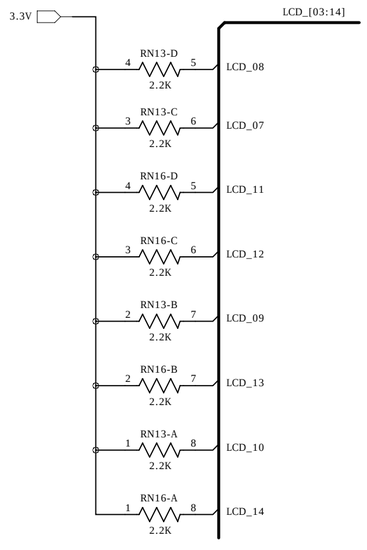
LCD04 is always output
active high-low, init to zero

SiLab SR



CPU Straps

Shift Reg + Latch

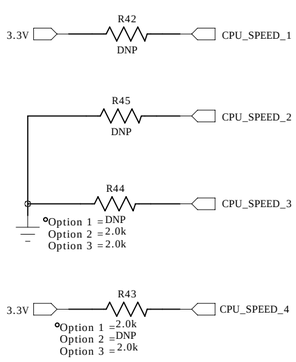


Pull-up resistors for
the open drain outputs

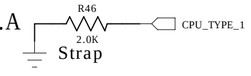
Open drain outputs can
sink 8 mA, but only source
current thru resistor

Option Res. Straps

4 Res. Straps for Board Config



Indicates Rev.A Strap



Resistor Strapping Table

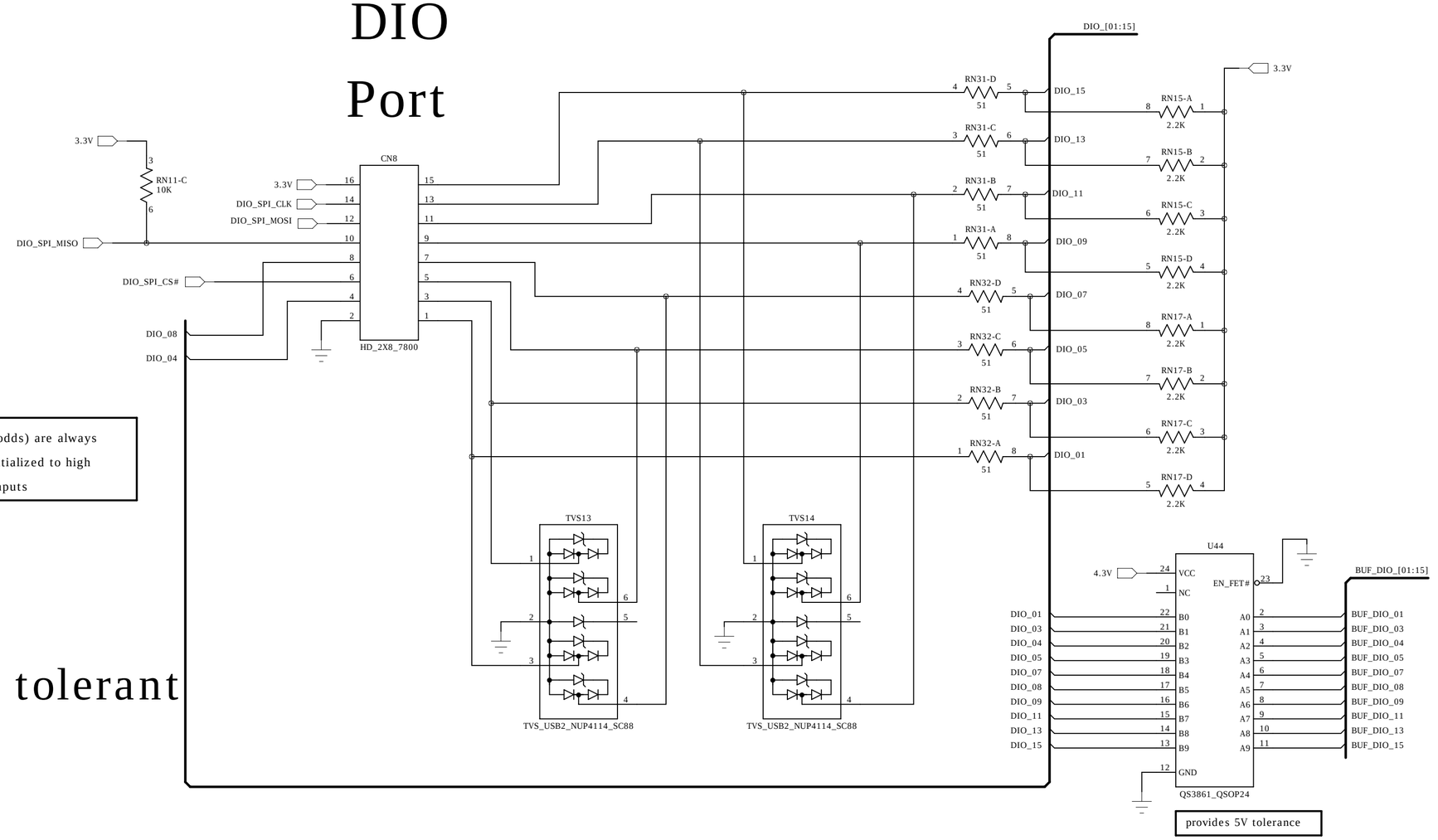
1 = POP, 0 = DNP

R42	R45	R44	R43		
0	0	0	1	Option 1	TS-7800-V2-DMN1I
0	0	1	0	Option 2	TS-7800-V2-DMW2I
0	0	1	1	Option 3	TS-7800-V2-DMW3I

MSB LSB

Technologic Systems	Date Jan. 20, 2018	
Title: TS-7800-V2		
Rev: A	Designer	Sheet 20 of 27

DIO Port



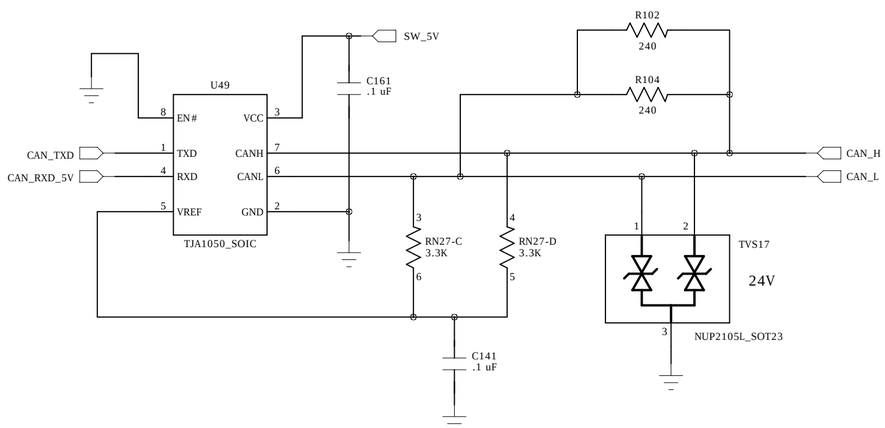
SPI_MISO is 5V tolerant
SPI_MOSI, CLK, and Frame
are 3.3V level outputs

DIO_01 thru DIO_15 (odds) are always
open drain outputs, initialized to high
They can be used as inputs

DIO_04 and DIO_08 initialize to inputs
when output, active high-low
They are programmable In or out

All DIO lines are 5V tolerant

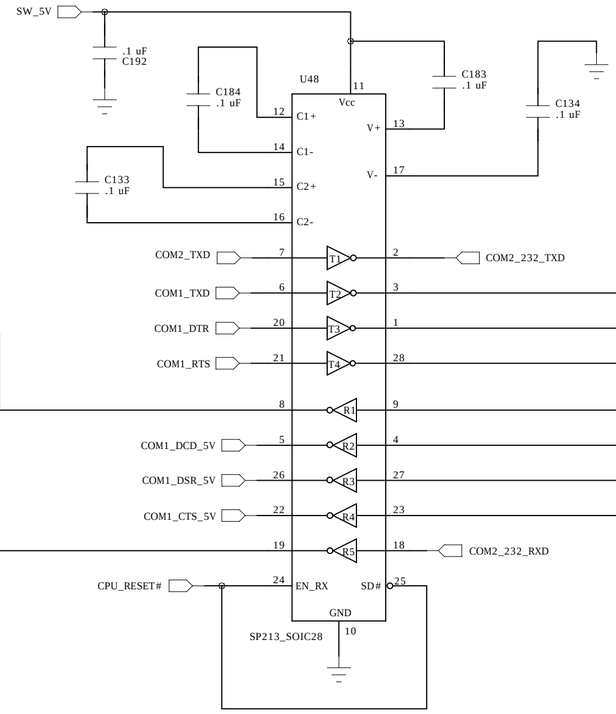
CAN Transceiver



Technologic Systems	Date Jan. 20, 2018	
Title: TS-7800-V2		
Rev: A	Designer	Sheet 21 of 27

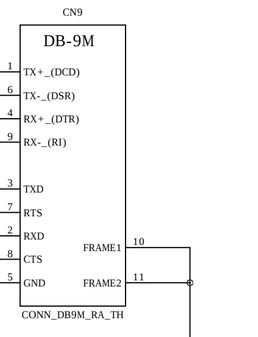
COM1

RS-232 Transceiver



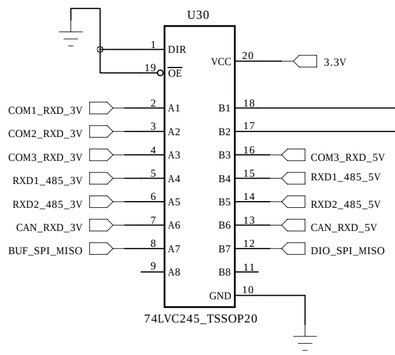
COM1

DB9M

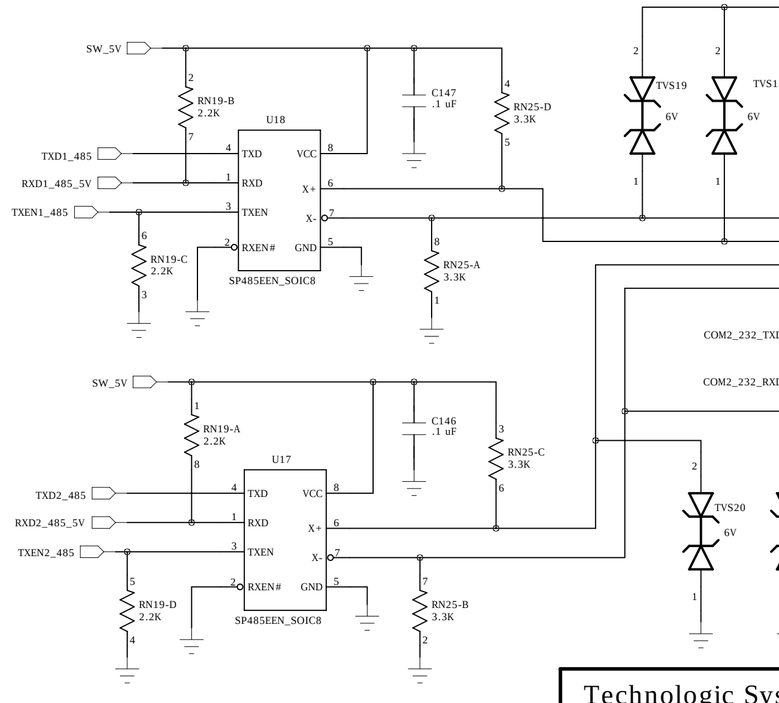


3.3V <-- 5V

Level shifter

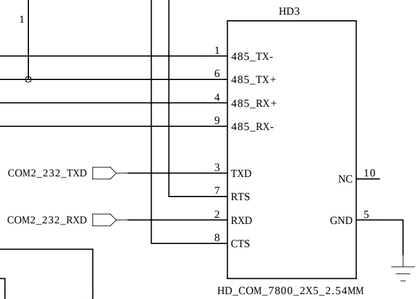


RS-485 Drivers

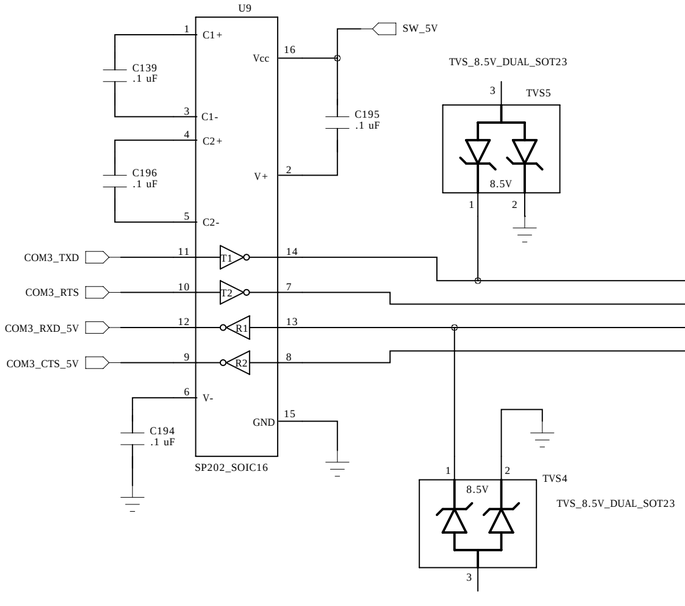


COM2

Header

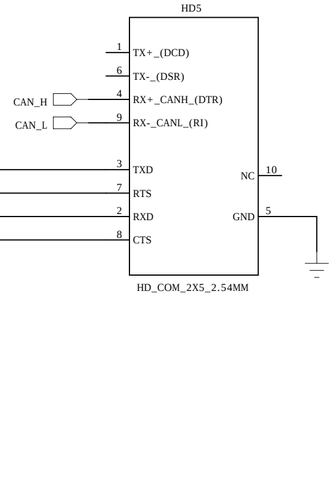


RS-232 Transceiver



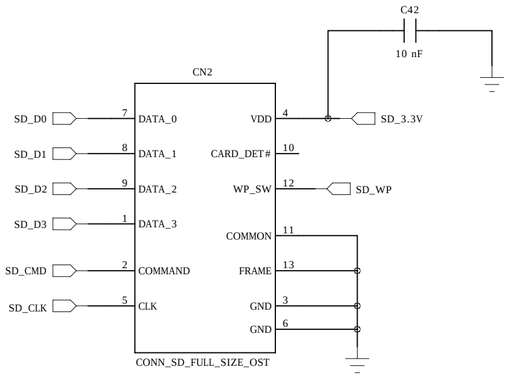
COM3

Header



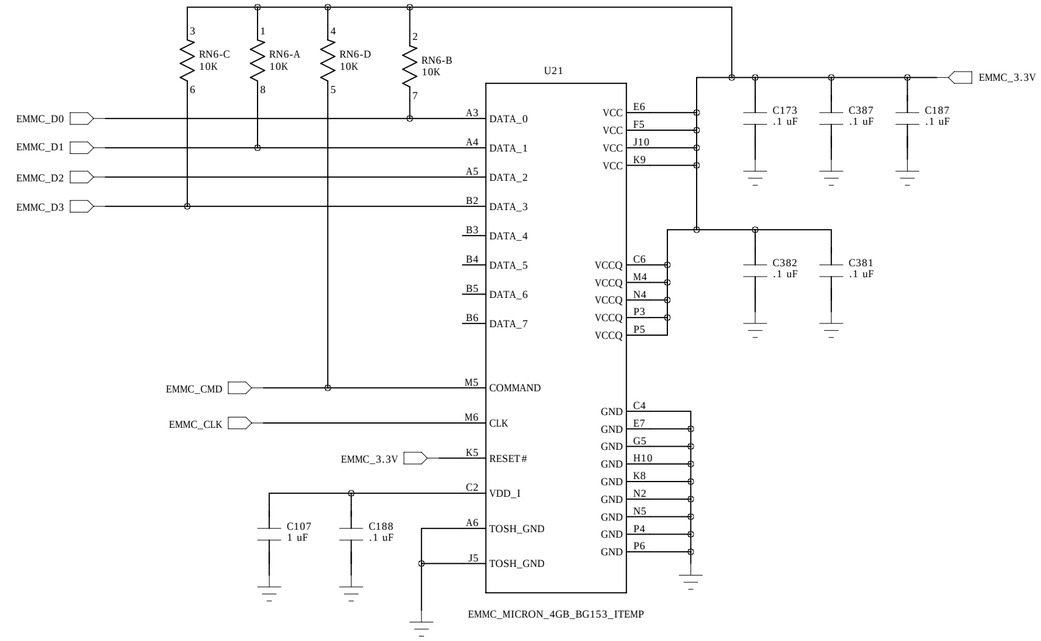
Technologic Systems	Date Jan. 20, 2018	
Title: TS-7800-V2		
Rev: A	Designer	Sheet 22 of 27

Full-Size SD Card Socket

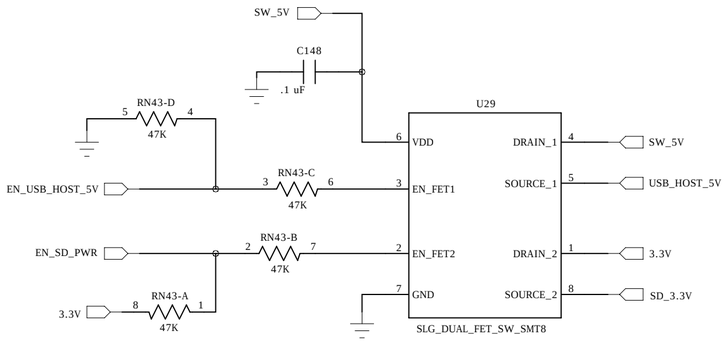


eMMC 4G

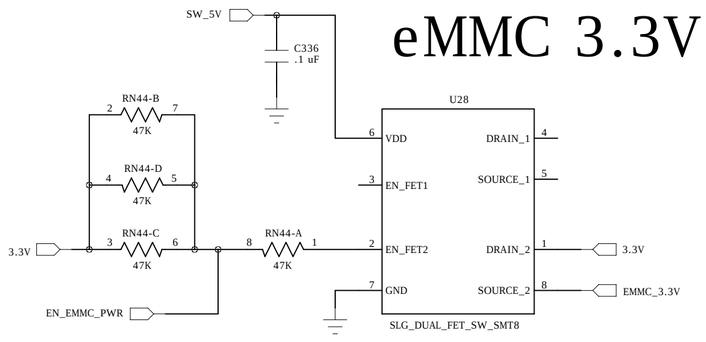
Optionally up to 64GB



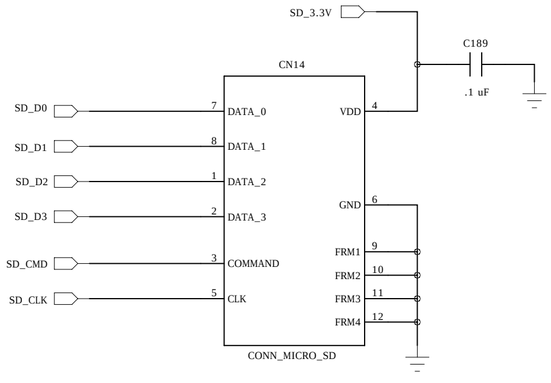
SD Card and USB Power Switch



eMMC 3.3V switch



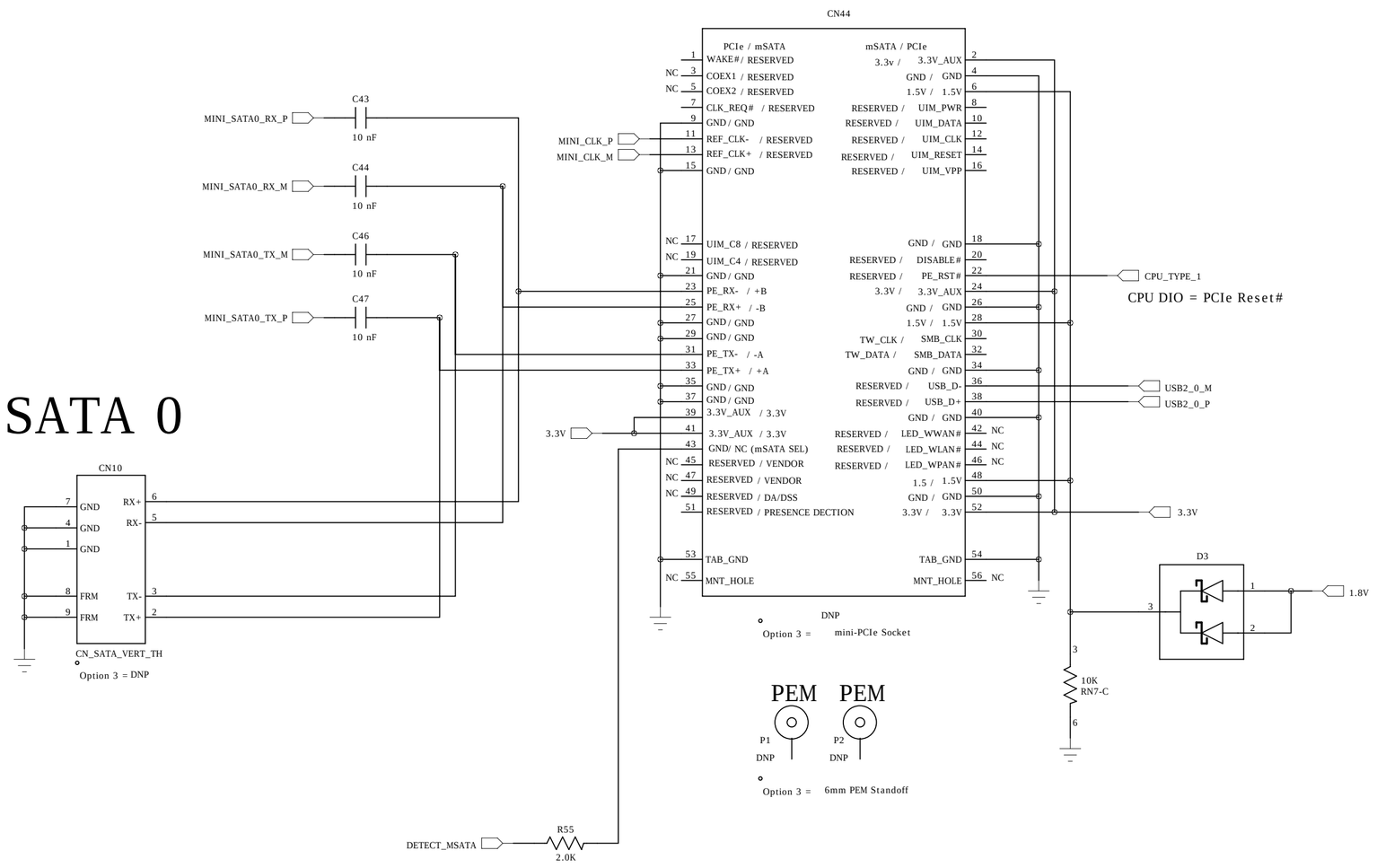
Micro SD Card Socket



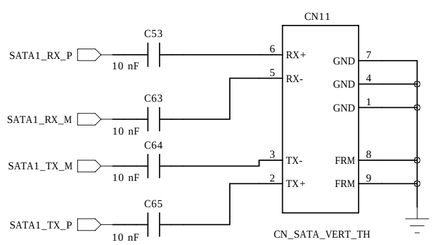
Technologic Systems	Date Jan. 20, 2018	
Title: TS-7800-V2		
Rev: A	Designer	Sheet 23 of 27

7mm Stack Height
to center of bd.

SATA 0

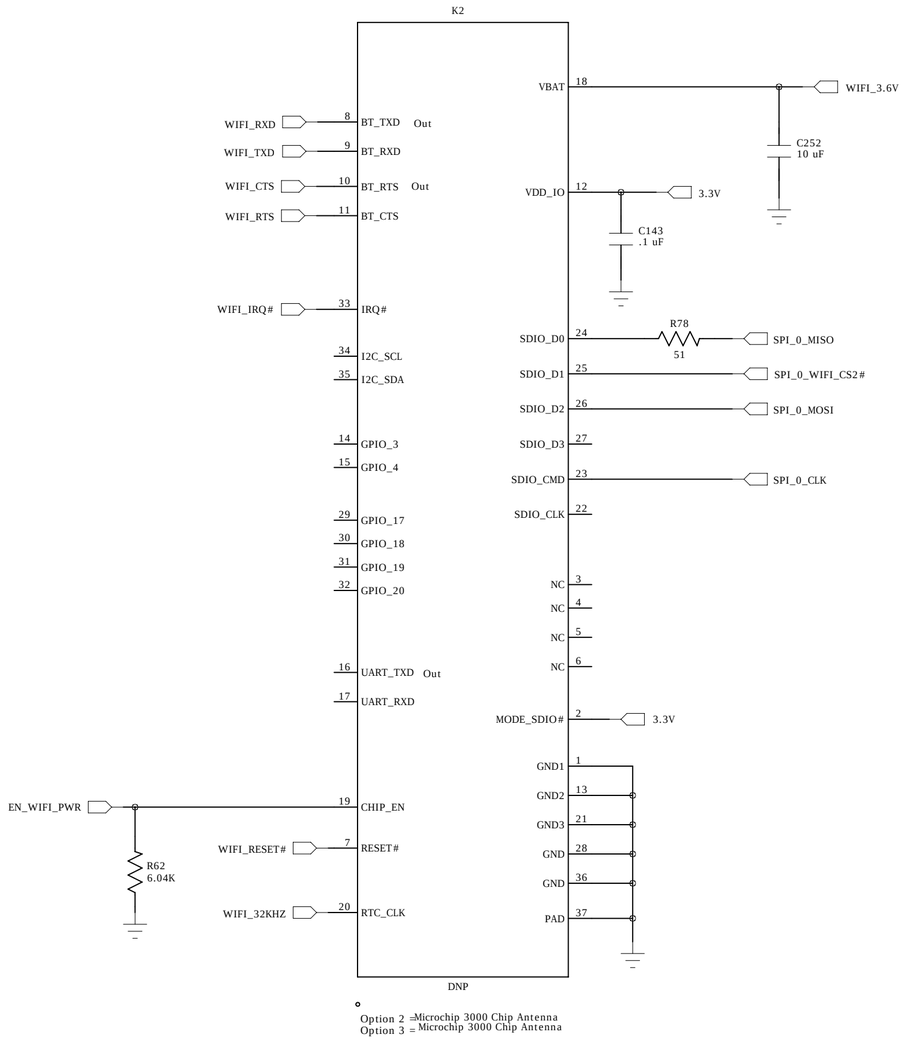


SATA 1

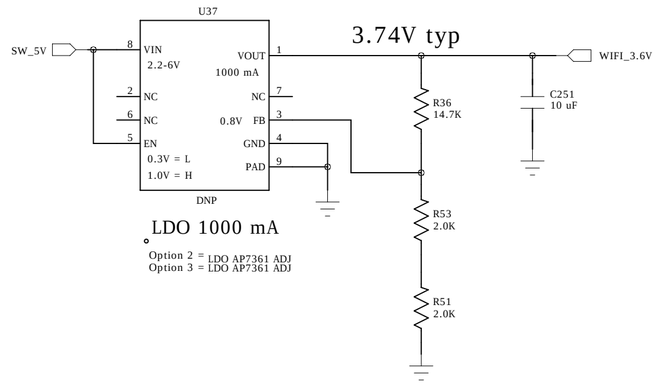


Technologic Systems	Date Jan. 20, 2018	
Title: TS-7800-V2		
Rev: A	Designer	Sheet 24 of 27

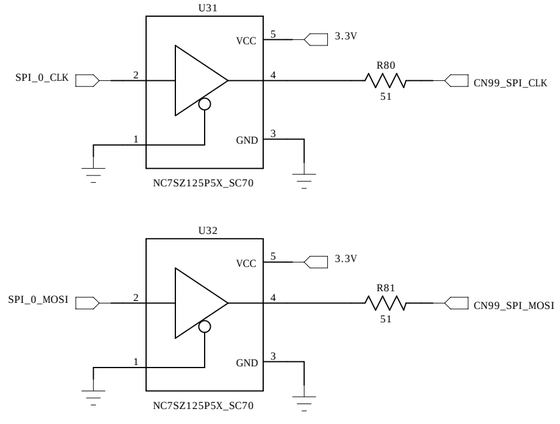
WiFi / Blutooth Radio Module



WiFi 3.6V Regulator

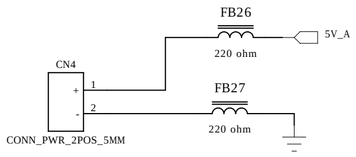


SPI Buffers

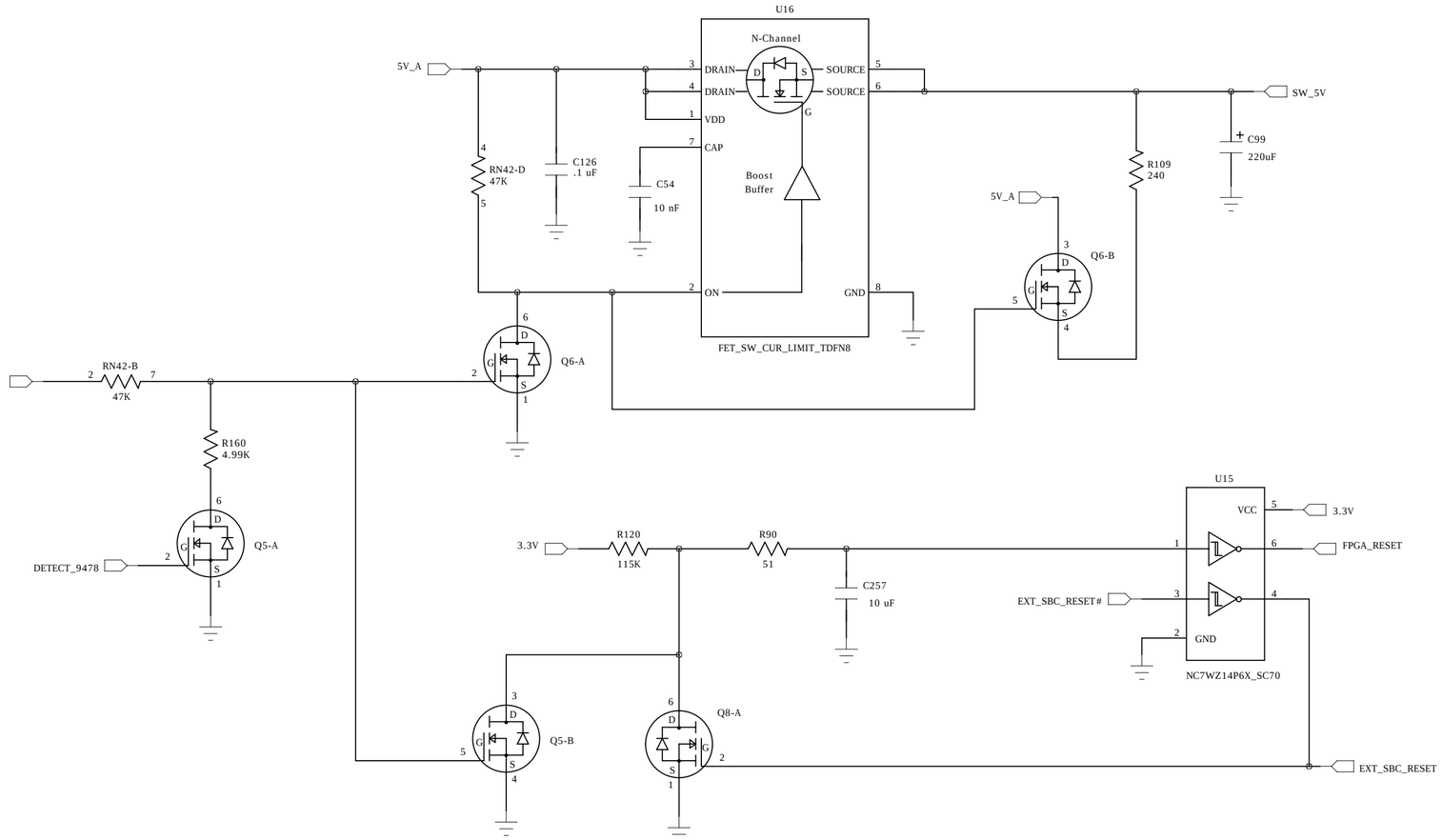


Technologic Systems	Date Jan. 20, 2018	
Title: TS-7800-V2		
Rev: A	Designer	Sheet 25 of 27

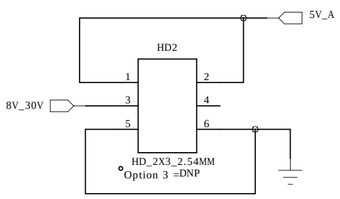
5V Power In

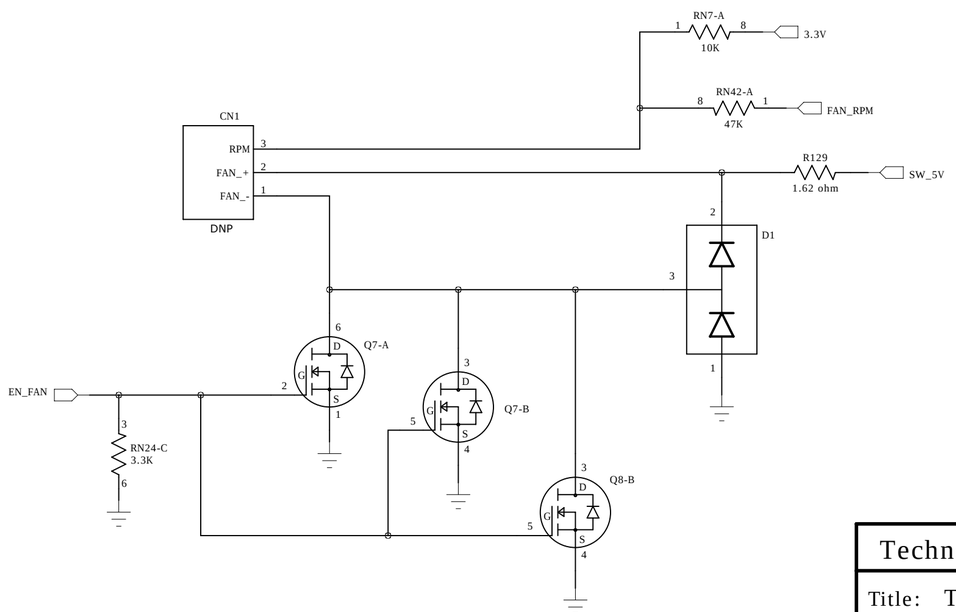


Main 5V Power Sw.



Interface to TS-781 Buck Reg.
For Optional 8V-28V Power In





Technologic Systems	Date Jan. 20, 2018	
Title: TS-7800-V2		
Rev: A	Designer	Sheet 26 of 27

USB Device Port and SiLab uC

USB Device Micro Port

R136 10.7K: 3.3V → AN_3.3V
R137 10.7K

U22 SiLabs

USB: USB_SILAB_P → USB_DP (4); USB_SILAB_M → USB_DM (5); USB_5V_DET → USB_VBUS (8)

PWR_IN (7) ← FB6 600 ohm ← D4 (3) ← 5V_A (1)
C149 .1 uF; C255 10 uF
SILAB_4.7V

R131 1.62 ohm; FB9 600 ohm

USB_5V_DET → RN18-D (5, 4) 2.2K → R148 10.7K

CN12 Micro B: 1 5V, 2 D-, 3 D+, 4 SENSE, 5 GND, FRM 9/8/7/6
USB_SILAB_M → D-; USB_SILAB_P → D+
CONN_USB_MICRO-B_RA

TVS12: 1, 6, 2, 5 SILAB_4.7V, 3, 4 MON_SYS_RESET#
TVS_USB2_NUP4114_SC88

SILAB_3.3V → R122 42.2K → PWR_IN

SILAB_3.3V → R39 14.7K → RN11-D (4, 5) 10K → DIO_04
DIO_04 can be Wakeup

I2C: I2C_0_DAT, I2C_0_CLK

8V_30V → R127 287K → R37 14.7K
Scale = 5.3%

5V_A → R121 42.2K → R30 36.5K
Scale = 44%

A/D

ADC_4 → R138 10.7K → R140 10.7K
AN_3.3V
ADC_2 → R139 10.7K → R141 10.7K
AN_ADC_3
ADC_1 → R142 10.7K → R143 10.7K
ADC_0 → R144 10.7K → R145 10.7K
ADC_3 → R146 10.7K → R147 10.7K → AN_ADC_3

SILAB_TXD
UART0_TXD

SILAB_3.3V; SiL_3.3V
C125 .1 uF; C254 10 uF
RN18-A (1, 8) 2.2K

C193 .1 uF; C253 10 uF
R73 475
U40 (2, 1, 3)

Q4-B (3 D, G, 5, S 4)
RN26-D (4, 5) 3.3K

SILAB_C8051F381_QFN32

MON_SYS_RESET# → RN11-A (1, 8) 10K → RN11-B (7, 2) 10K → SYS_RESET#

RN18-C (3, 6) 2.2K

A/D full scale = 2.50V

SiLab LED

EN_SILAB_LED → R101 240 → LED3 (2, 1) SiLab Green

5 Channel 10-bit A/D - 5V full scale

HD4 (2, 4, 6, 8, 10 / 1, 3, 5, 7, 9)
ADC_0
ADC_1
ADC_2
ADC_3
ADC_4

Technologic Systems	Date Jan. 20, 2018	
Title: TS-7800-V2		
Rev: A	Designer	Sheet 27 of 27