# TS-7800-V2 Standard Options

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Option 1</td>
<td>TS-7800-V2-DMN1I Marvell Armada 385 1.33 GHz ARM Cortex A9 1G DDR3 RAM, 4GB eMMC Flash, Temp Sensor, Real Time Clock, Full-Duplex RS-485(-40C to 85C)</td>
</tr>
<tr>
<td>Option 2</td>
<td>TS-7800-V2-DMN2I Marvell Armada 385 1.33 GHz ARM Cortex A9 1G DDR3 RAM and 4GB eMMC Flash, WiFi, Temp Sensor, Real Time Clock, Full-Duplex RS-485(-40C to 85C)</td>
</tr>
<tr>
<td>Option 3</td>
<td>TS-7800-V2-DMN3I Marvell Armada 385 1.33 GHz ARM Cortex A9 1G DDR3 RAM, 4GB eMMC Flash, mPCIe, WiFi, Accelerometer, Temp Sensor, RTC, Full-Duplex RS-485(-40C to 85C)</td>
</tr>
</tbody>
</table>

## Optional Components/Features Summary

### WiFi/Bluetooth Option
- **w/ Chip Antenna**
  - U.FL available on request
  - Included only on xxWxx Standard Options
  - ADD: K2 (chip antenna), U37
  - (alternate: U.FL antenna connector)

### CPU Heat Sink
- Included on ALL Standard Options
- **ADD:** Alpha Novatech S08CHL0A

### Available Accessories
- Included on NO Standard Options
- **TS-781 "8-28V Power daughter board"**
  - Compatible ONLY with xxx1x, xxx2x Standard Option

### Rev.P2 --> Rev.A Changes:
- Added new RTC (U41 = M41T00) on I2C bus
- Add PD on MPP_10 (R57) - this disables clocks on MPP_45 and 46
- Removed D7, connected SYS_RESET# to Silab pin 32
- CN44 (Mini-PCIe) pin 22 needs to use DIO (use CPU_TYPE_1)
- Change "CPU_TYPE_1" to be biased low (R46) to indicate Rev.A
- PTP Ethernet timing will not be supported
- Moved SATA Conn (CN10) away from PC/104 Conn 0.3mm
- Made FPGA_RESET longer = 680 ms

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Web Schematic: Some proprietary information has been withheld.
10/100/1000 Marvell 88E1512 PHY

Gig MagJack

Strapped for PHY address = 1
FPGA JTAG

Conn.

Tag-Connect

Cyclone

2 MB

SPI Flash

FPGA

MUX

FPGA_JTAG_TDO
FPGA_JTAG_TDI
FPGA_JTAG_TCK
FPGA_JTAG_TMS
FPGA_FLASH_CS#

MSEL2 high = Fast POR

3.3V
2.5V

3.3V
3.3V
3.3V

FPGA_SPI_CS#
FPGA_SPI_CLK
FPGA_SPI_MOSI
FPGA_SPI_MISO

EXT_SBC_RESET

ALTERA_CYCLONE_IV_EP4CGX22CF19C8N
C145
U4-C

ALTERA_CYCLONE_IV_EP4CGX22CF19C8N
C145
U4-C

ALTERA_CYCLONE_IV_EP4CGX22CF19C8N
C145
U4-C

ALTERA_CYCLONE_IV_EP4CGX22CF19C8N
C145
U4-C

ALTERA_CYCLONE_IV_EP4CGX22CF19C8N
C145
U4-C

ALTERA_CYCLONE_IV_EP4CGX22CF19C8N
C145
U4-C

ALTERA_CYCLONE_IV_EP4CGX22CF19C8N
C145
U4-C

ALTERA_CYCLONE_IV_EP4CGX22CF19C8N
C145
U4-C

ALTERA_CYCLONE_IV_EP4CGX22CF19C8N
C145
U4-C

ALTERA_CYCLONE_IV_EP4CGX22CF19C8N
C145
U4-C
PC/104  64-pin Connector

Warning:
All IRQs and data lines are 5V tolerant, but all other signals must use 3.3V levels.
IRQ3 and 4 must be 3.3V levels.

FETs provide 5V tolerance

PC/104  40-pin Connector

29 lines directly into FPGA (bi-directional)
IRQ1 thru IRQ15 are read only
**LCD Port**

LCD03, LCD05, LCD06 init to inputs when outputs, active high-low
These are programmable I/O

All LCD lines are 5V tolerant

LCD07 thru LCD14 are always open drain outputs, initialized to high
They can be used as inputs

LCD04 is always output active high-low, init to zero
These are programmable I/O

All LCD lines are 5V tolerant

**Option Res. Straps**

4 Res. Straps for Board Config

Pull-up resistors for the open drain outputs

Open drain outputs can sink 8 mA, but only source current thru resistor

**Resistor Strapping Table**

<table>
<thead>
<tr>
<th>R42</th>
<th>R45</th>
<th>R44</th>
<th>R43</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

1 = POP, 0 = DNP

**SiLab SR**

Shift Reg + Latch

**CPU Straps**

Res. Straps

Option

Indicates Rev.A

CPU Speeds

SPREAD SPECTRUM#
DIO Port

All DIO lines are 5V tolerant

CAN Transceiver

provides 5V tolerance
7mm Stack Height
to center of bd.

SATA 0

SATA 1
5V Power In

Main 5V Power Sw.

Interface to TS-781 Buck Reg.
For Optional 8V-28V Power In

Technologic Systems

Title: TS-7800-V2
Rev: A
Date: Jan. 20, 2018
Sheet 26 of 27
USB Device Port and SiLab uC

A/D full scale = 2.50V

5 Channel 10-bit A/D - 5V full scale

DIO_04 can be Wakeup