

TS-7970 Standard Options

| | | |
|----------|-----------------------------------|---------------------------------------------------------------------------------------------------------------|
| Option 1 | TS-7970-1G-4GF-S8S-RTC-I | Solo 800MHz i.MX6 CPU, 1GB RAM, 4GB eMMC, 1x GbETH, BB-RTC (-40 to 85) |
| Option 2 | TS-7970-2G-4GF-Q10S-RTC-E | Quad 1GHz i.MX6 CPU, 2GB RAM, 4GB eMMC, 1x GbETH, BB-RTC, (-20 to 70) |
| Option 3 | TS-7970-1G-4GF-S8S-RTC-CP-WIFI-I | Solo 800MHz i.MX6 CPU, 1GB RAM, 4GB eMMC, BB-RTC, 2x GbETH, Audio In/Out, USB Mini-Card, WiFi/BT, (-40 to 85) |
| Option 4 | TS-7970-2G-4GF-Q10S-RTC-CP-WIFI-E | Quad 1GHz i.MX6 CPU, 2GB RAM, 4GB eMMC, BB-RTC, 2x GbETH, Audio In/Out, mSATA/Mini-Card, WiFi/BT, (-20 to 70) |

Options Overview:

CPU can be Quad or Single ITemp
 U22 and U24 (RAM) not pop on Single core
 K1 (WiFi module) is on the WIFI models
 Mini-Card Connector (J3) has a USB interface & is on CP models
 mSATA support on this connector with Quad only
 SIM Card connector not included in standard options
 PEM Mounts provided with Mini-Card Connector
 No I2C on this interface
 2nd Ethernet (U32 & T2) is on the CPU's PCIe port on CP Models
 Audio (U30 & J7) is on the CP Models
 Gyro (U17) is not populated for any model
 Standard SATA Connector is not populated for any model

All 4 iMX6 UARTs MUXed thru FPGA
 Features that require UART:

2 RS-232 Ports
 2 RS-485 Ports
 1 TTL UART to HD1
 1 UART for BlueTooth

Heat Sink for CPU

Excel Cell Electronic # A1404036

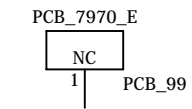
Resistor Strapping Table

| R39 | R37 | R36 | R34 | | |
|-----|-----|-----|-----|----------|-----------------------------------|
| 0 | 0 | 0 | 1 | Option 1 | TS-7970-1G-4GF-S8S-RTC-I |
| 0 | 0 | 1 | 0 | Option 2 | TS-7970-2G-4GF-Q10S-RTC-E |
| 0 | 0 | 1 | 1 | Option 3 | TS-7970-1G-4GF-S8S-RTC-CP-WIFI-I |
| 0 | 1 | 0 | 0 | Option 4 | TS-7970-2G-4GF-Q10S-RTC-CP-WIFI-E |
| 1 | 1 | 1 | 1 | Reserved | |

0=DNP, 1=POP

| | | | |
|-------------------------|----------|-------|---------------|
| Technologic Systems | | Date | Dec. 27, 2016 |
| Title: TS-7970 iMX6 SBC | | | |
| Rev: E | Designer | Sheet | 2 of 27 |

TS-7970 Revisions



Rev.C was never built

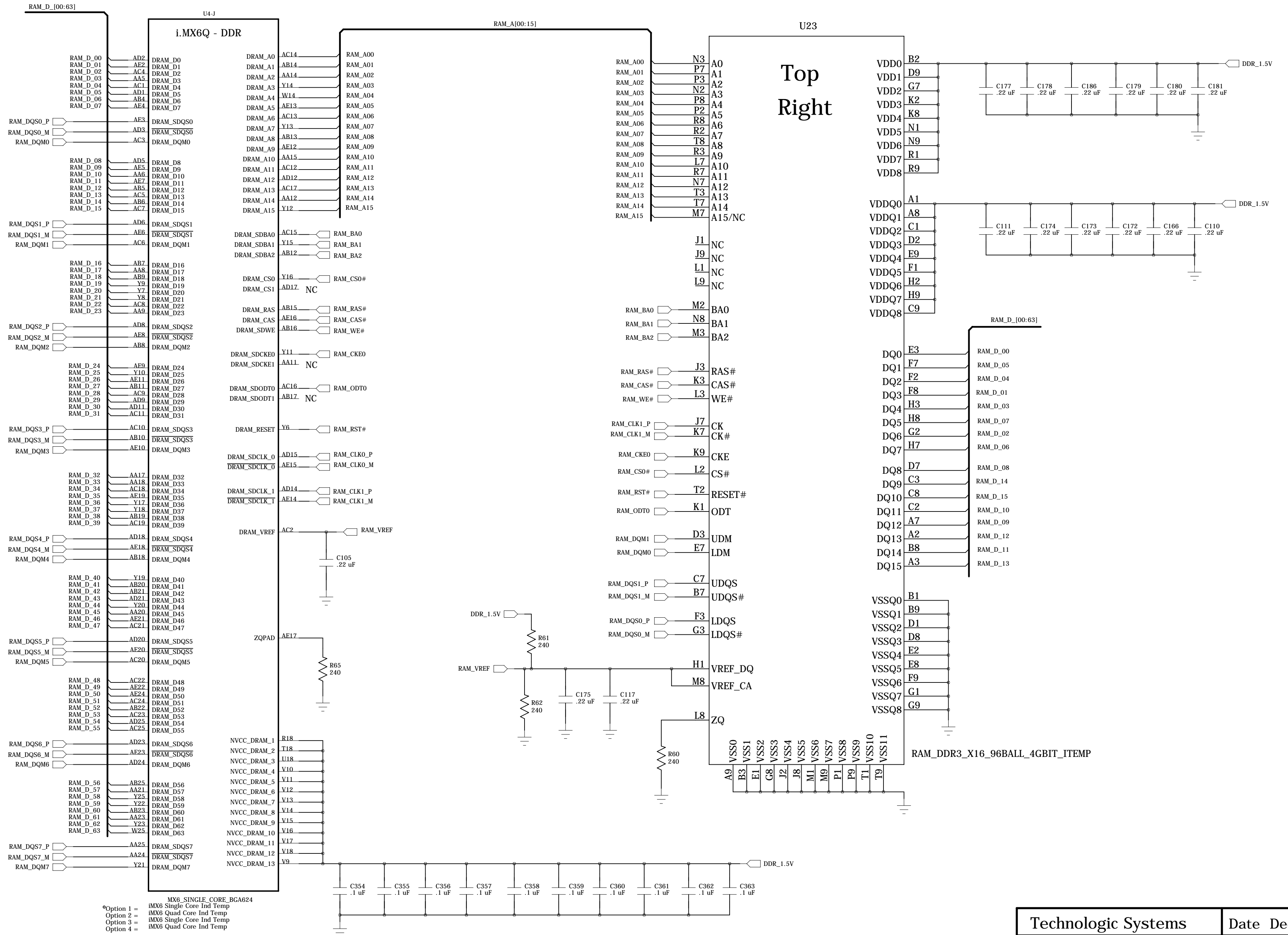
Rev.B to D Changes

Changed Eth PHY to Marvell
Changed Magjack (T1) to one with separate CT
Added Q17 to improve PHY reset
Added two lane MIPI connector (CN1)
Change RTC battery holder to smaller one
When Console Jumper off, pull USB_5V_DETECT low
Added PUSH_SW# signal to HD1
allows SiLab wake-up via header

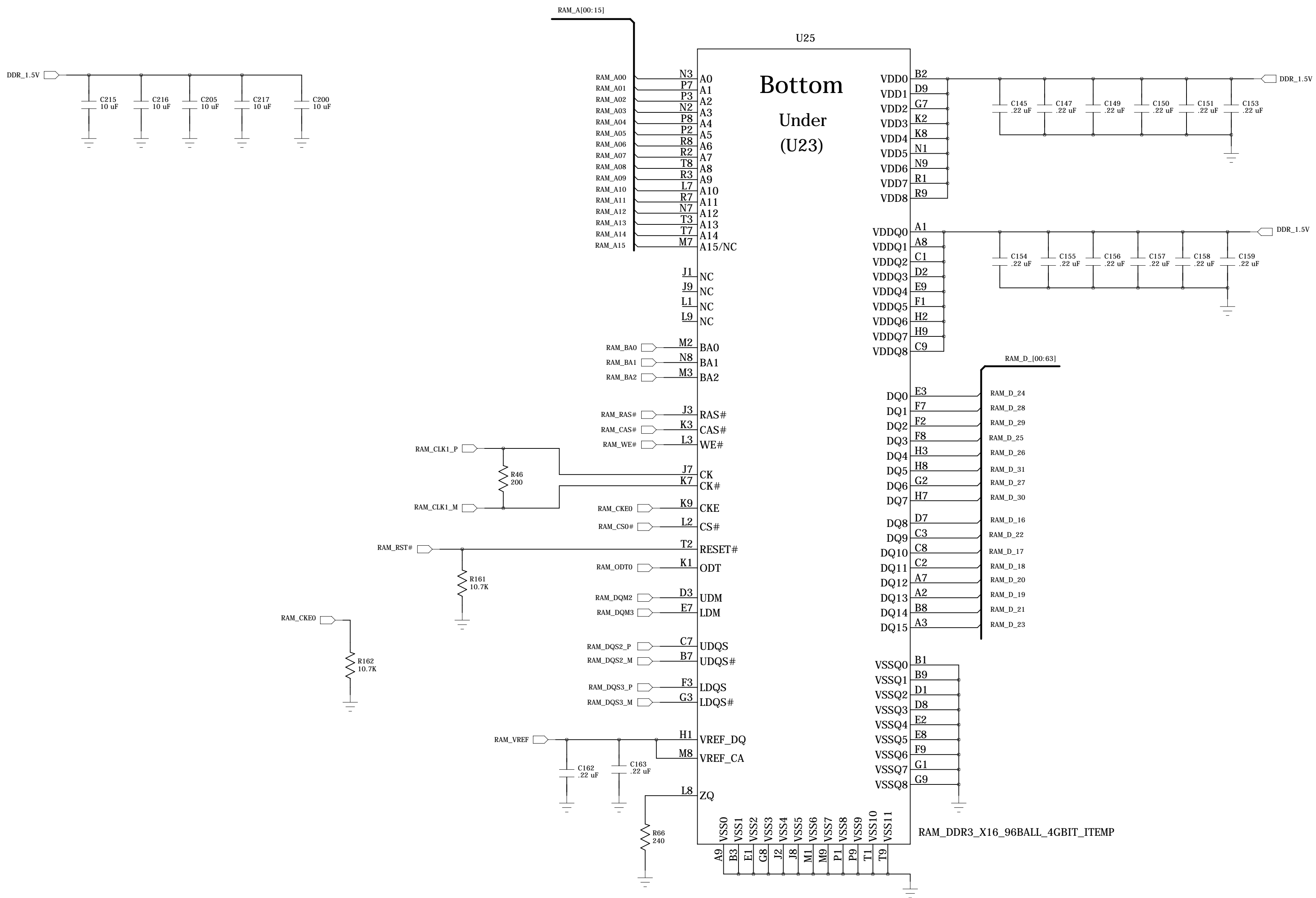
Improved CN99 (Factory Programming Interface)
Removed 1.2V Reg (used by Micrel PHY)
Added optional Xtal Osc (X1) for PHYs

Rev.E Changes:

Added TVS10-13 for RS-485
Updated Factory Programming Interface

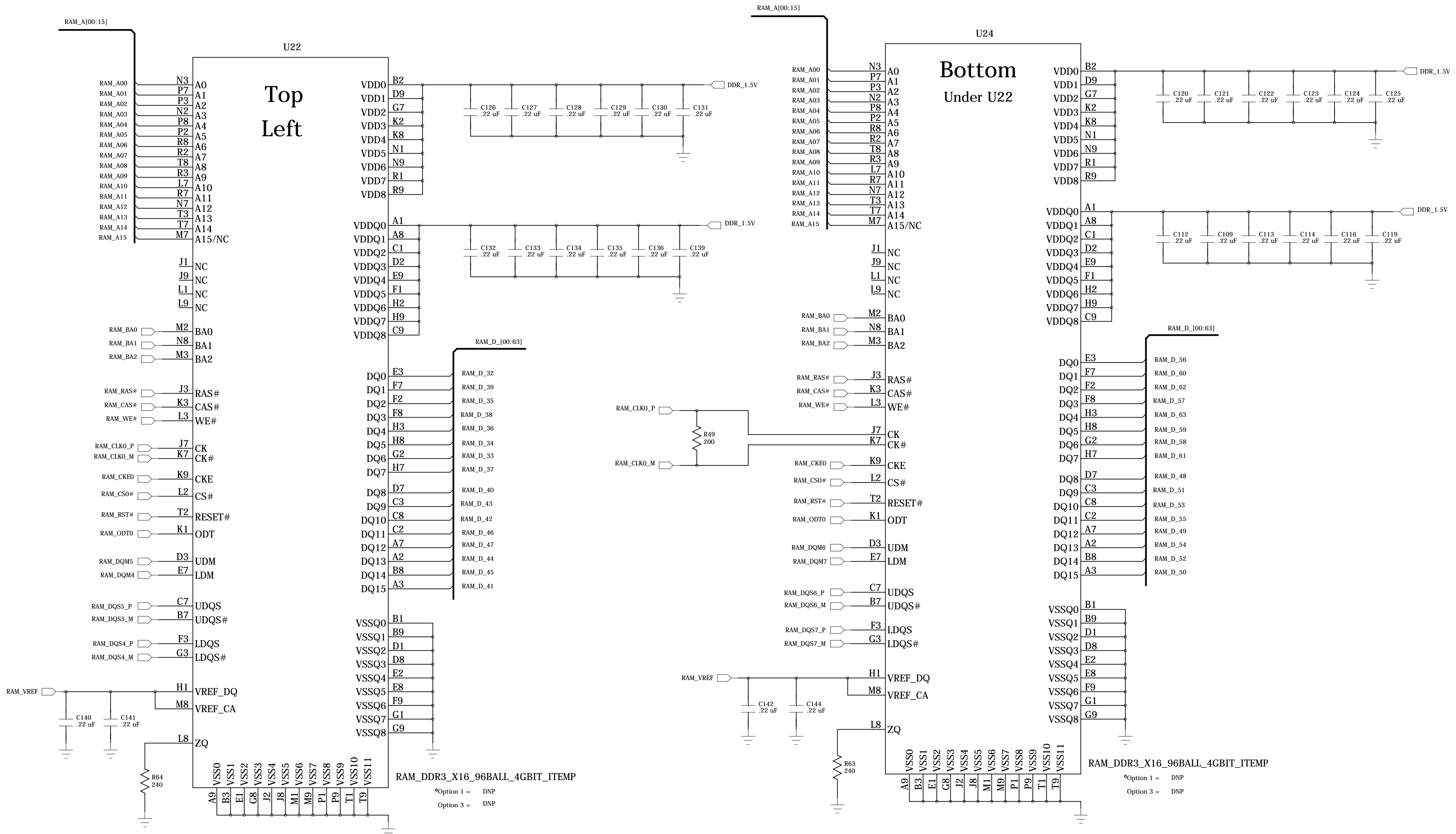


MX6_SINGLE_CORE_BGA624
 Option 1 = iMX6 Single Core Ind Temp
 Option 2 = iMX6 Quad Core Ind Temp
 Option 3 = iMX6 Single Core Ind Temp
 Option 4 = iMX6 Quad Core Ind Temp



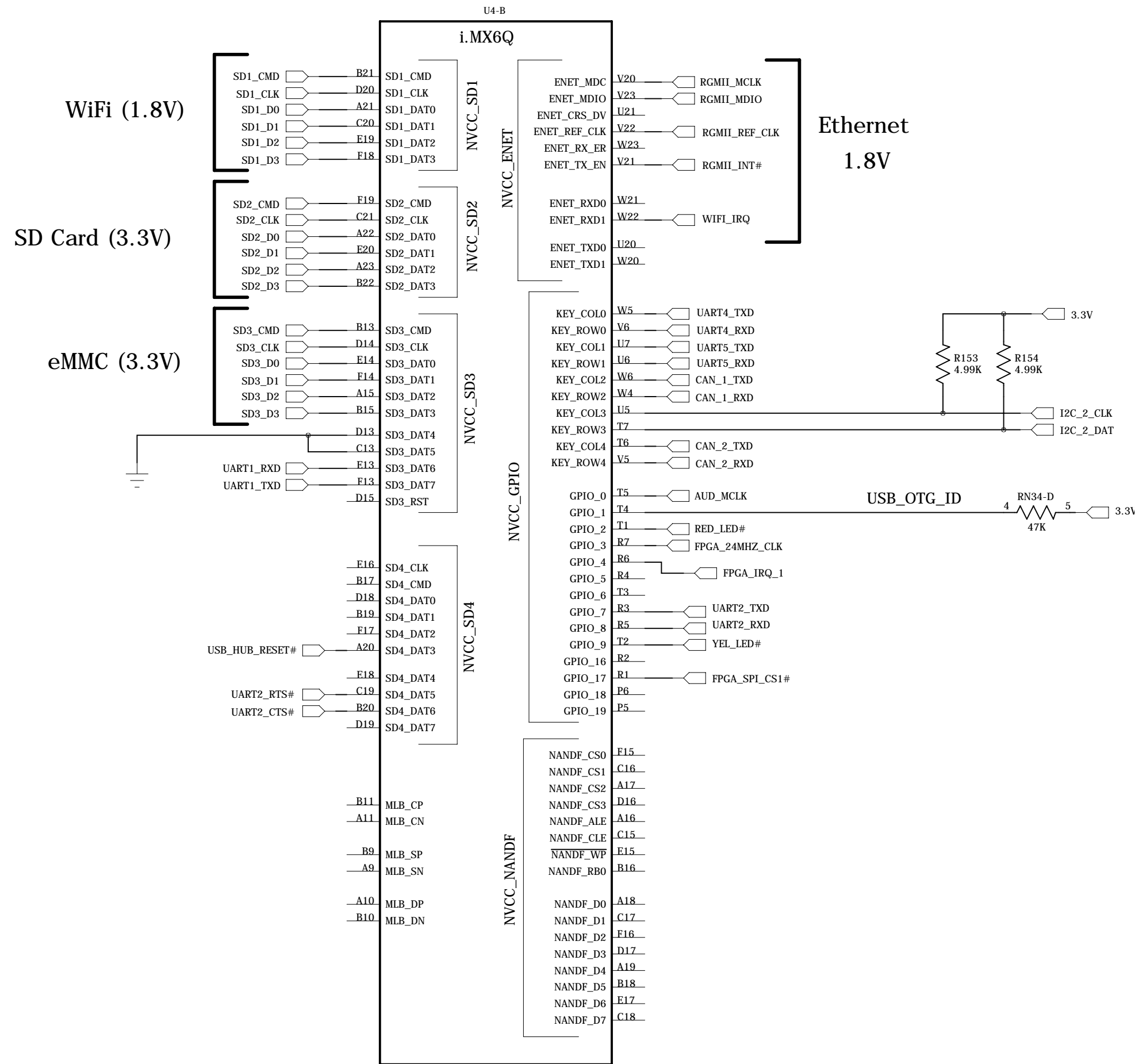
RAM Data bits 32-63

Not populated for Single Core CPU

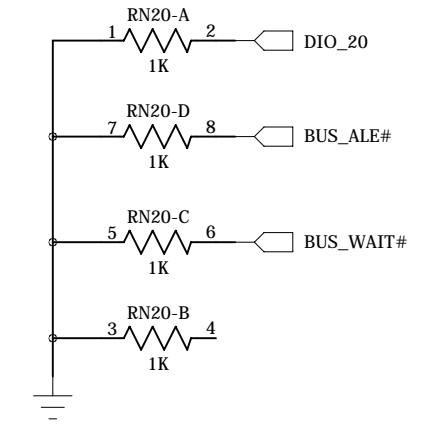
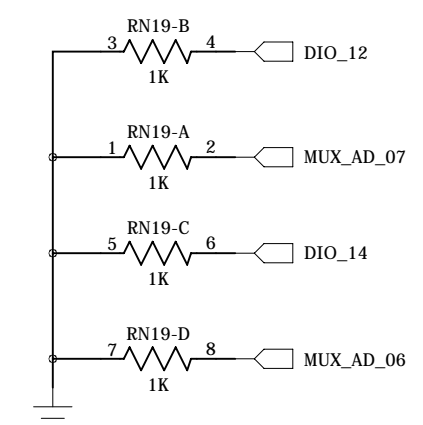
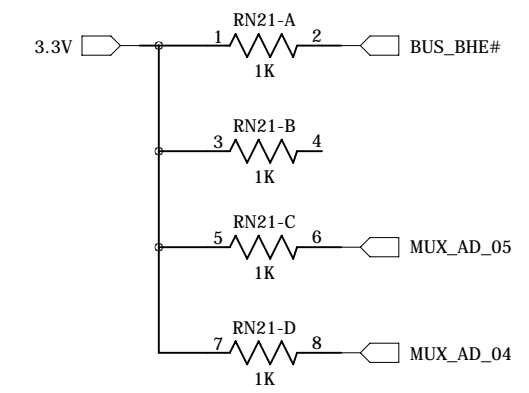


SD, GPIO, NAND

Bias Res.



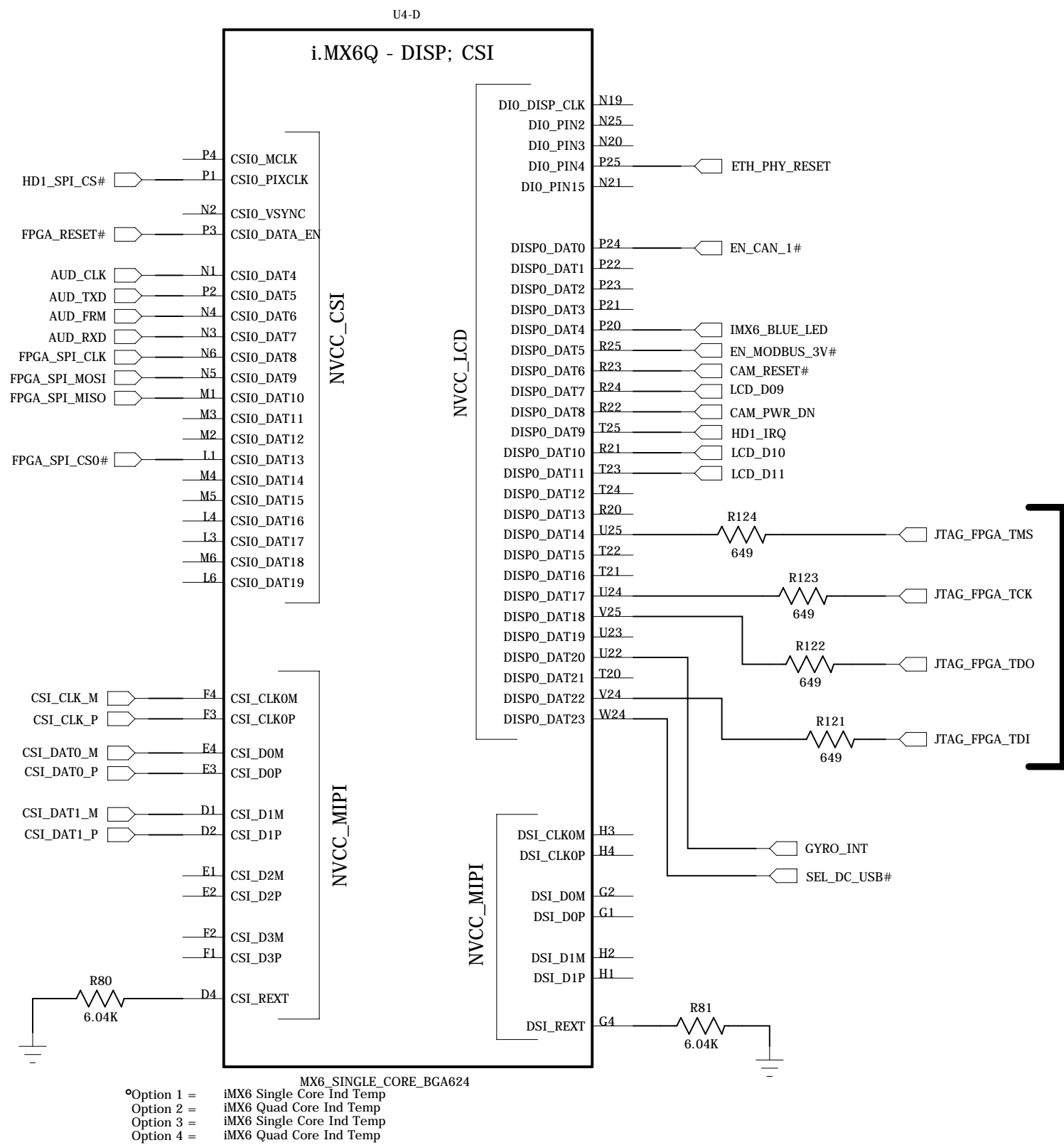
MX6_SINGLE_CORE_BGA624
 Option 1 = iMX6 Single Core Ind Temp
 Option 2 = iMX6 Quad Core Ind Temp
 Option 3 = iMX6 Single Core Ind Temp
 Option 4 = iMX6 Quad Core Ind Temp



4 PWM total

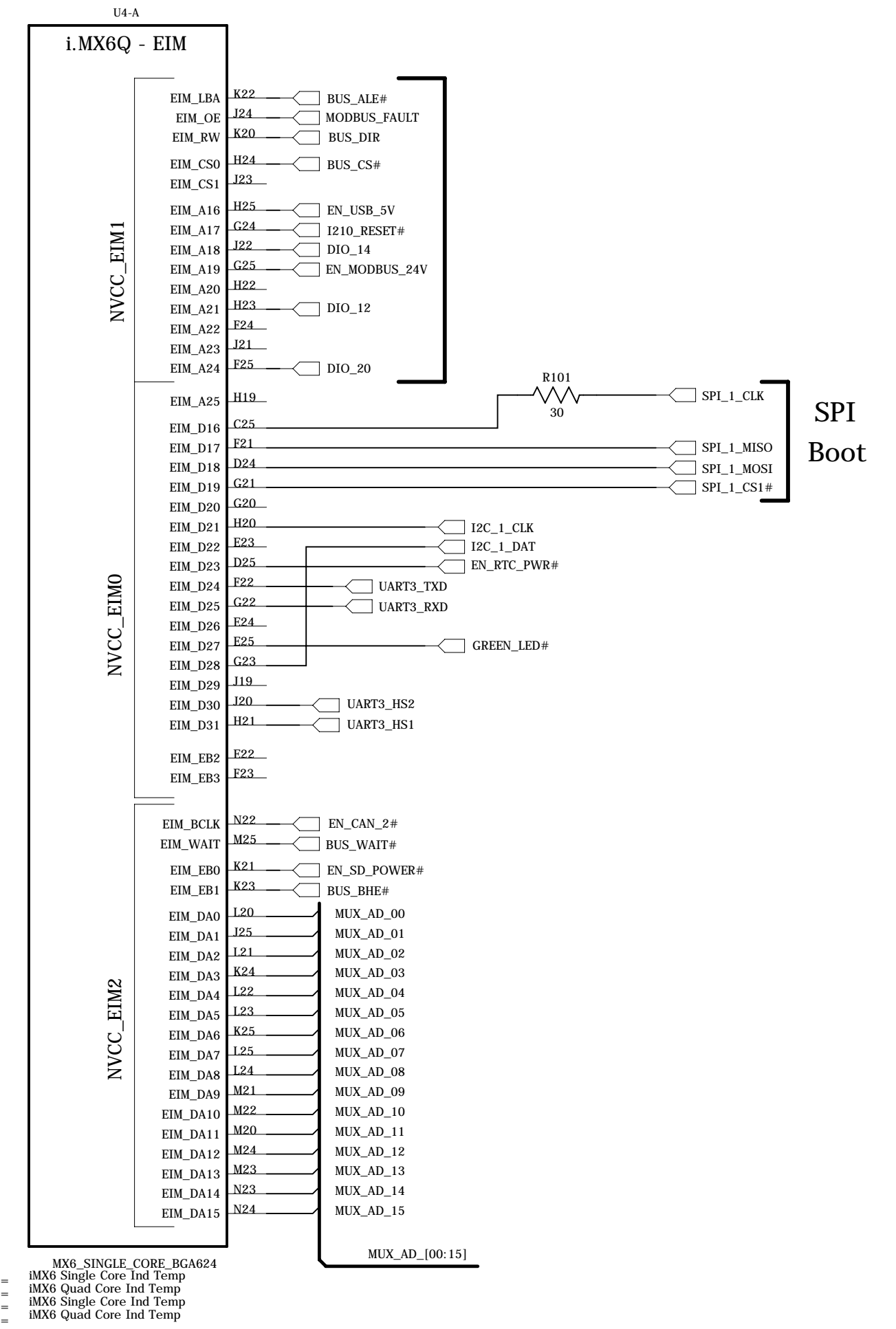
PWM on SD4_DAT 1 or 2
 GPIO_1 and GPIO_9

LCD



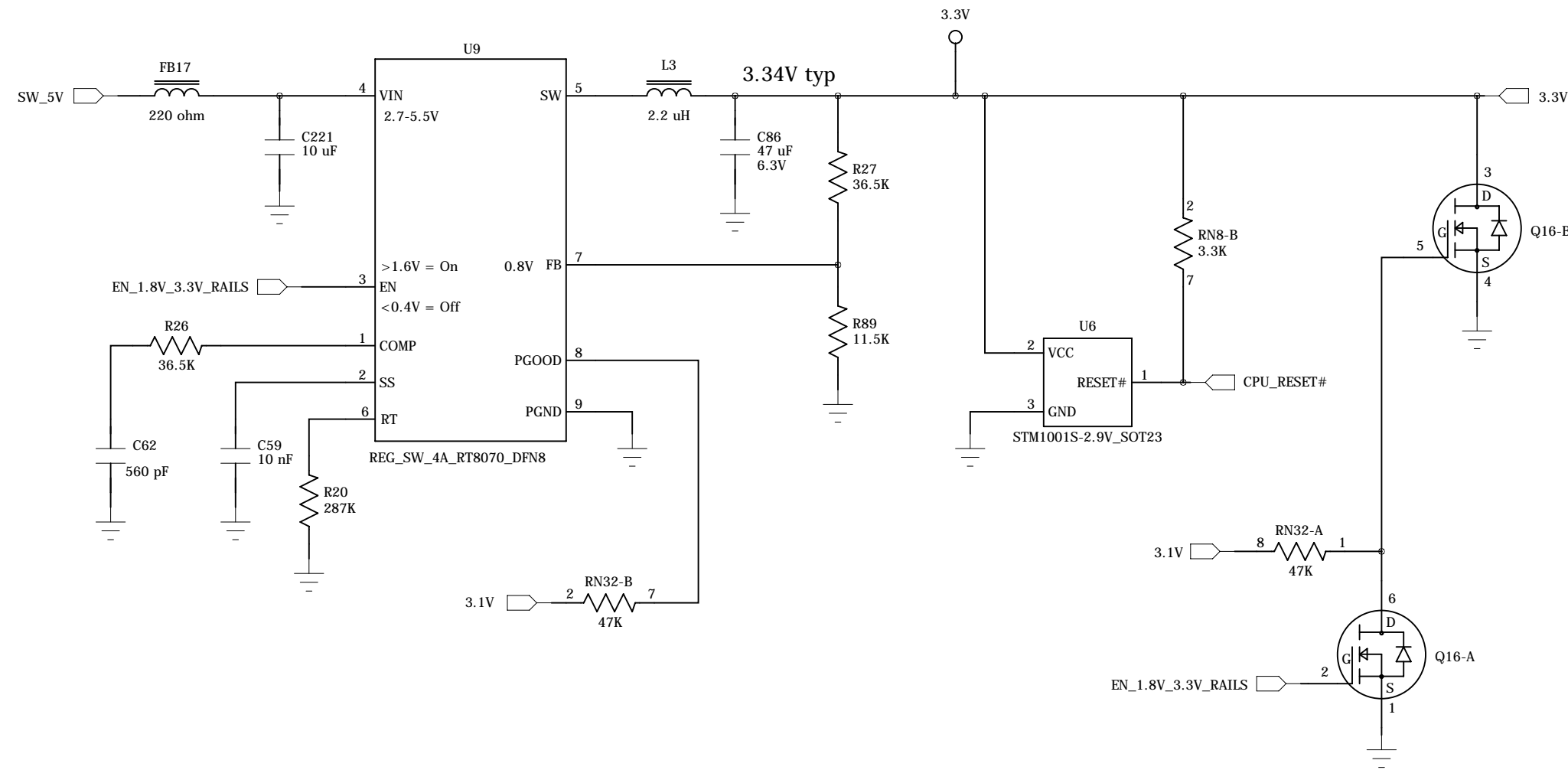
Allows MX6 to program FPGA

EIM

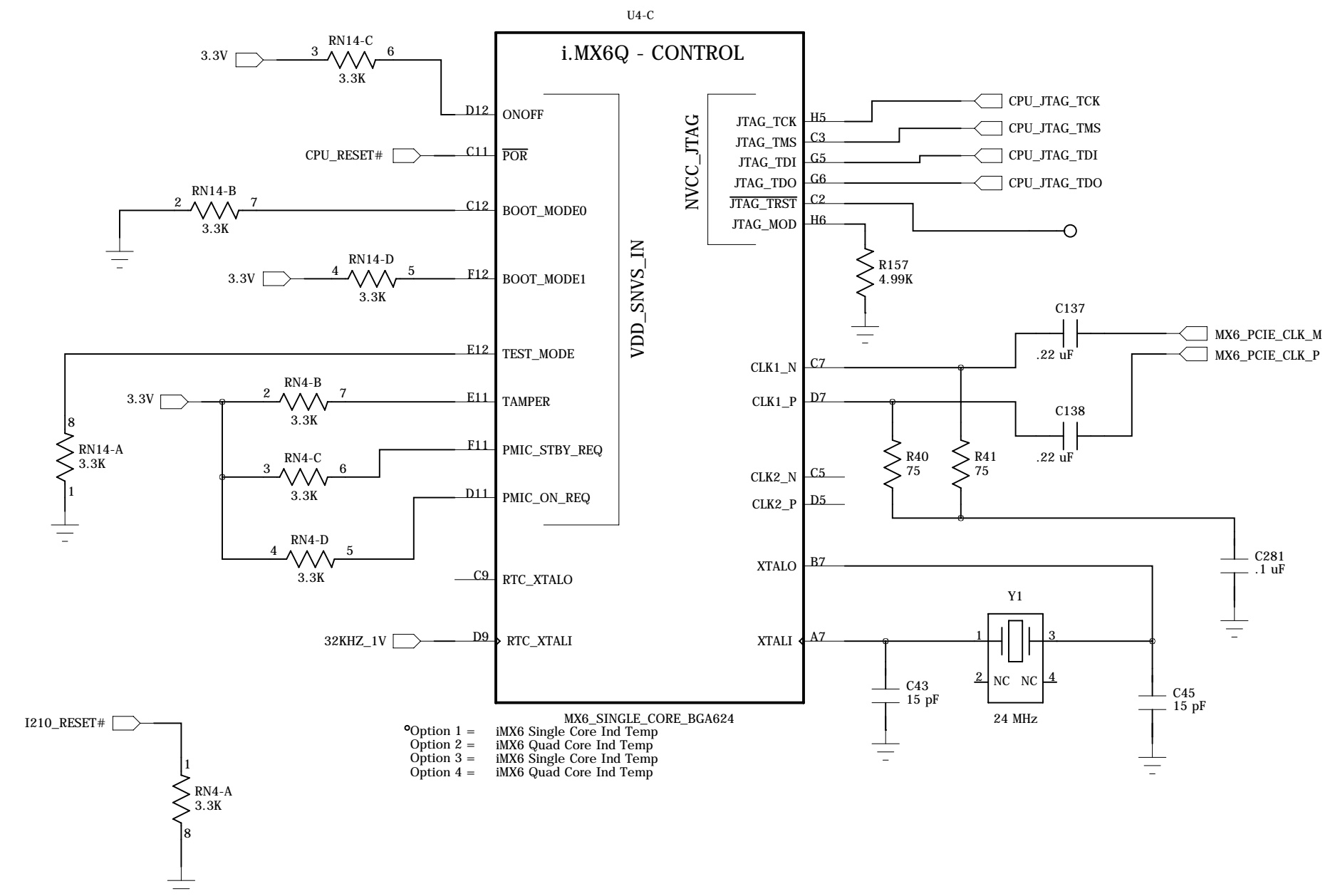


SPI Boot

3.3V Reg. #5



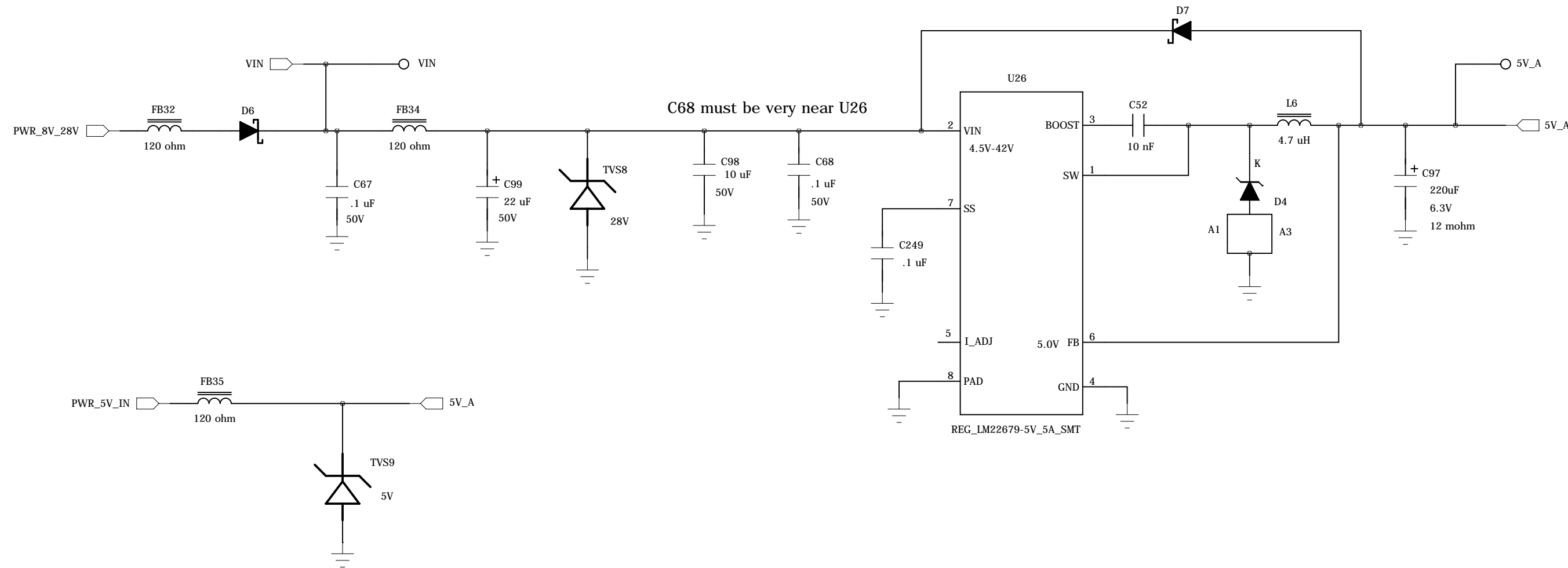
CPU Control



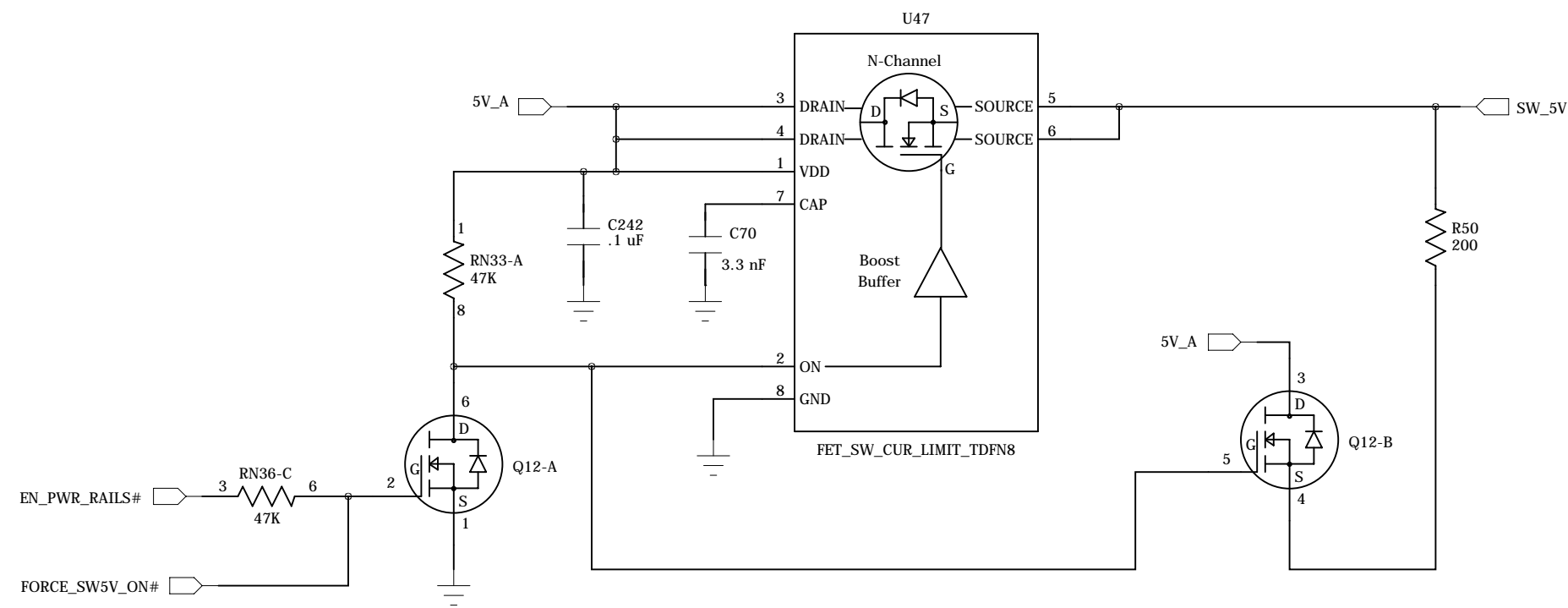
MX6_SINGLE_CORE_BGA624
 *Option 1 = iMX6 Single Core Ind Temp
 *Option 2 = iMX6 Quad Core Ind Temp
 *Option 3 = iMX6 Single Core Ind Temp
 *Option 4 = iMX6 Quad Core Ind Temp

5V Power Supply (5A)

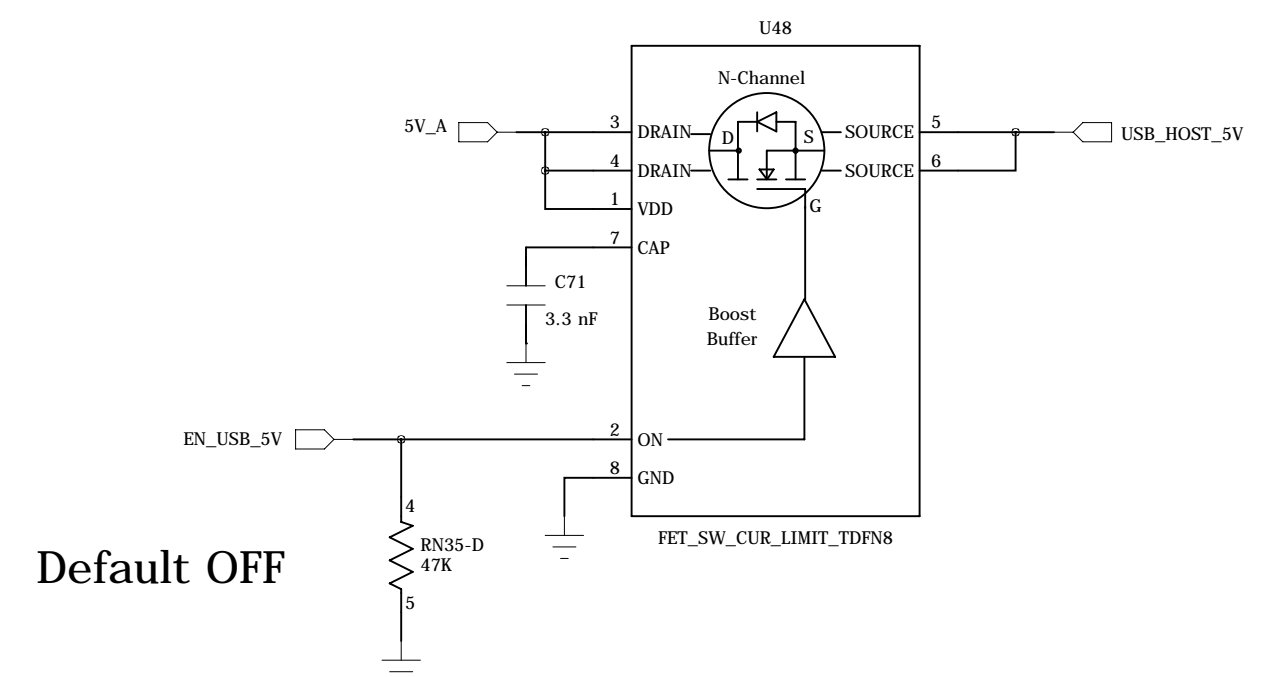
8-28 VDC
Power Input



Main 5V Power Sw.

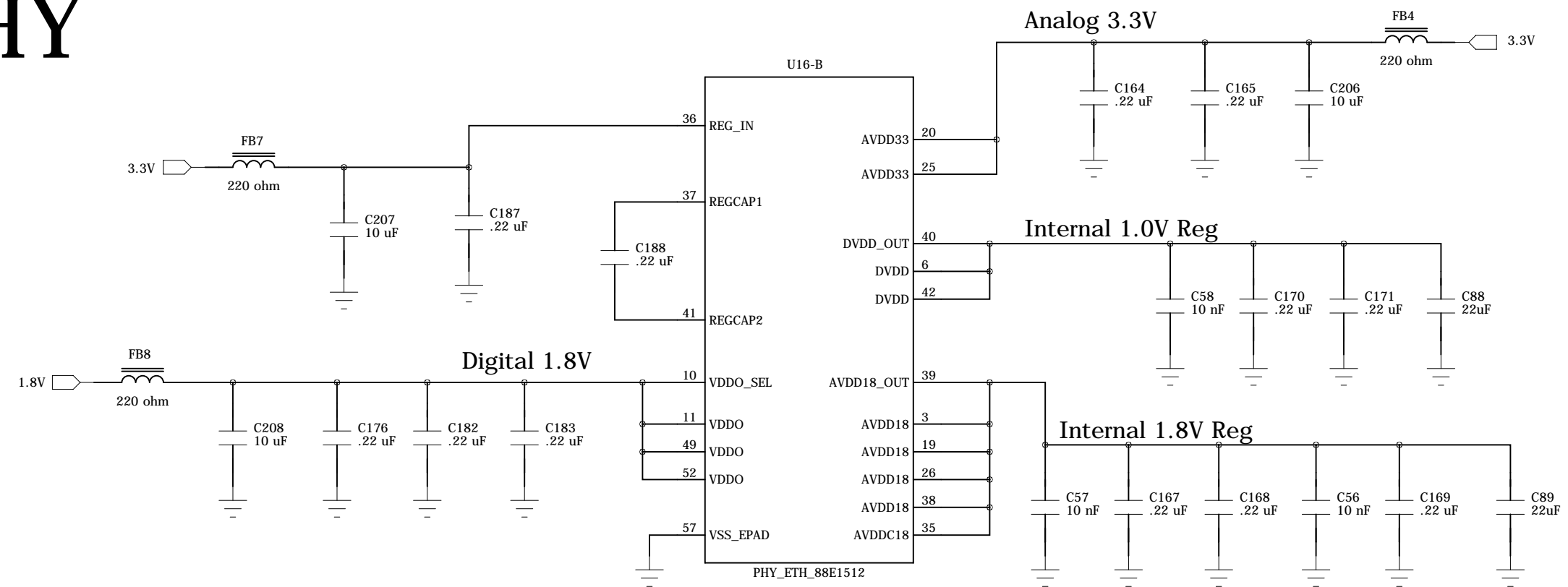


USB Sw. 5V

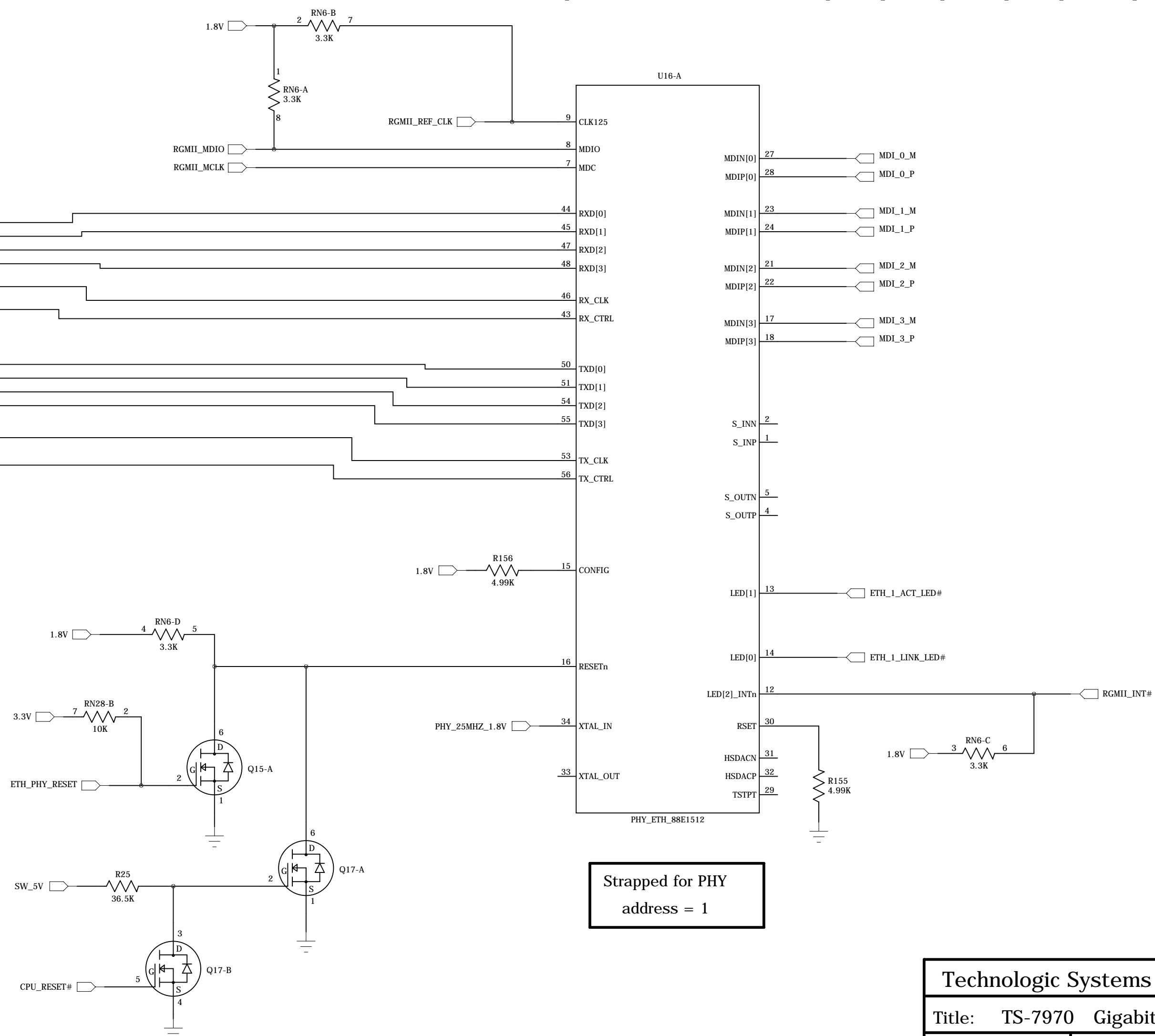
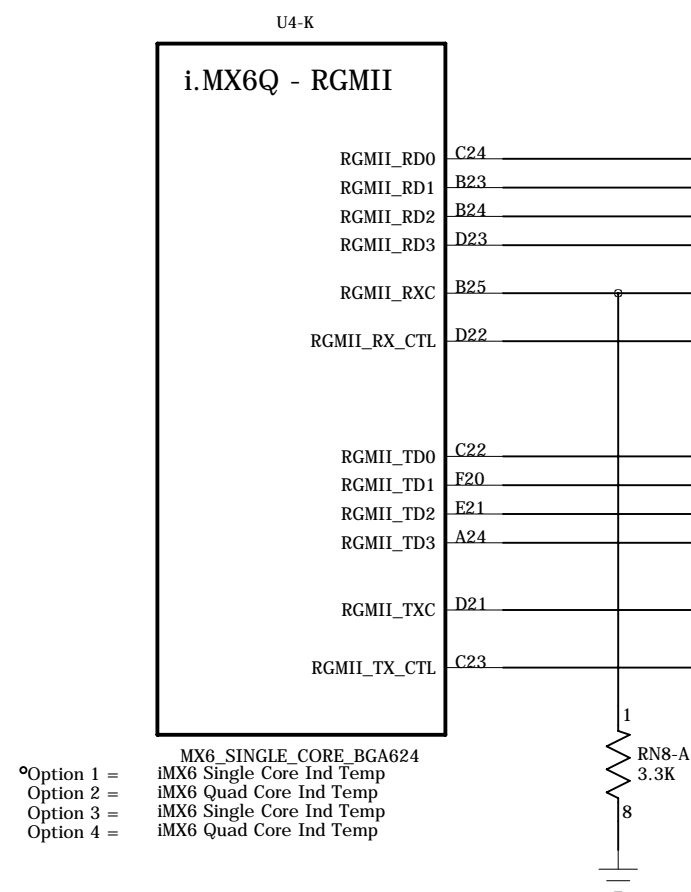


| | |
|----------------------------------------|--------------------|
| Technologic Systems | Date Dec. 27, 2016 |
| Title: TS-7970 5V Reg and Pwr Switches | |
| Rev: E | Designer |
| Sheet 11 of 27 | |

10/100/1000 Marvell PHY



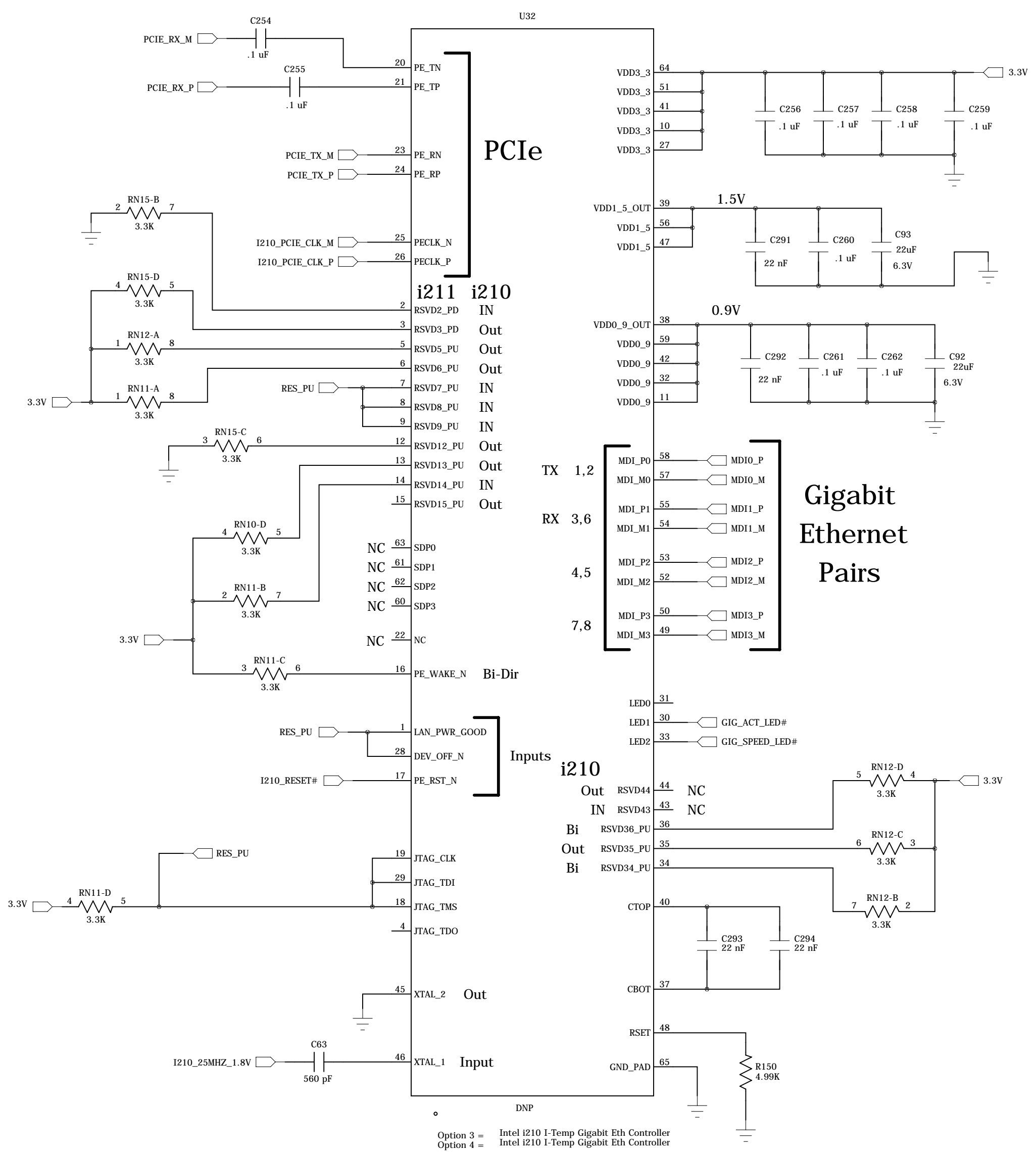
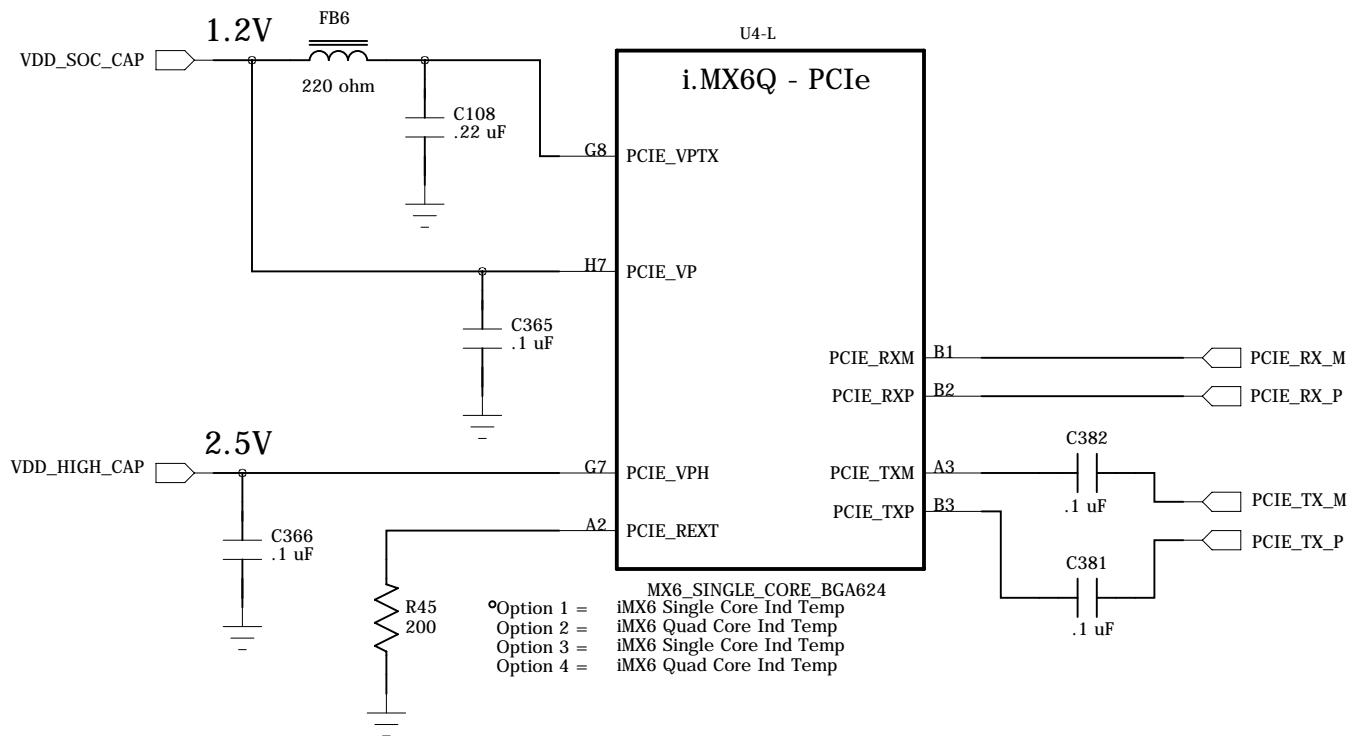
CPU ETH1



| | |
|-------------------------------------|-----------------------------|
| Technologic Systems | Date Dec. 27, 2016 |
| Title: TS-7970 Gigabit Ethernet PHY | |
| Rev: E | Designer RLM Sheet 12 of 27 |

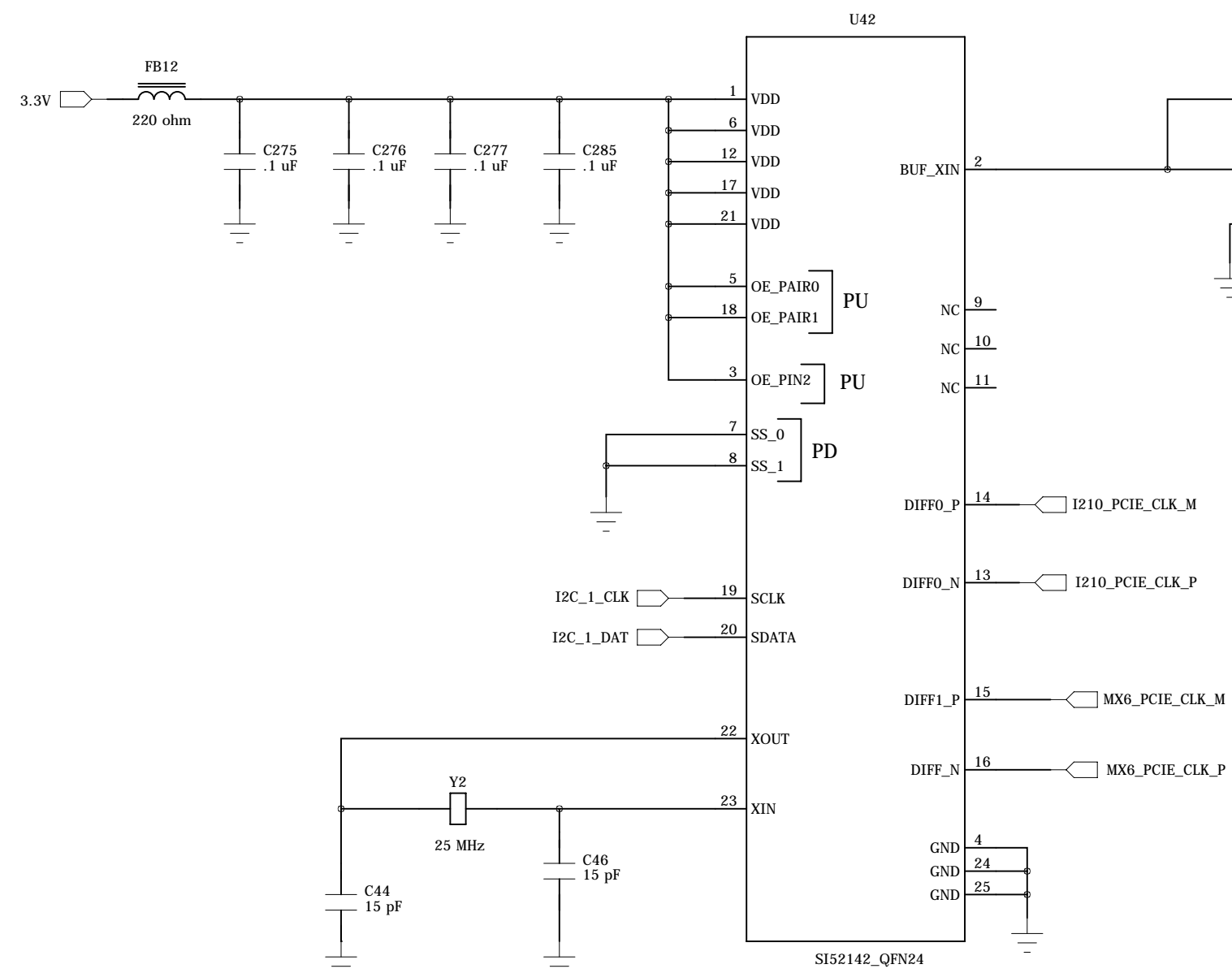
Gigabit Ethernet Controller

CPU PCIe

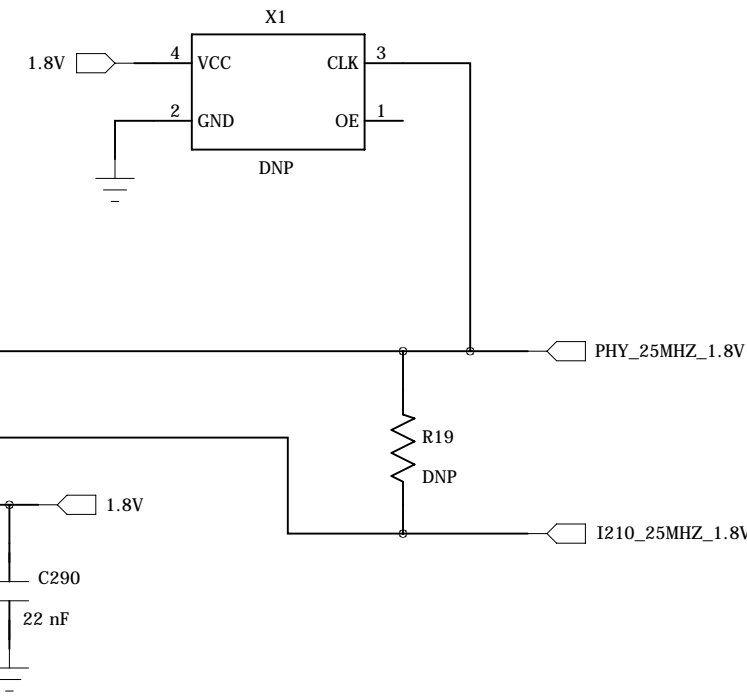


MDIX supported in 10/100 modes

PCIe 100 MHz Clock Generator

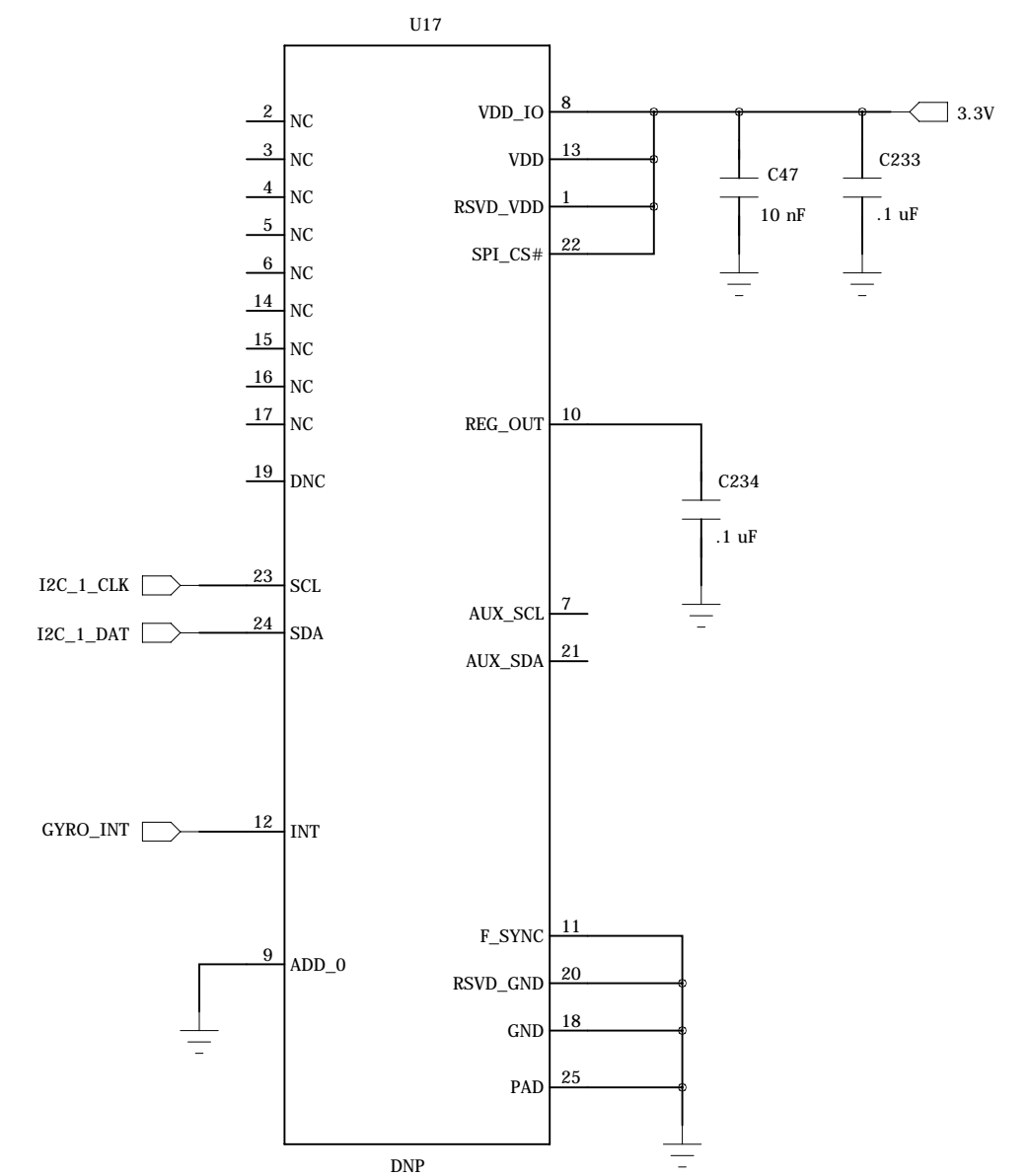


Level Shifter

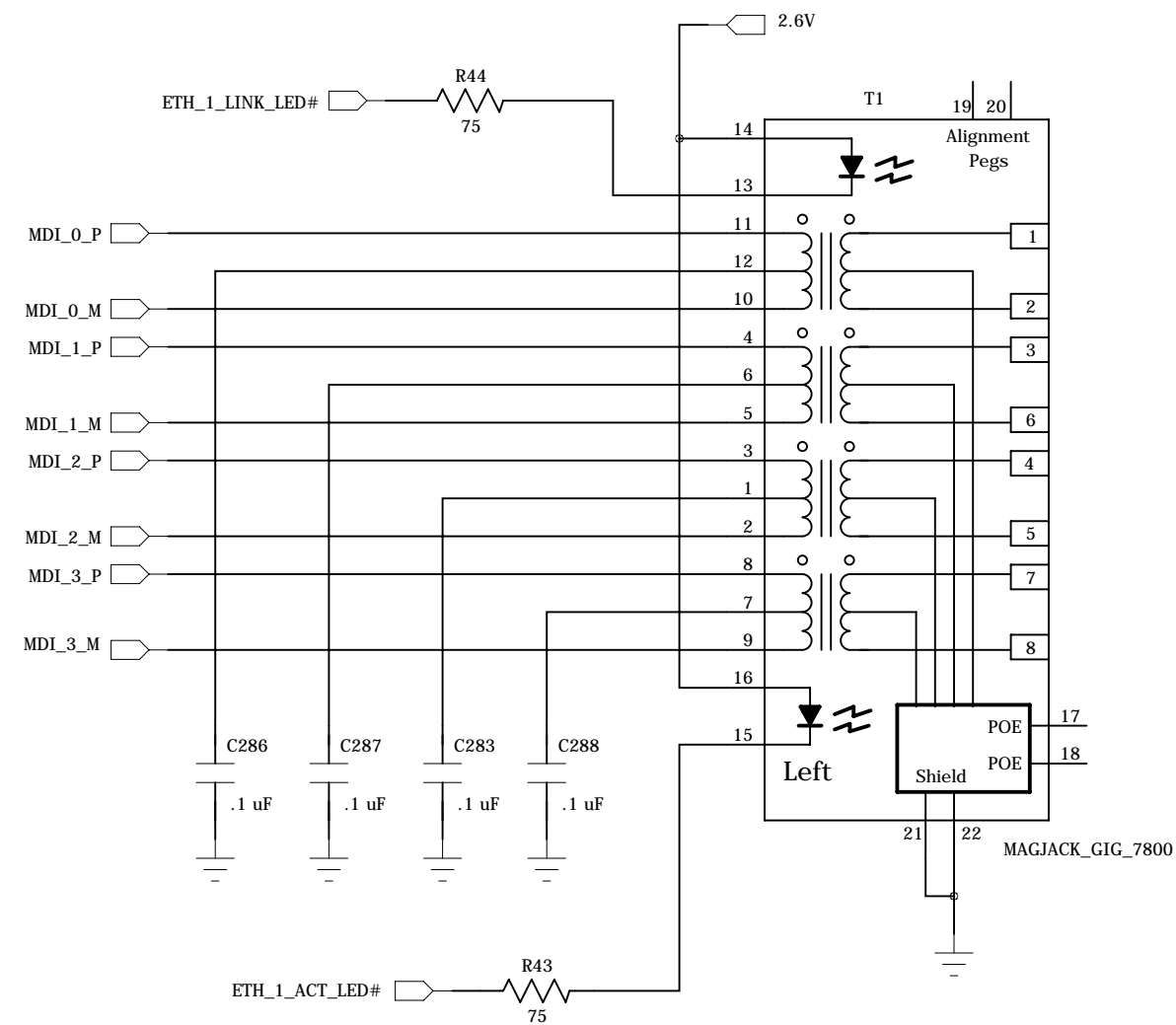


Gyro-Accelerometer

Option not populated on any standard models

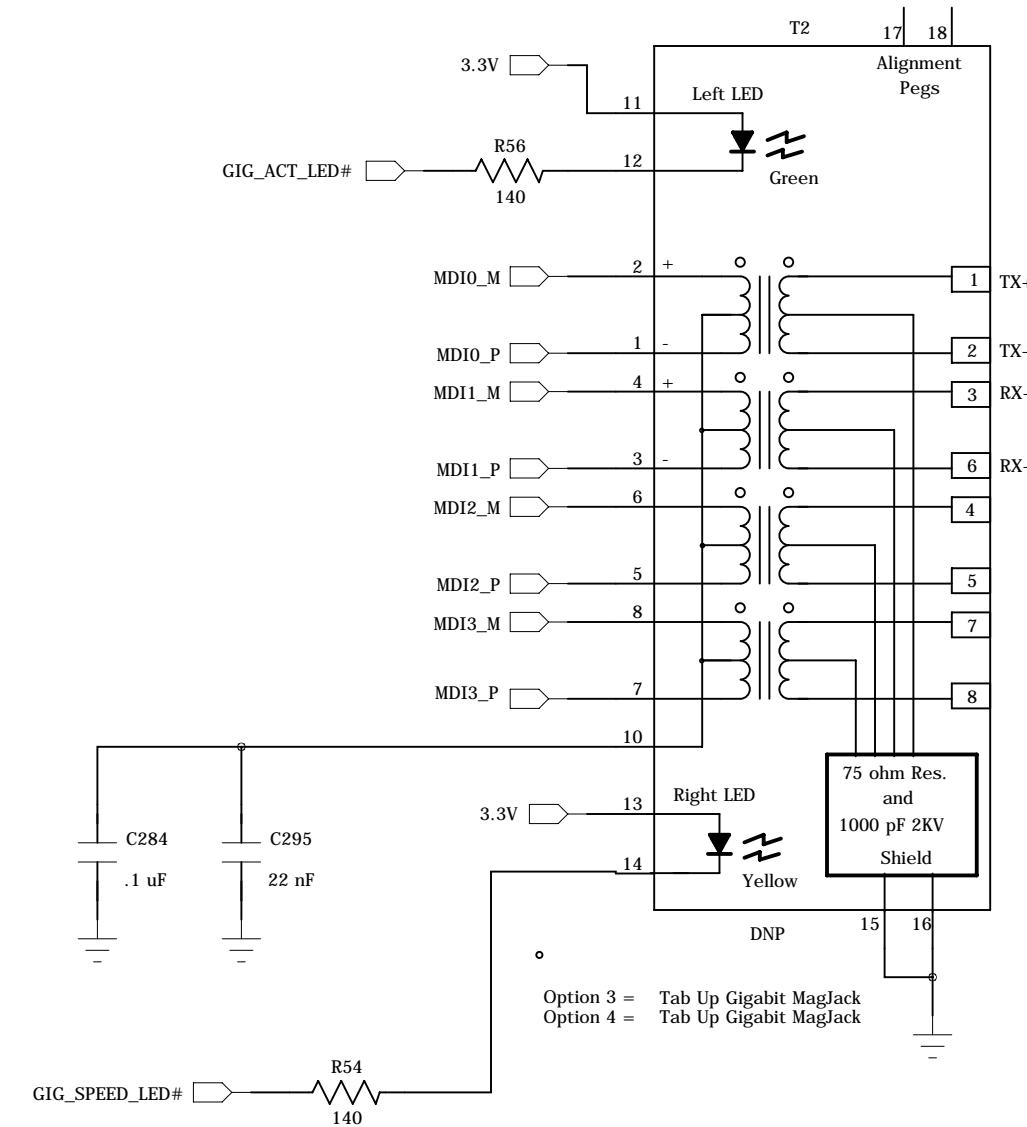


CPU ETH1 Gig MagJack



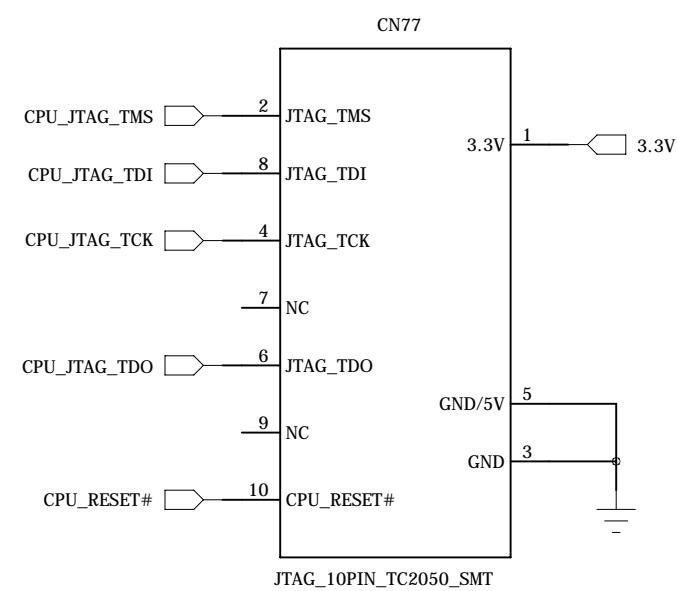
Left LED (Green)
Link / Activity

PCIe Ethernet Gig MagJack



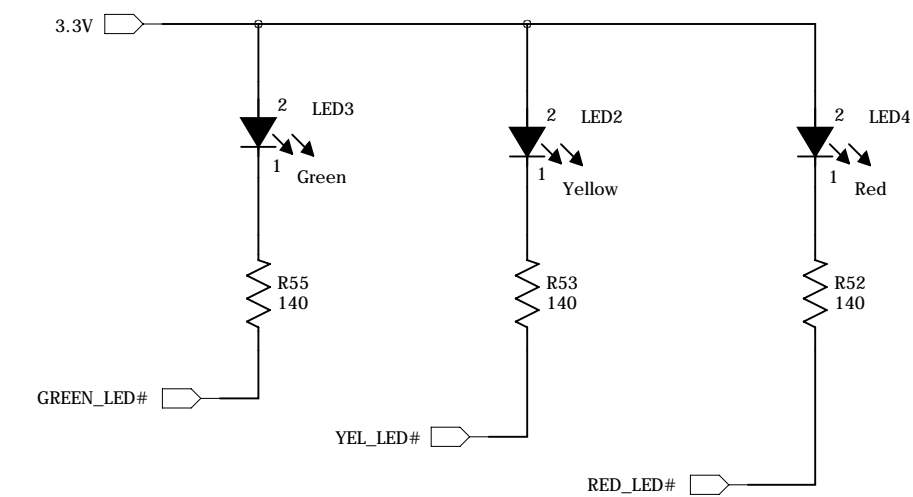
Swapped polarity of Ethernet pairs

CPU JTAG

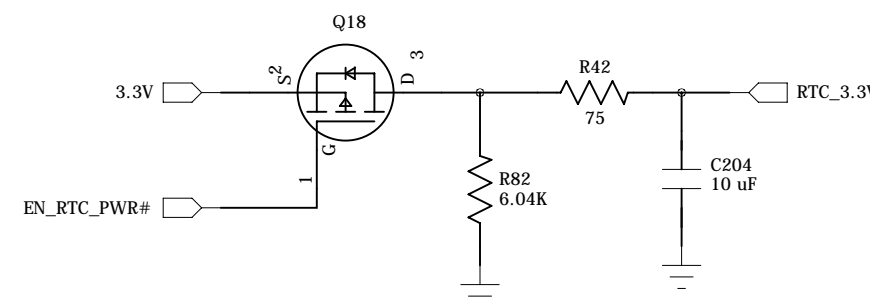
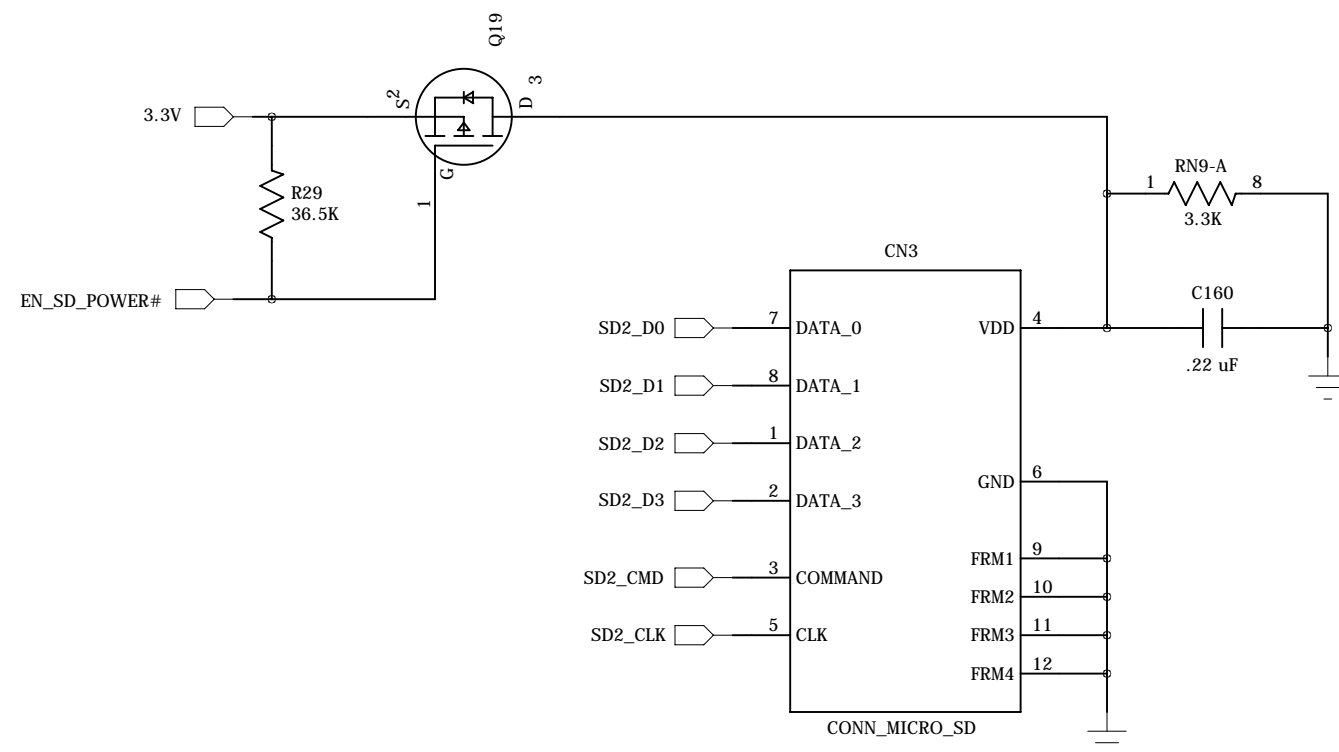


Tag-Connect

SMT RA LEDs

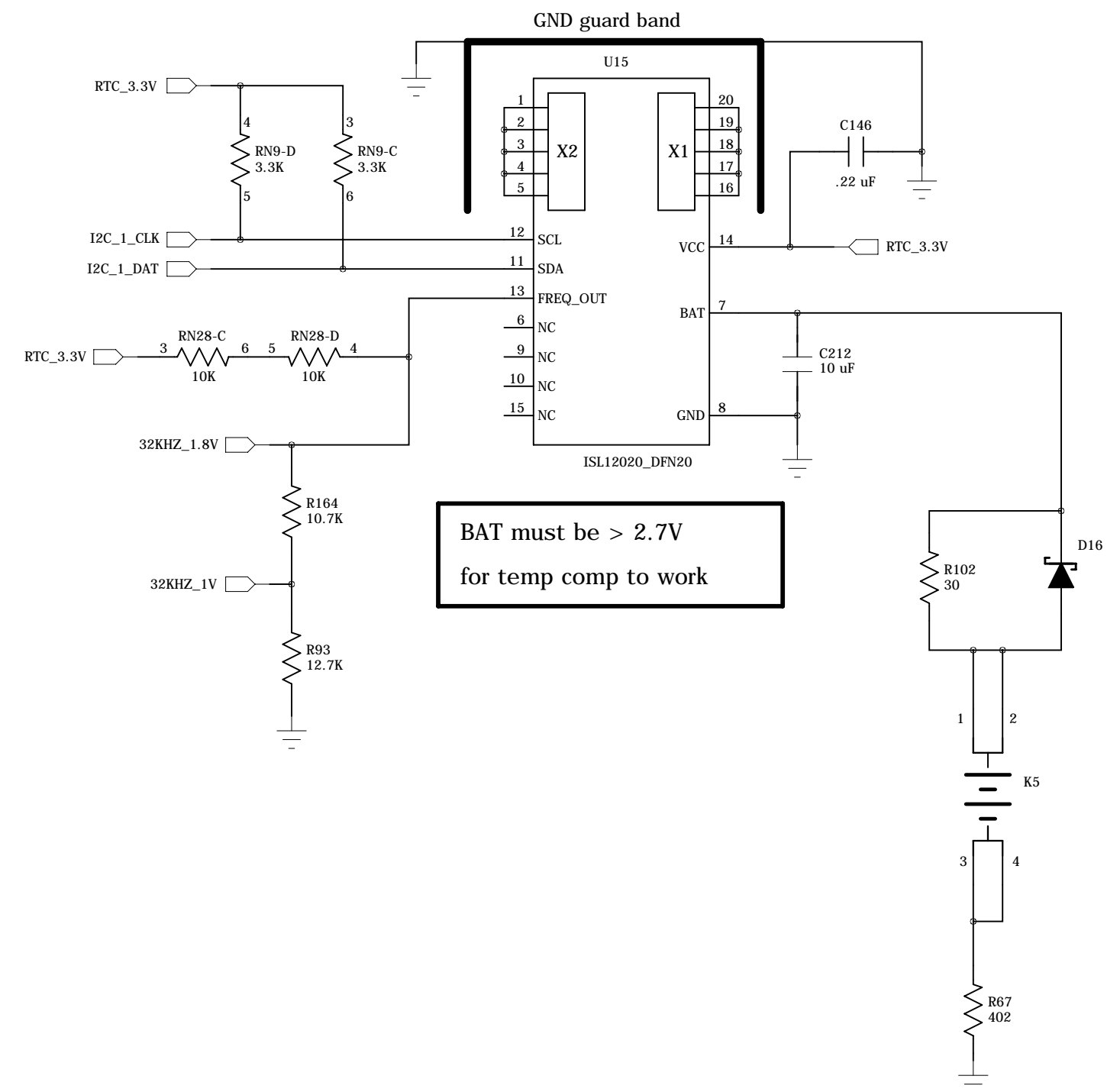


Micro SD Card Socket

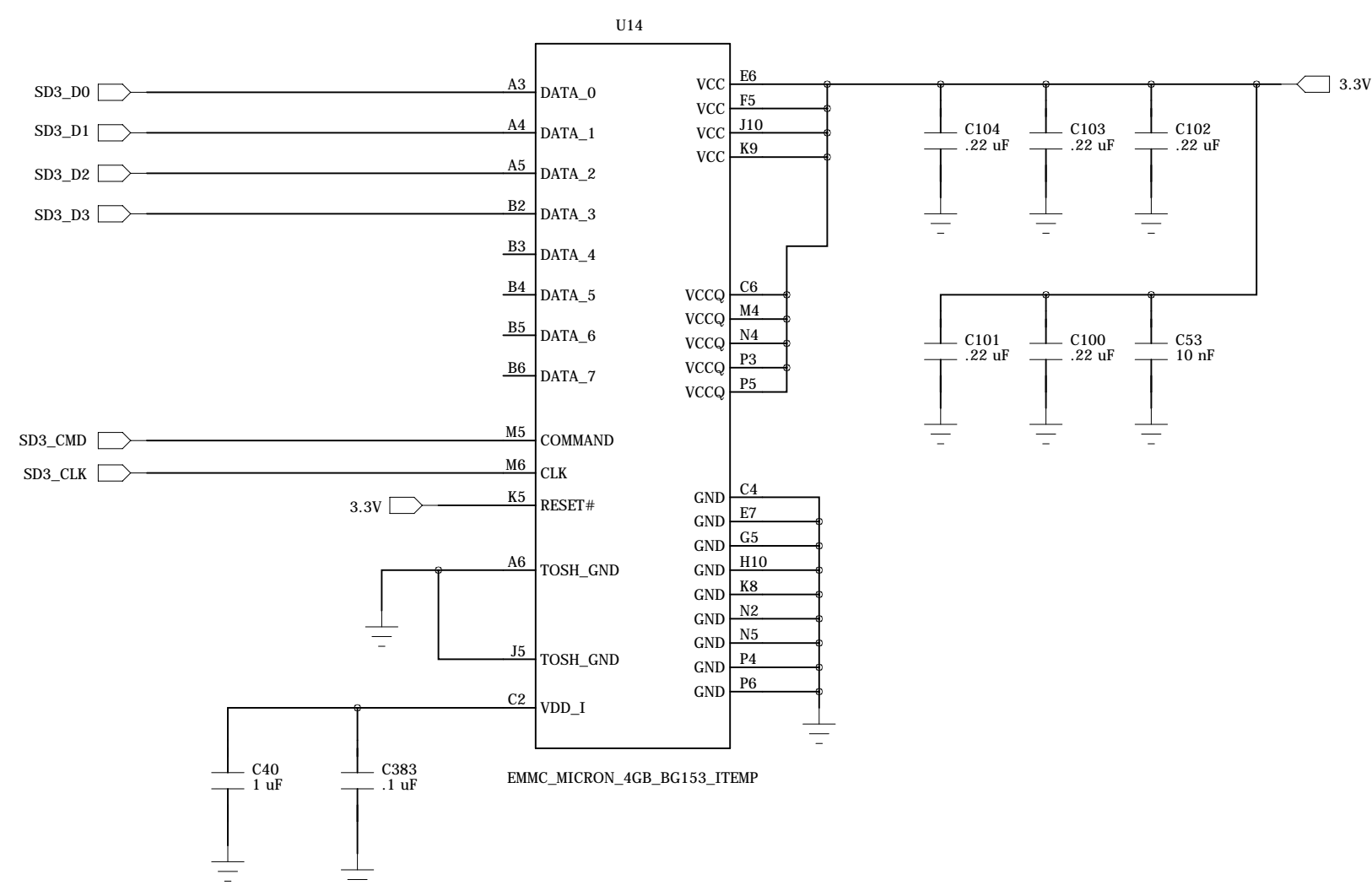


At system power up, FET is off

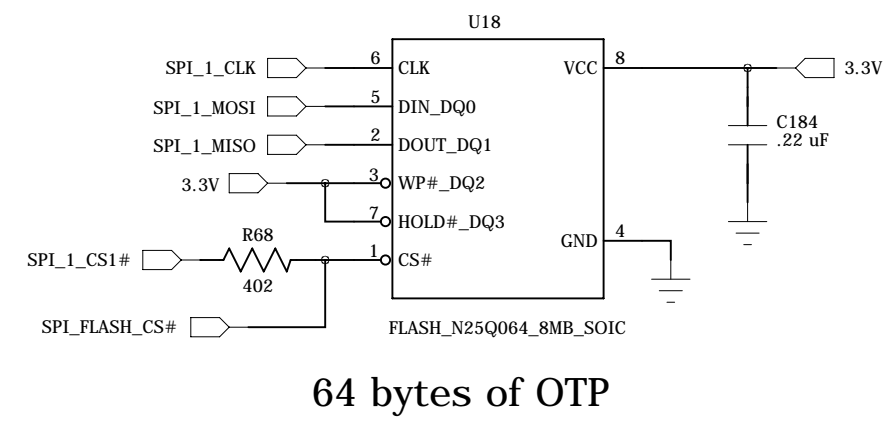
Precision RTC and Temp. Sensor



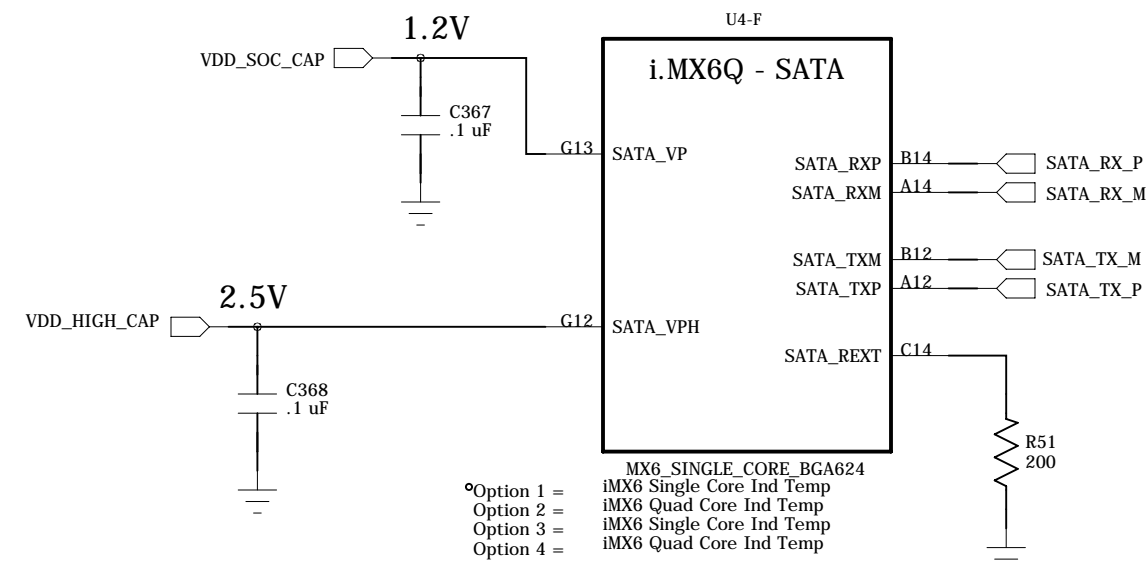
eMMC 4GB



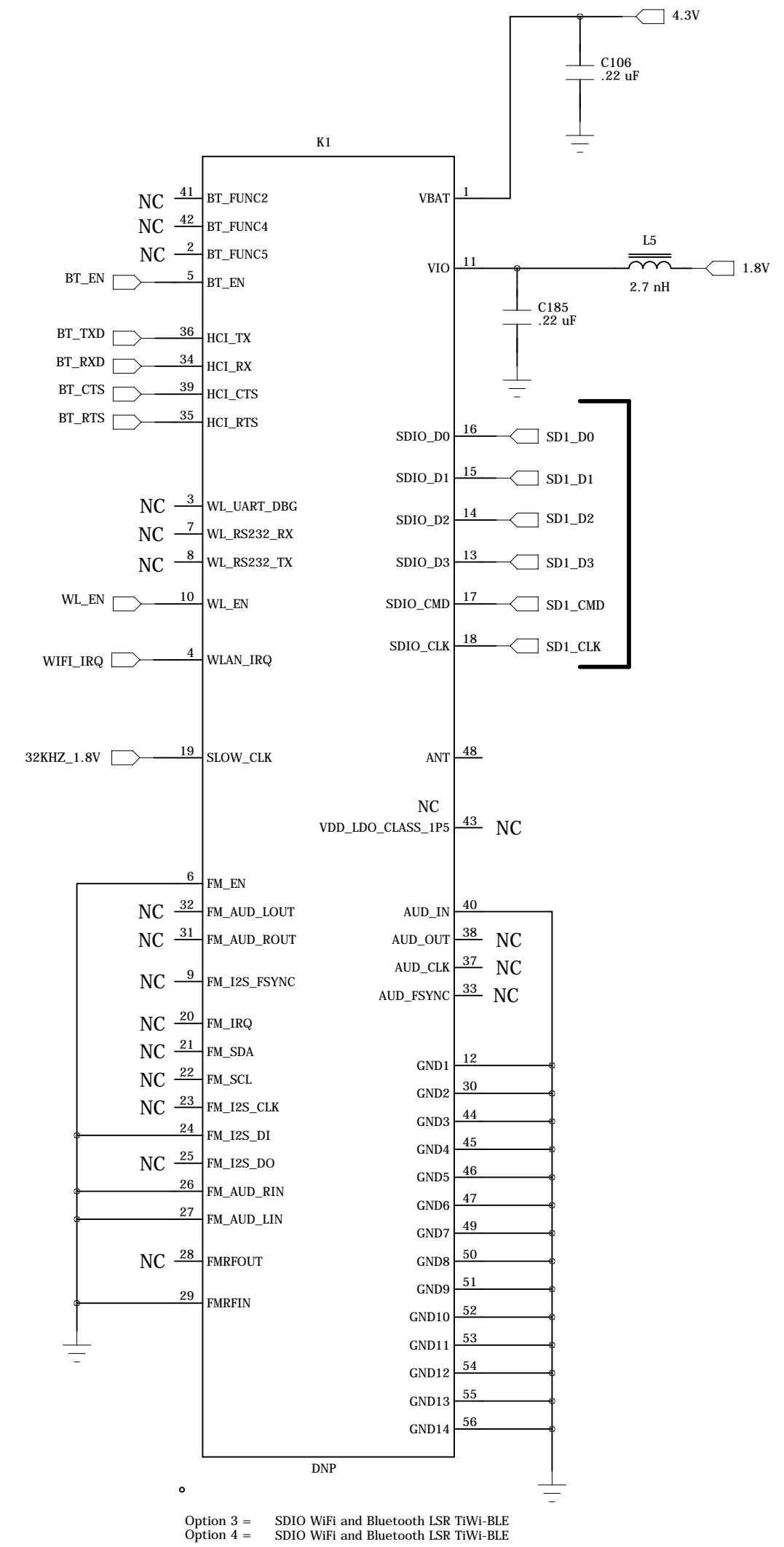
SPI Boot Flash



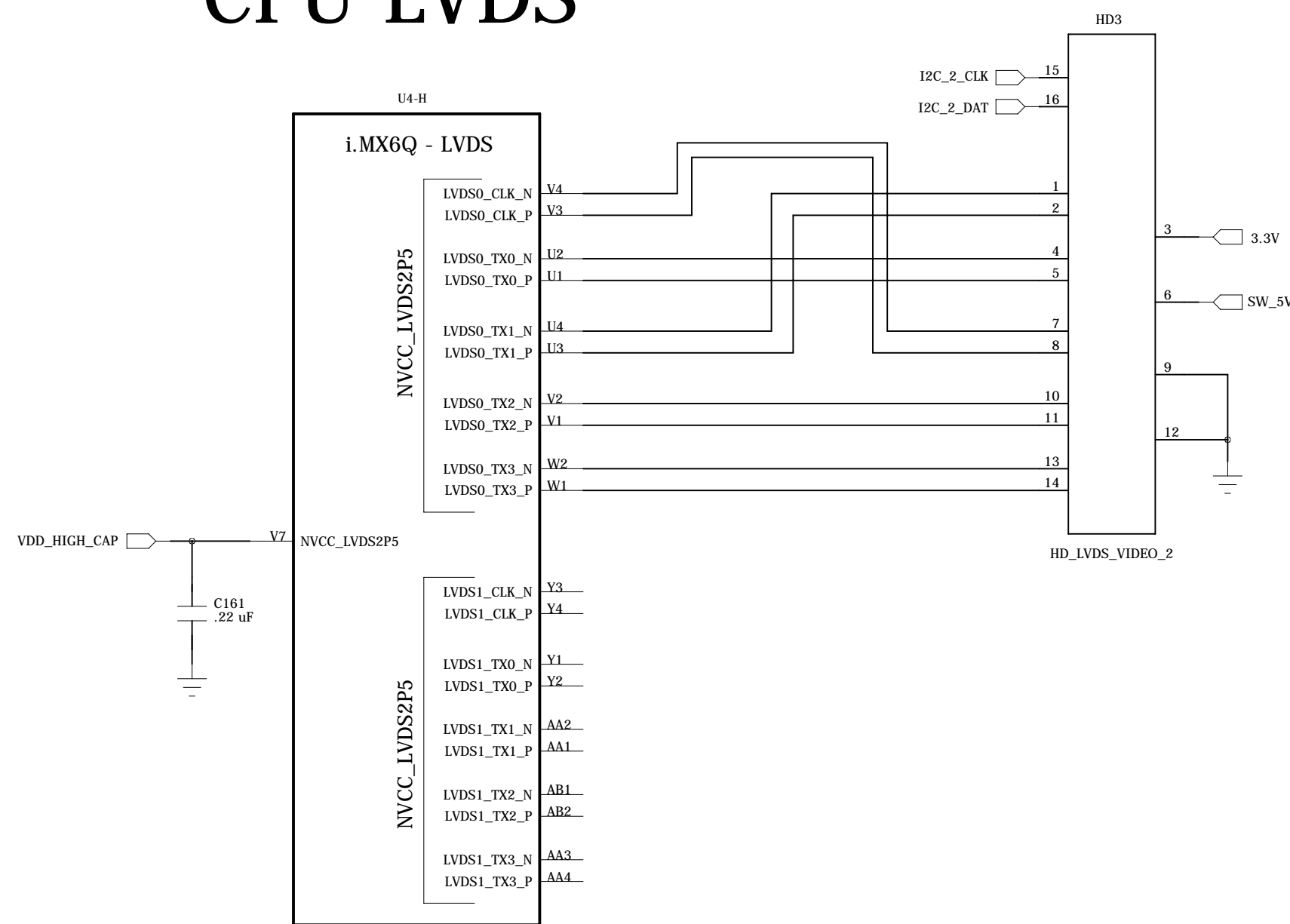
SATA



WiFi Radio



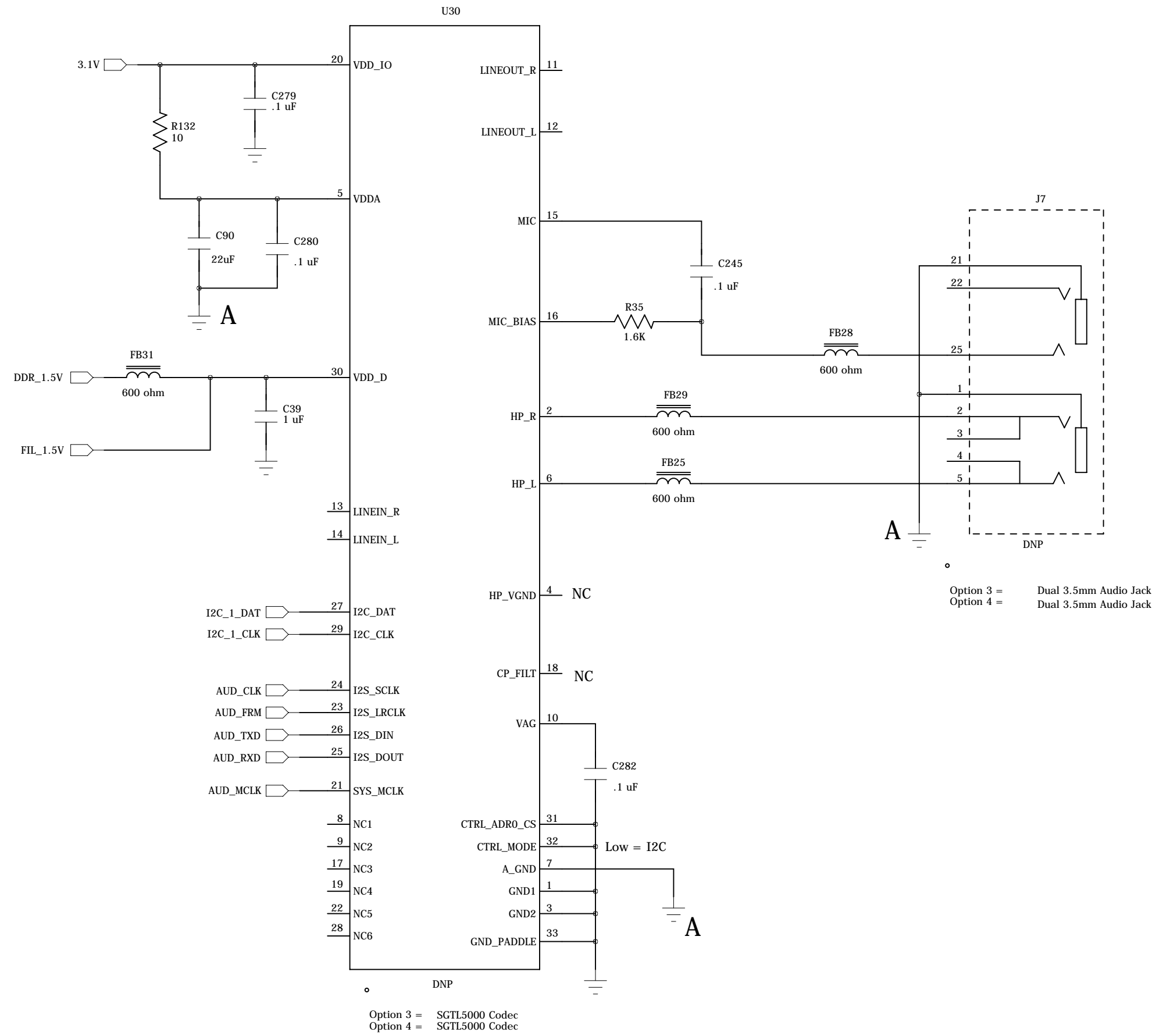
CPU LVDS



MX6_SINGLE_CORE_BGA624
 Option 1 = iMX6 Single Core Ind Temp
 Option 2 = iMX6 Quad Core Ind Temp
 Option 3 = iMX6 Single Core Ind Temp
 Option 4 = iMX6 Quad Core Ind Temp

LVDS Header

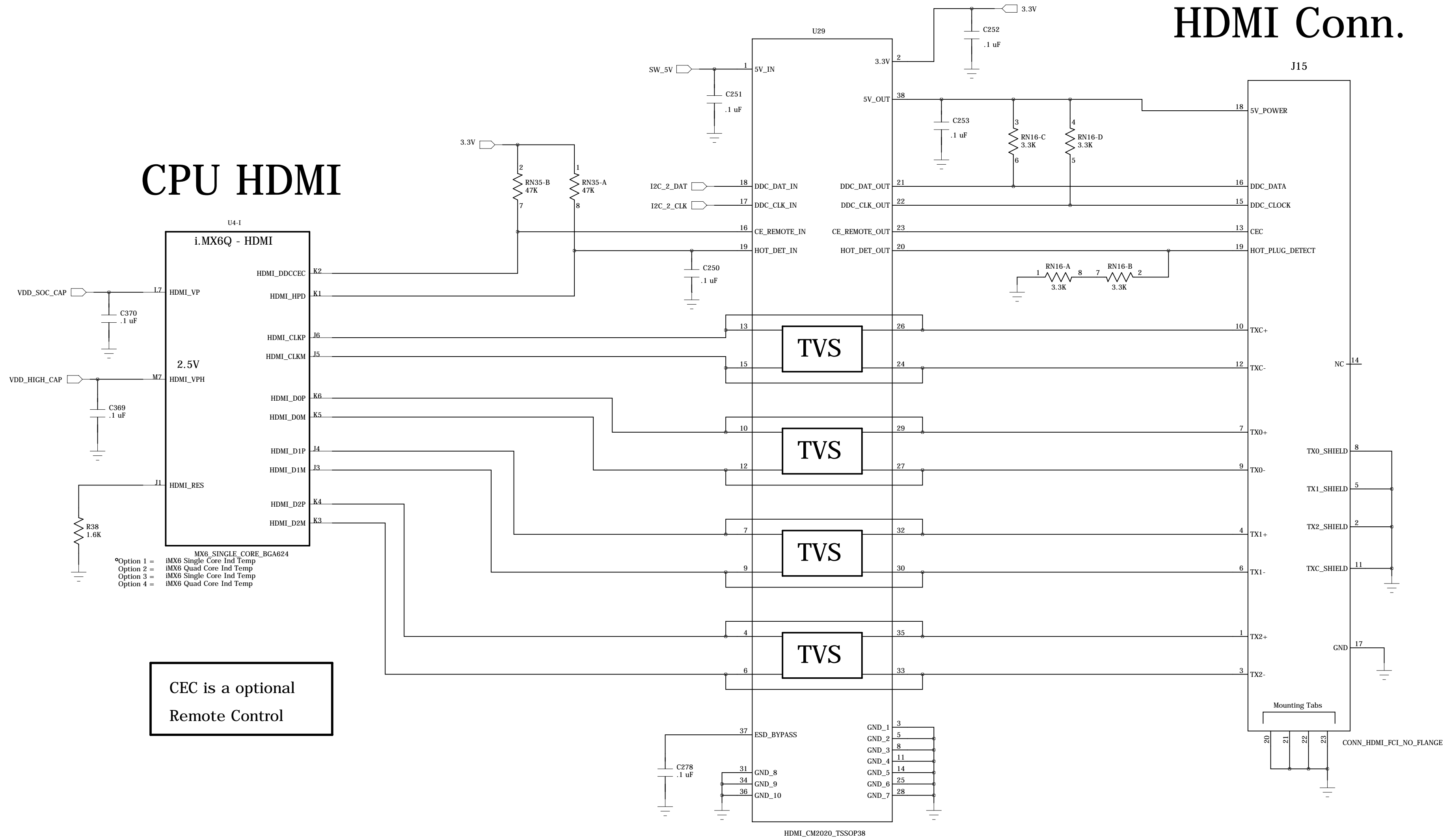
Audio CODEC



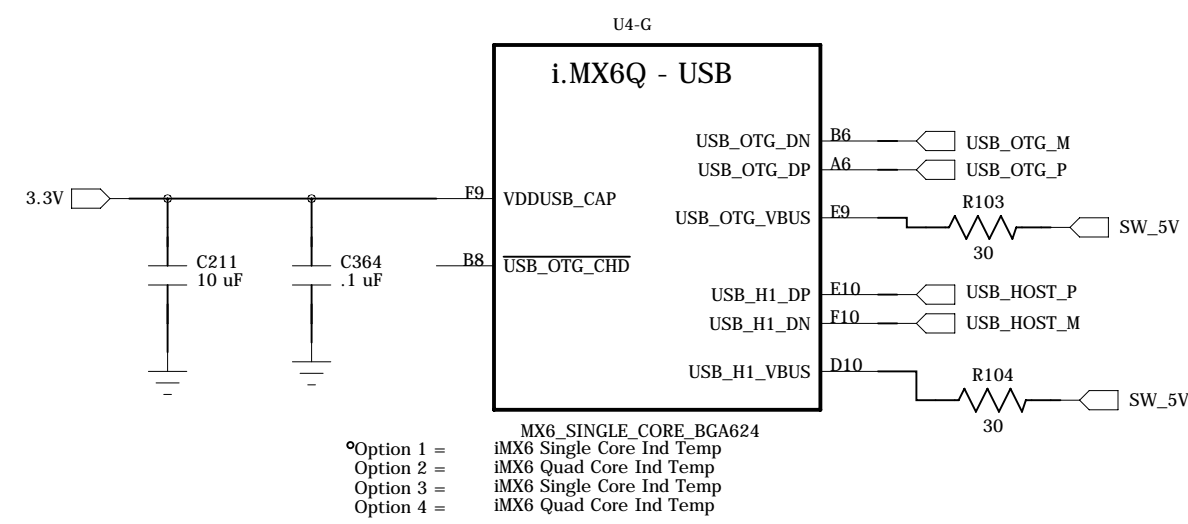
HDMI PHY

HDMI Conn.

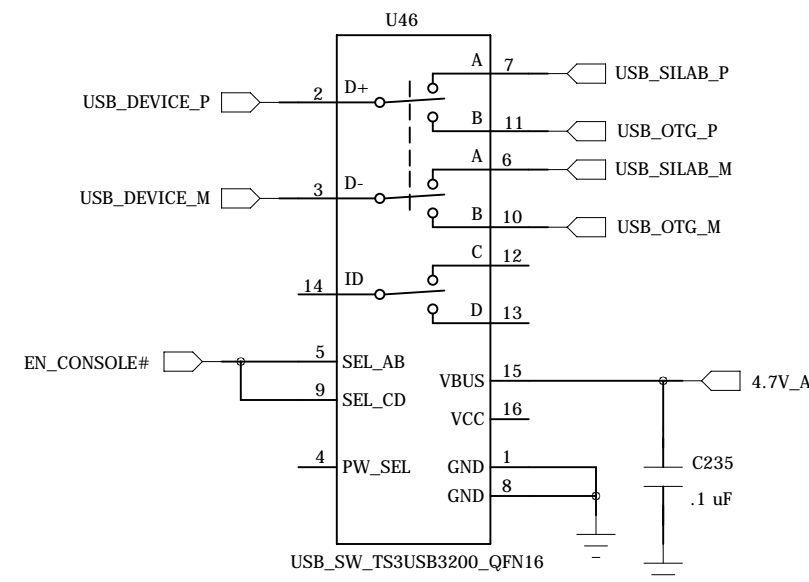
CPU HDMI



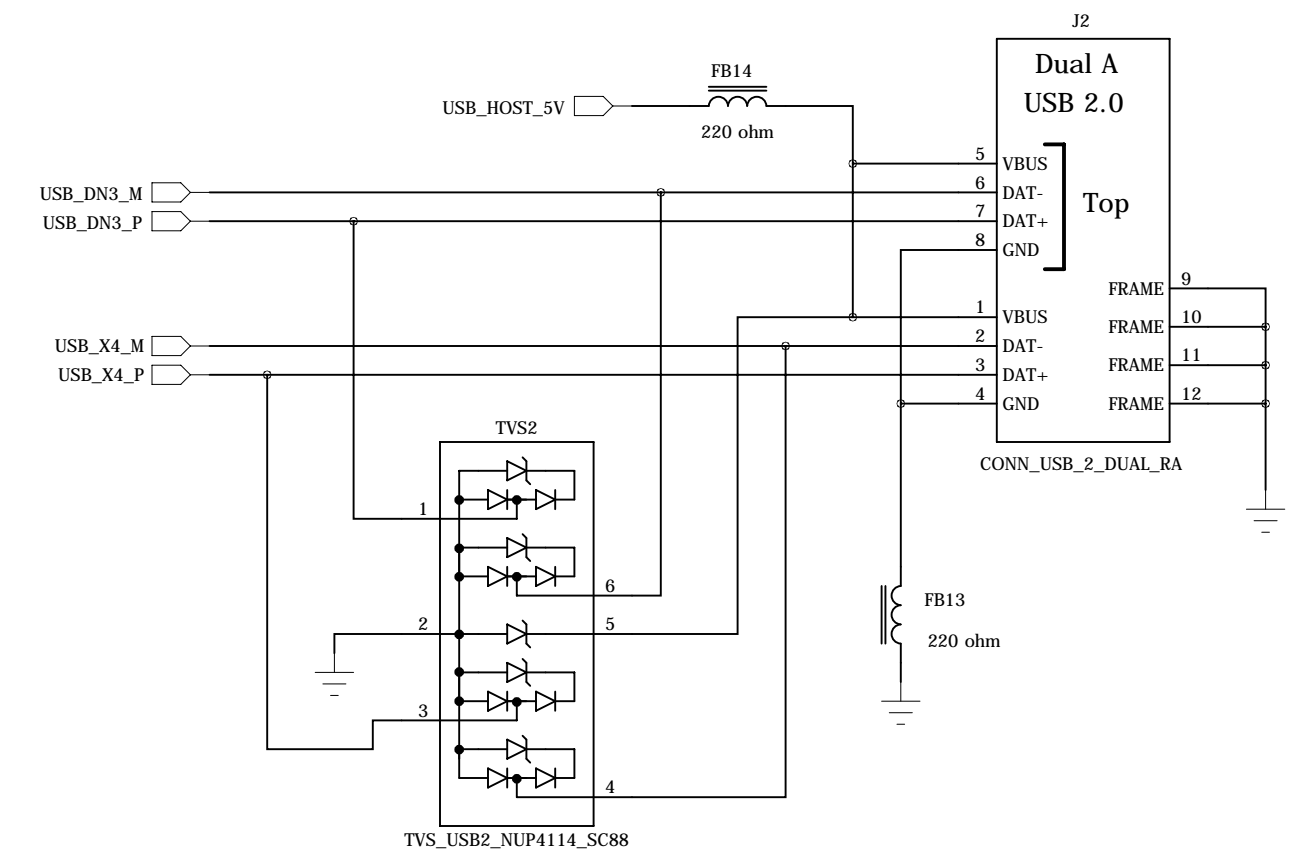
CPU USB



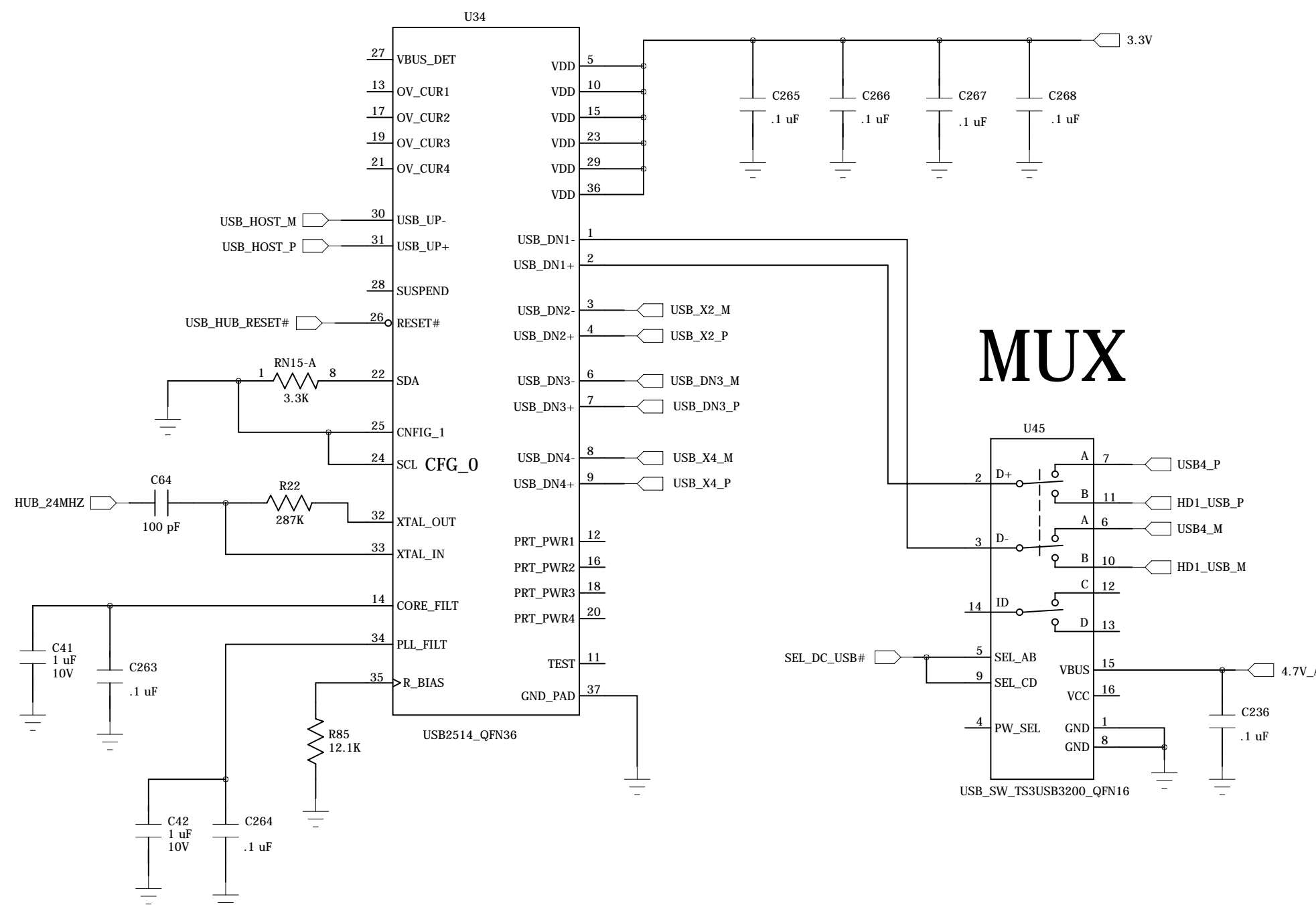
MUX



Dual Host USB

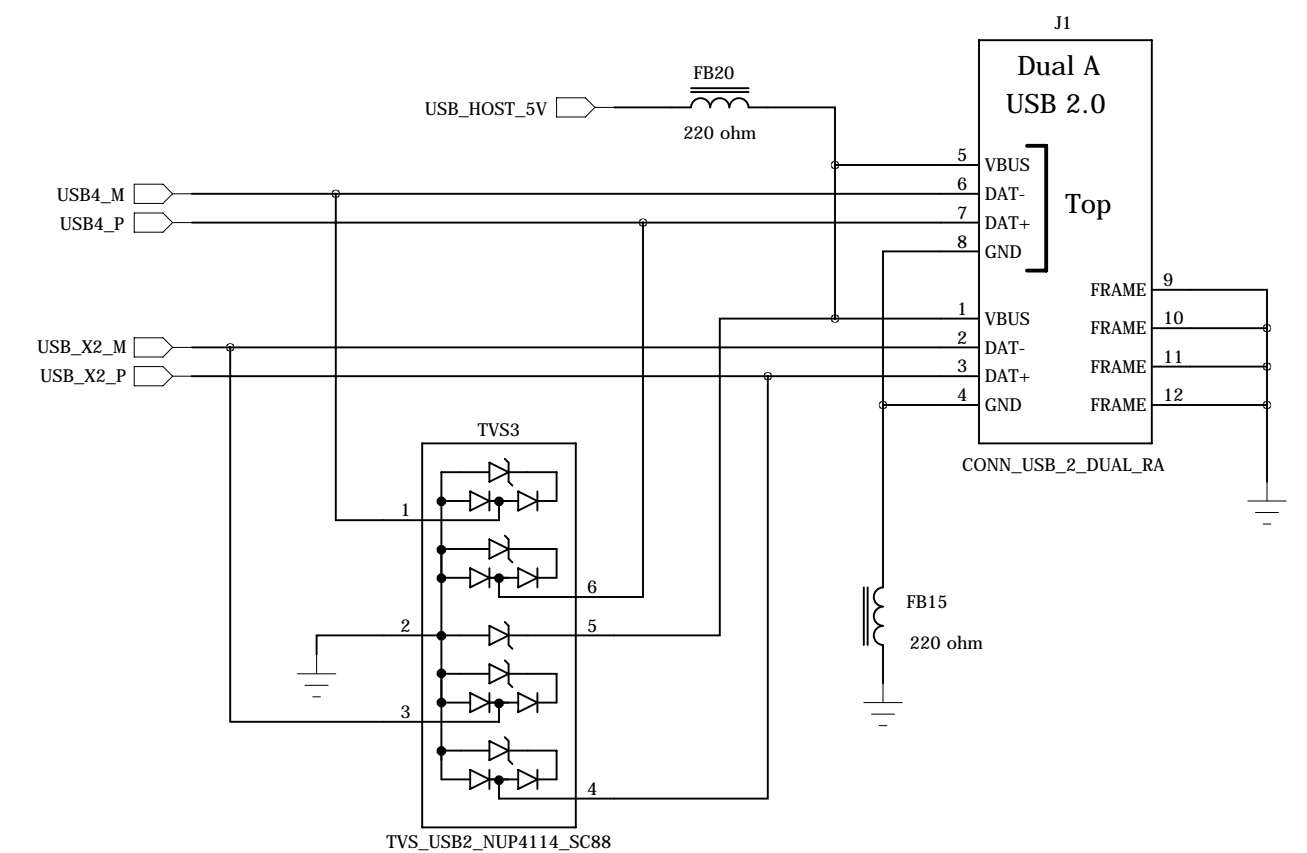


SMSC USB Hub



MUX

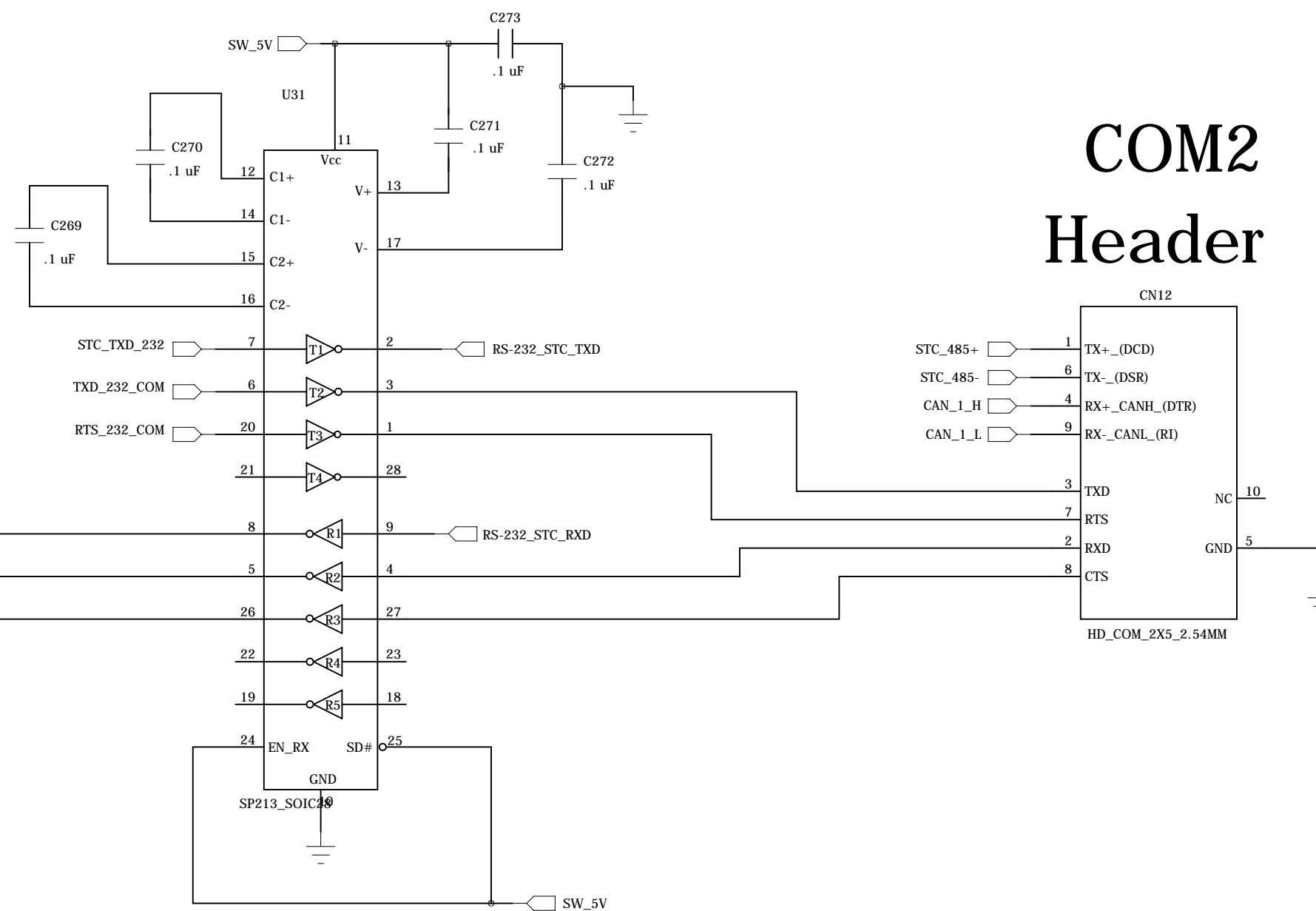
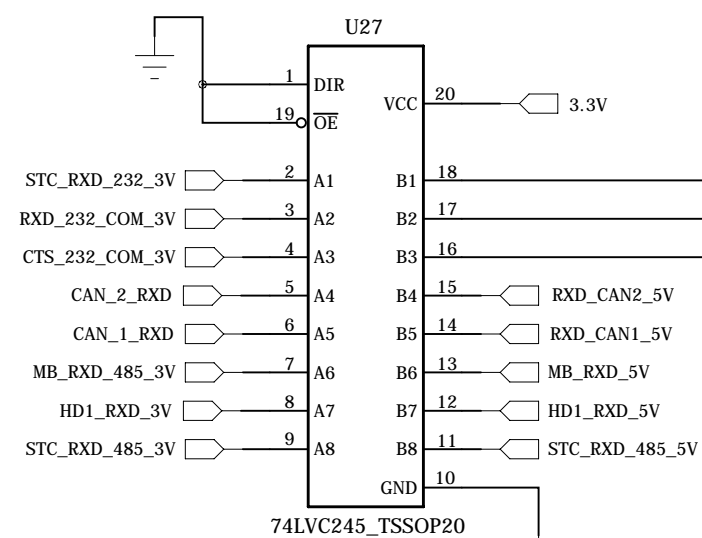
Dual Host USB near Ethernet Ports



RS-232 Transceiver

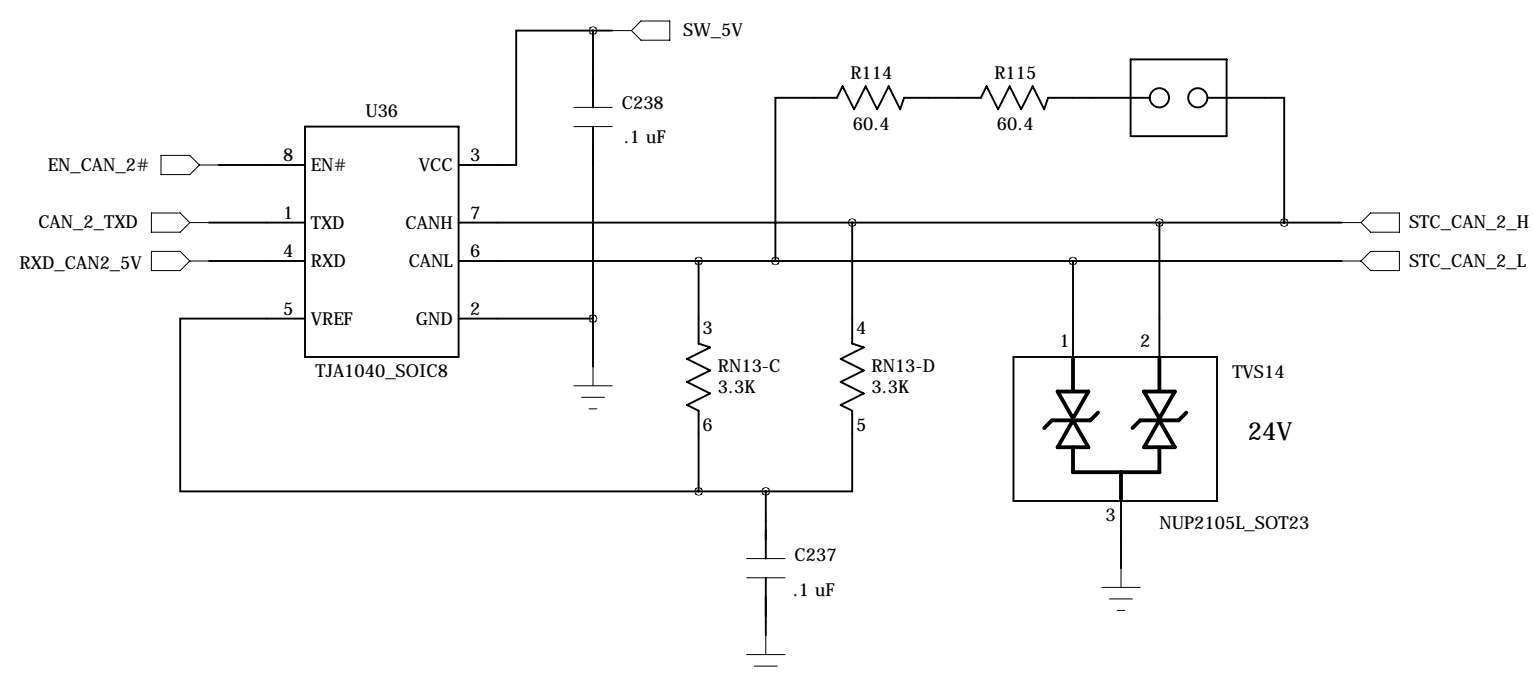
3.3V <-- 5V

Level shifter

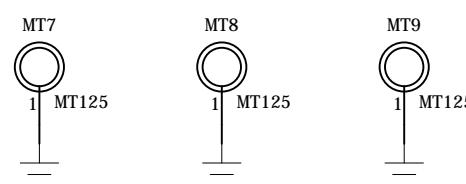
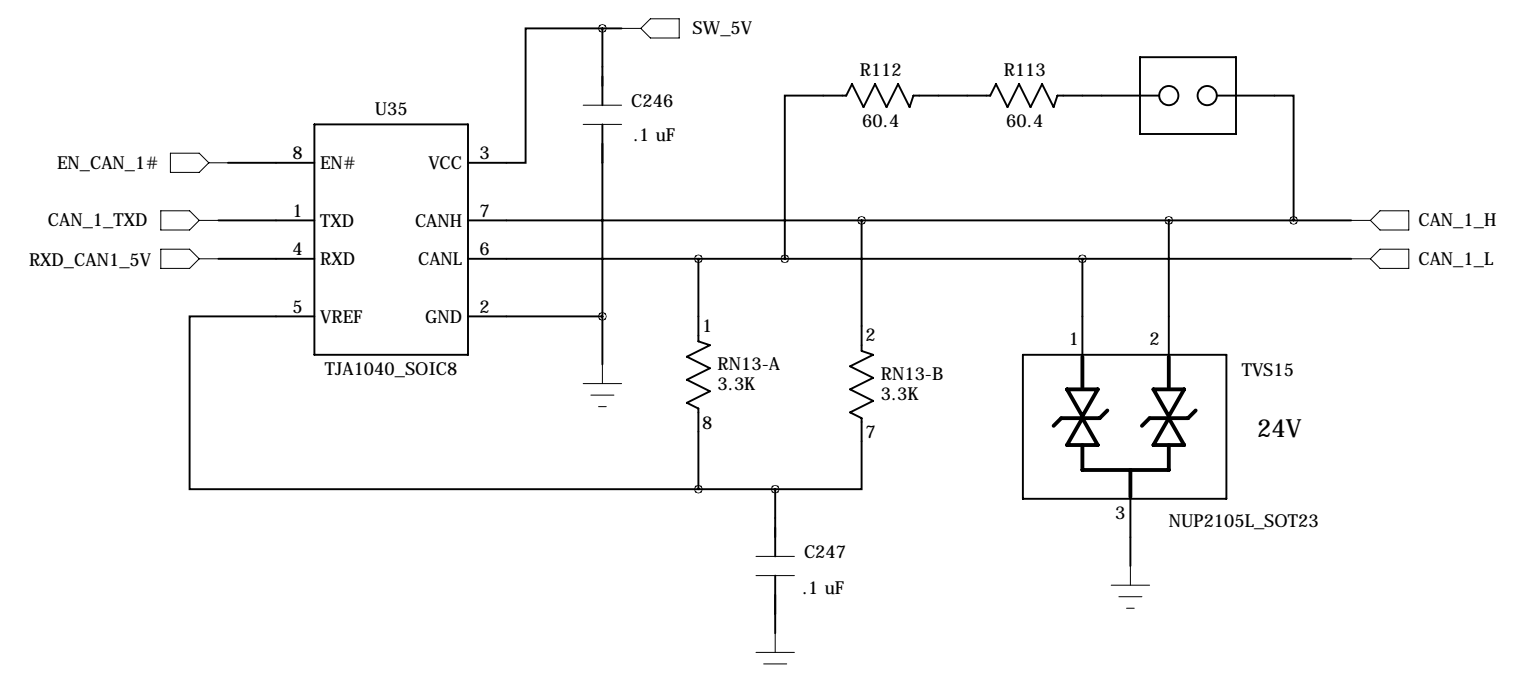


COM2 Header

CAN2 Transceiver

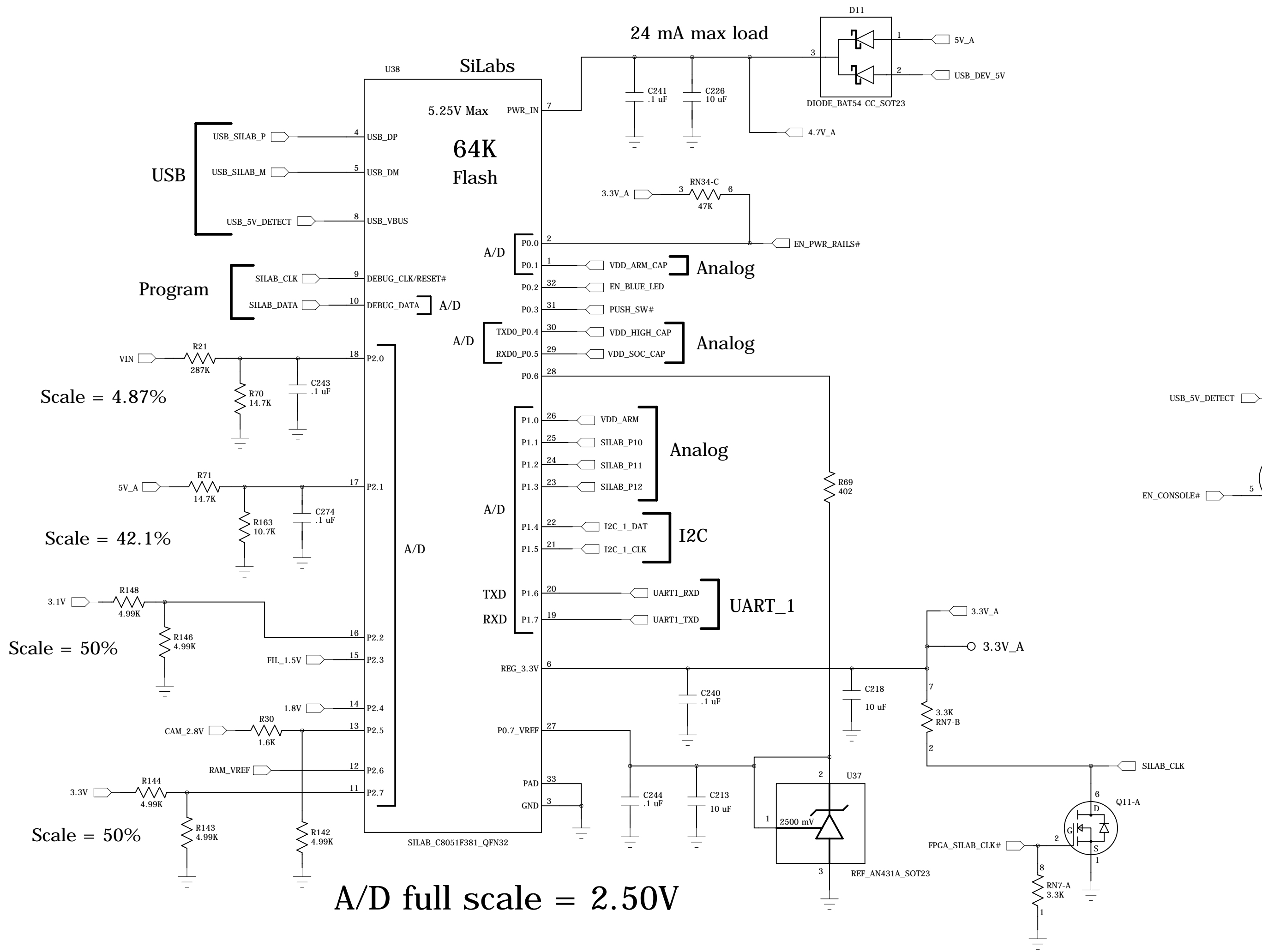


CAN1 Transceiver



| | | | |
|----------------------------|----------|--------------------|--|
| Technologic Systems | | Date Dec. 27, 2016 | |
| Title: TS-7970 RS-232, CAN | | | |
| Rev: E | Designer | Sheet 22 of 27 | |

USB Device Port and Silab uC



Scale = 4.87%

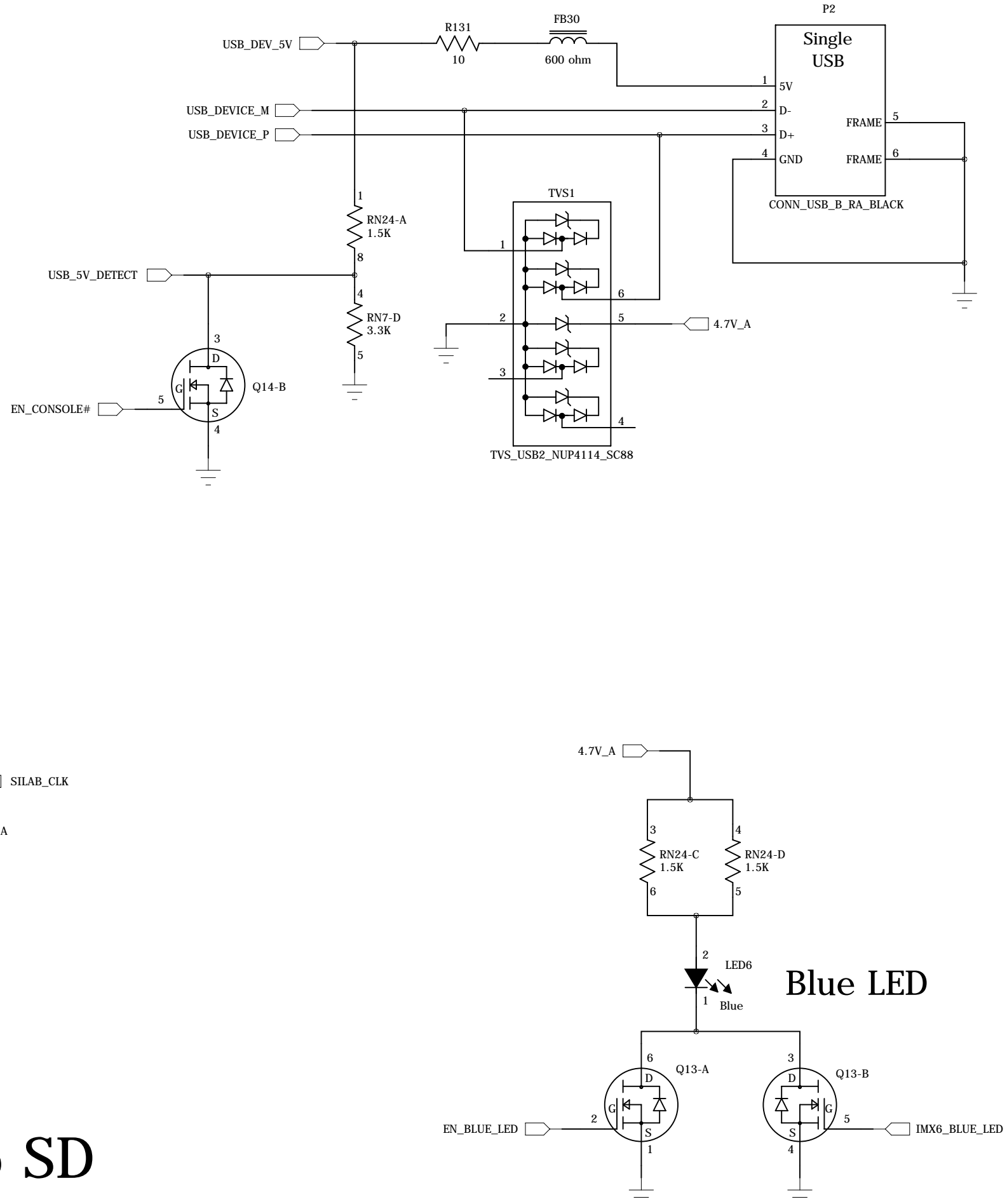
Scale = 42.1%

Scale = 50%

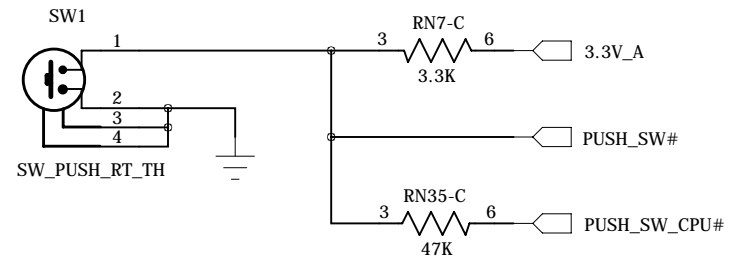
Scale = 50%

A/D full scale = 2.50V

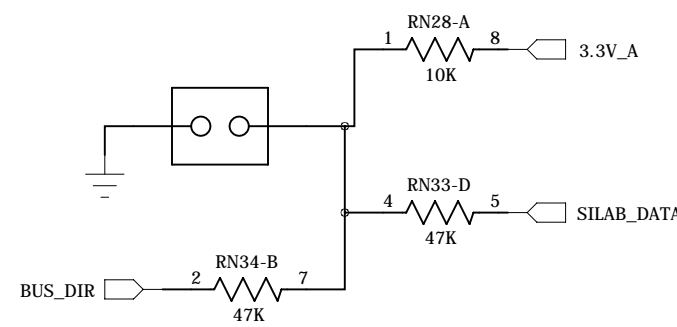
USB Device Port



Push Switch



Boot to SD



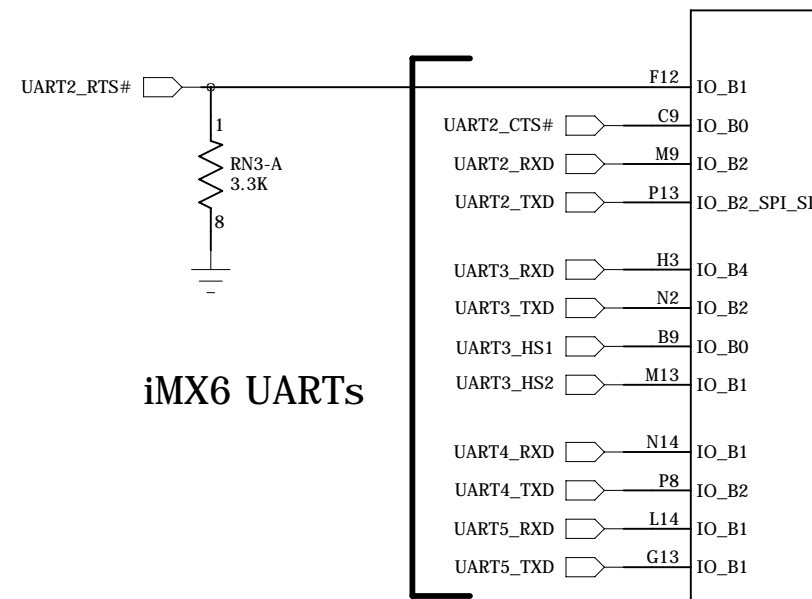
| | |
|---------------------------------|--------------------|
| Technologic Systems | Date Dec. 27, 2016 |
| Title: TS-7970 Micro Controller | |
| Rev: E | Designer |
| Sheet 23 of 27 | |

MACH XO2 FPGA

FPGA required for:

- Adds a MAX3100 UART via SPI
- Auto-485 for two UARTs
- Provides serial port MUXing

iMX6 UARTs



Resistor Strapping Table

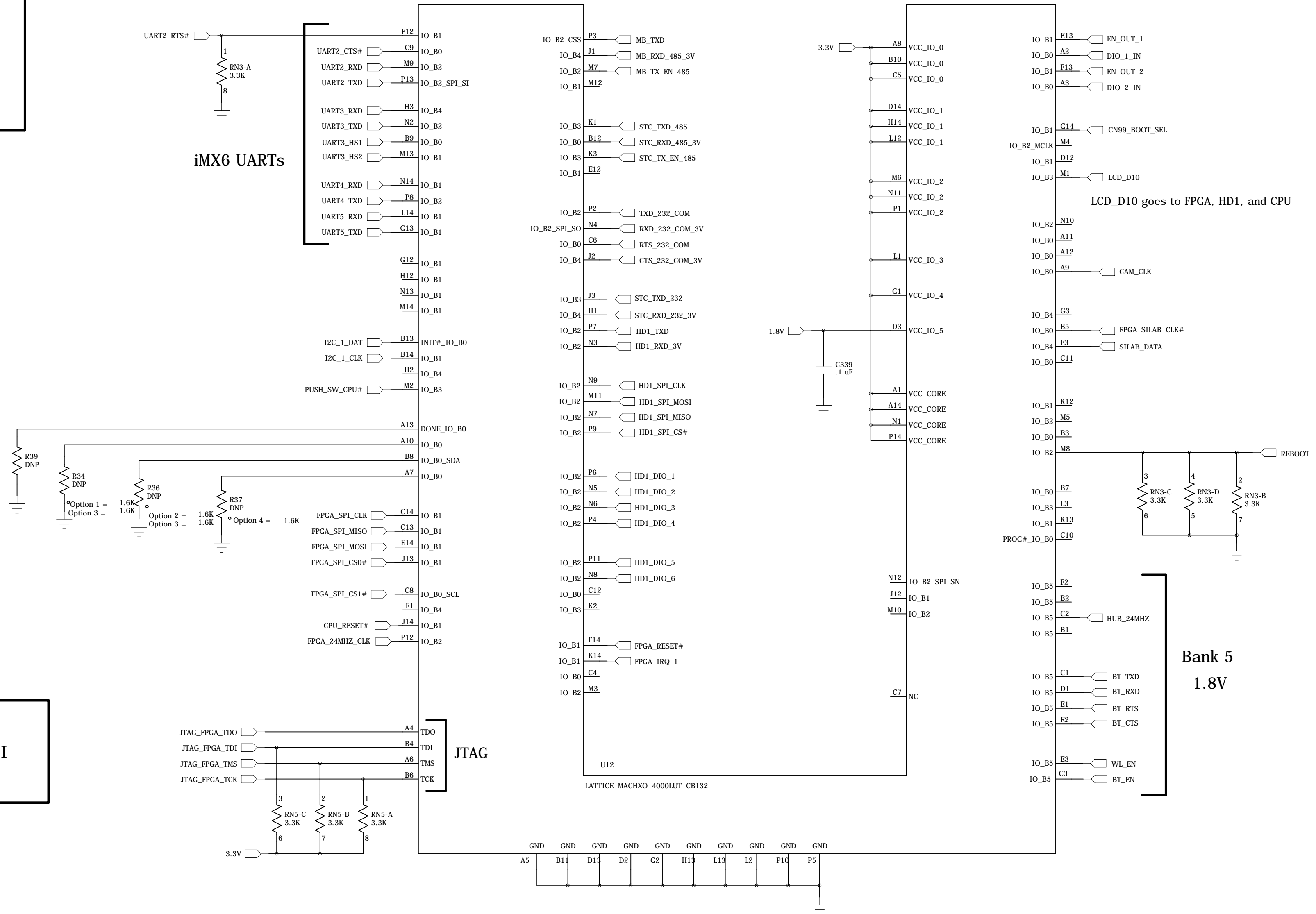
0=DNP, 1=POP

| R39 | R37 | R36 | R34 | |
|-----|-----|-----|-----|----------|
| 0 | 0 | 0 | 1 | Option 1 |
| 0 | 0 | 1 | 0 | Option 2 |
| 0 | 0 | 1 | 1 | Option 3 |
| 0 | 1 | 0 | 0 | Option 4 |
| 1 | 1 | 1 | 1 | Reserved |

PUSH_SW# has no direct connect to CPU

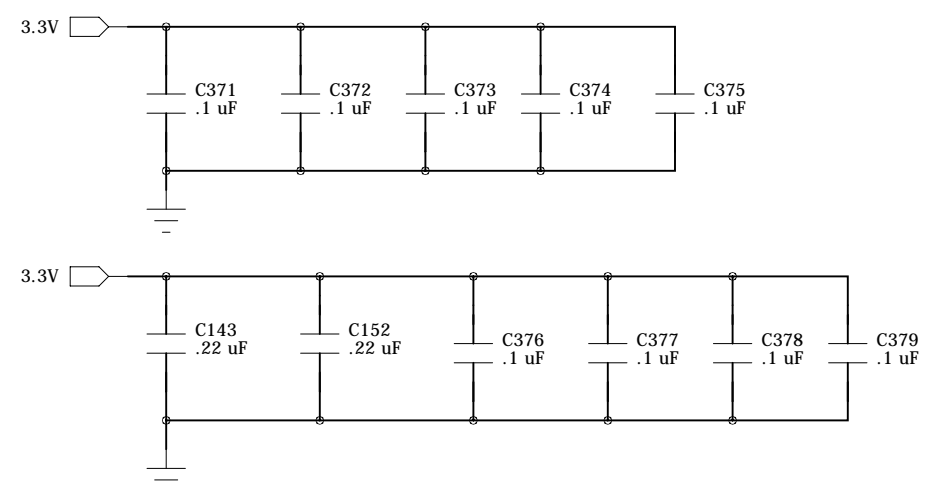
send status to CPU via_FPGA_IRQ1 until disabled

HD1_SPI_CS# is driven by CPU
When true, FPGA "passes thru" SPI bus signals to HD1



LCD_D10 goes to FPGA, HD1, and CPU

Bank 5 1.8V

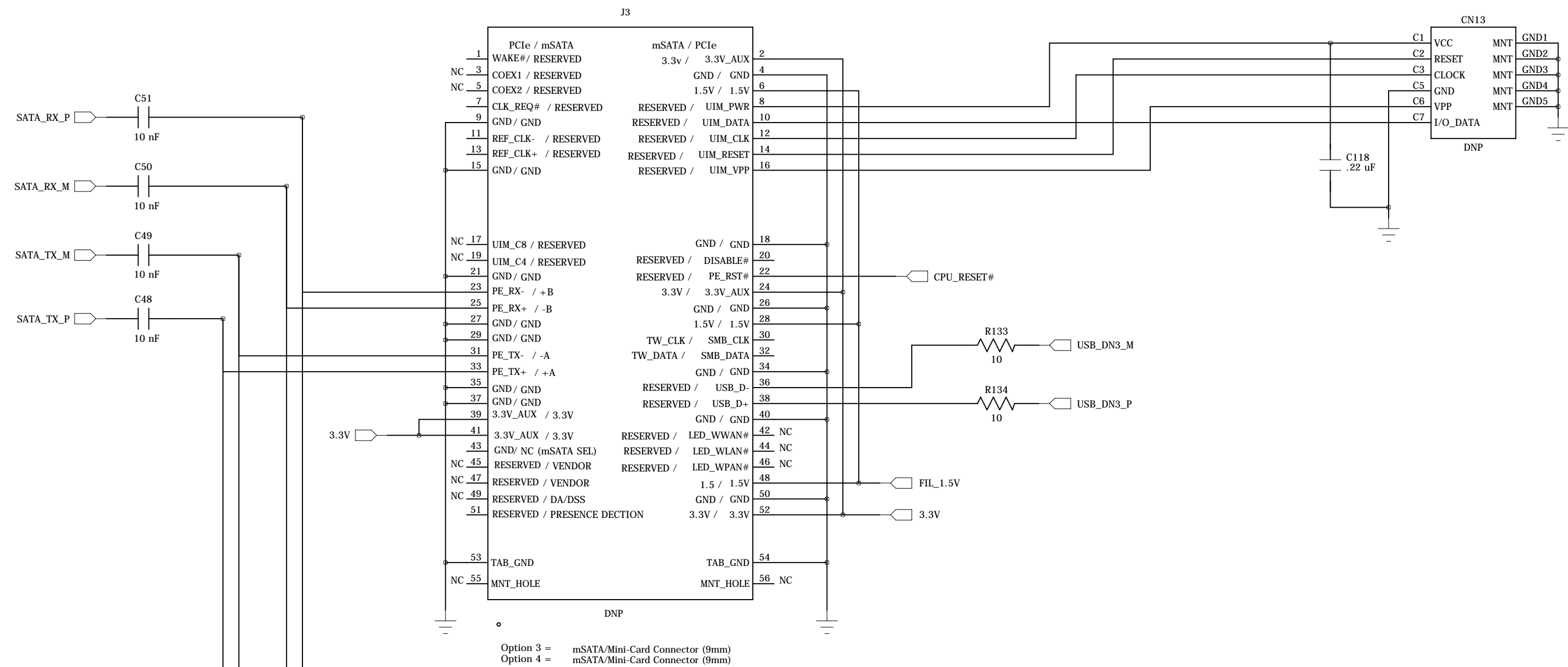


mSATA or USB only Mini-Cards

7mm Stack Height
to center of bd.

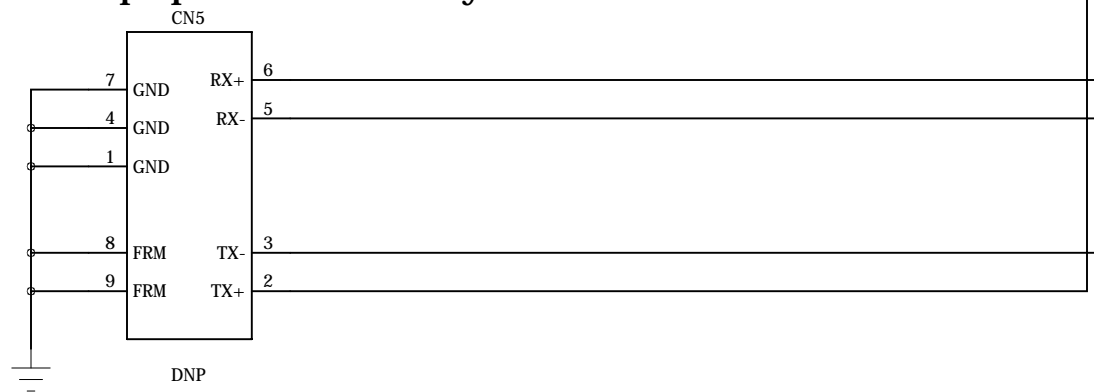
SIM Card Connector

For use with mini-card USB Cell modems

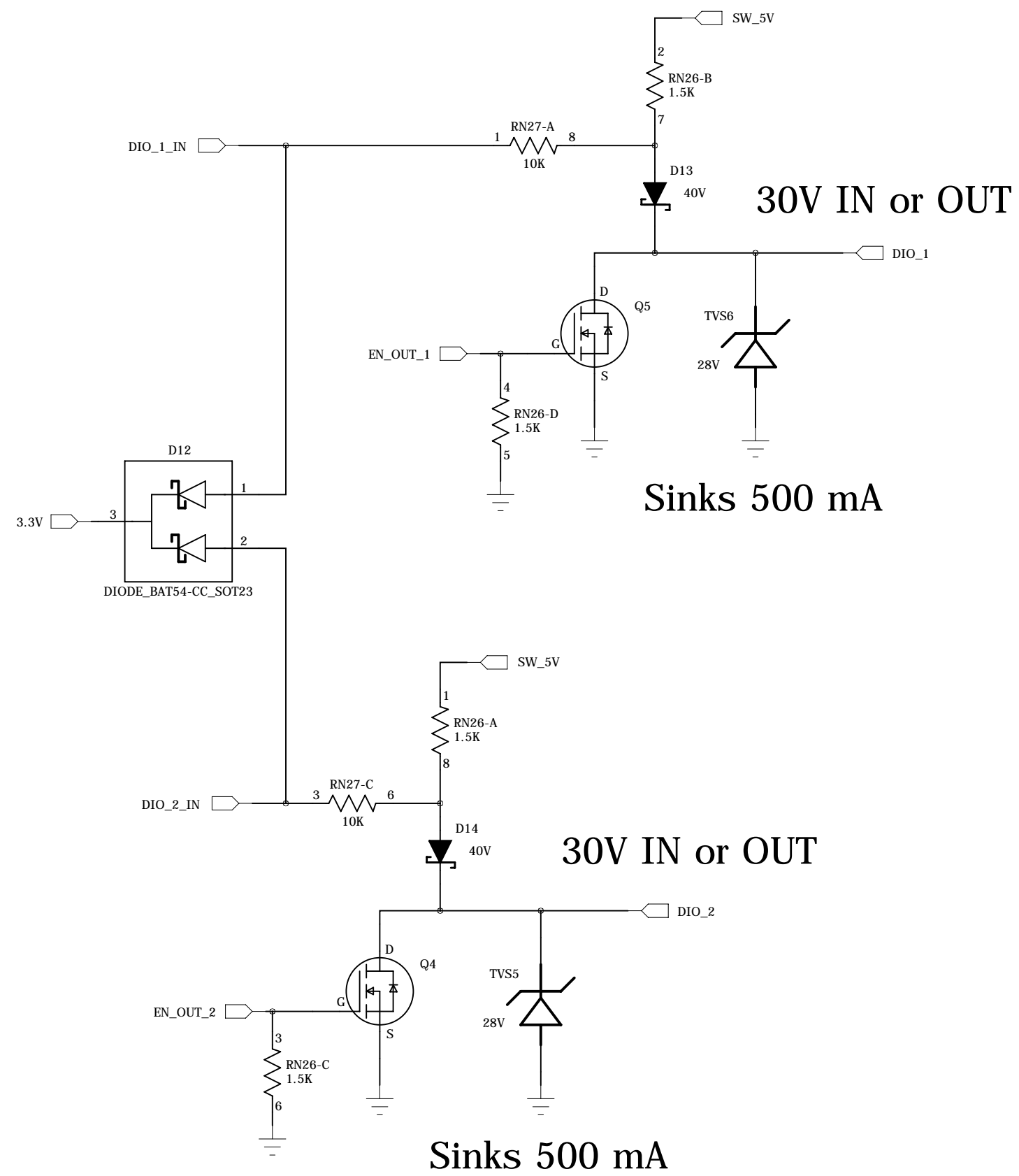


SATA Port

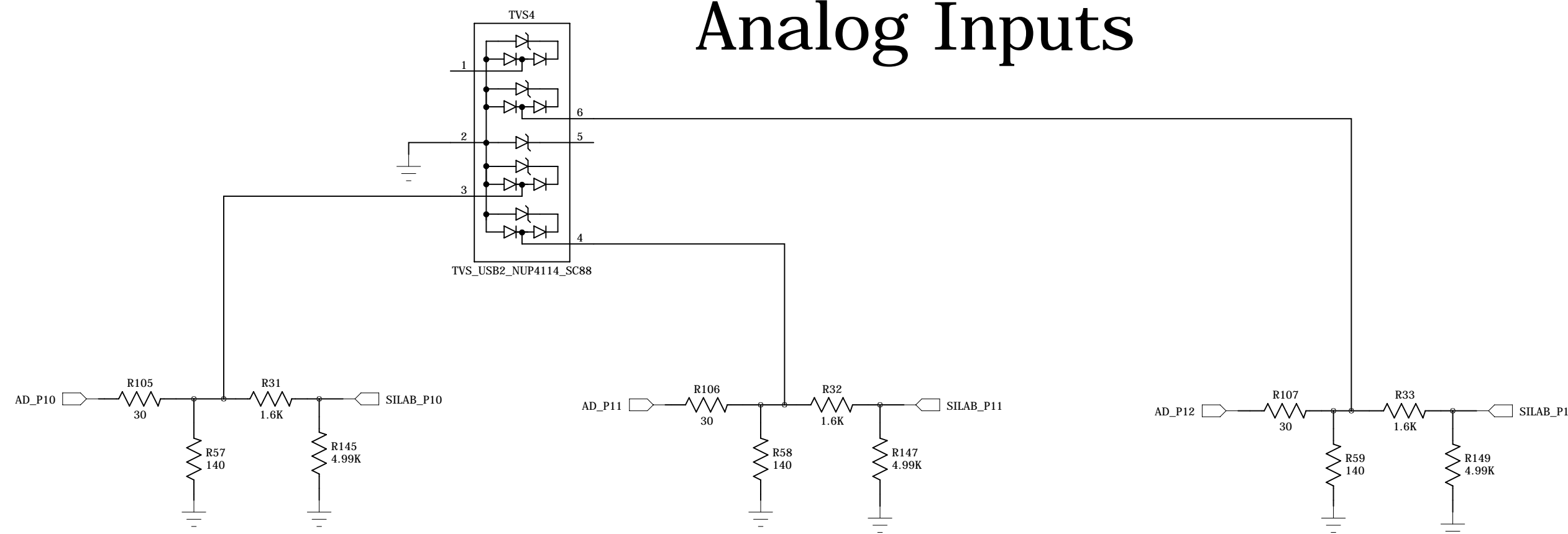
Option not populated on any standard models



Two DIO



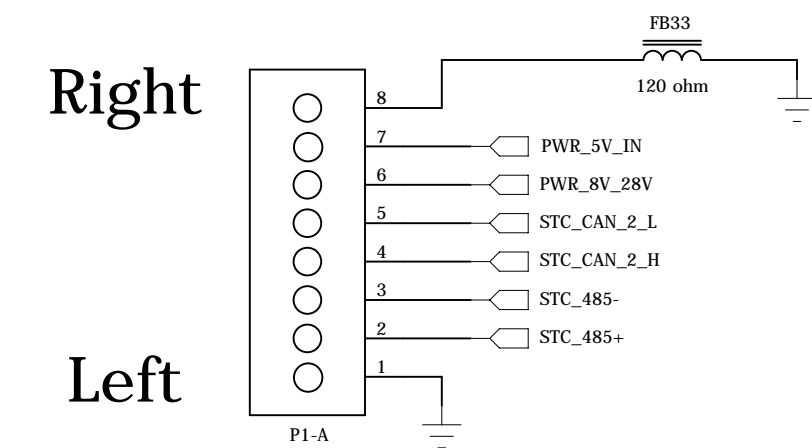
4 to 20 mA Analog Inputs



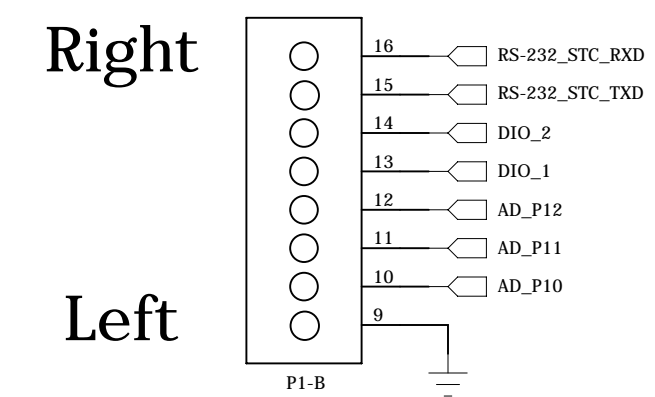
Screw Terminals

2 Rows x 8

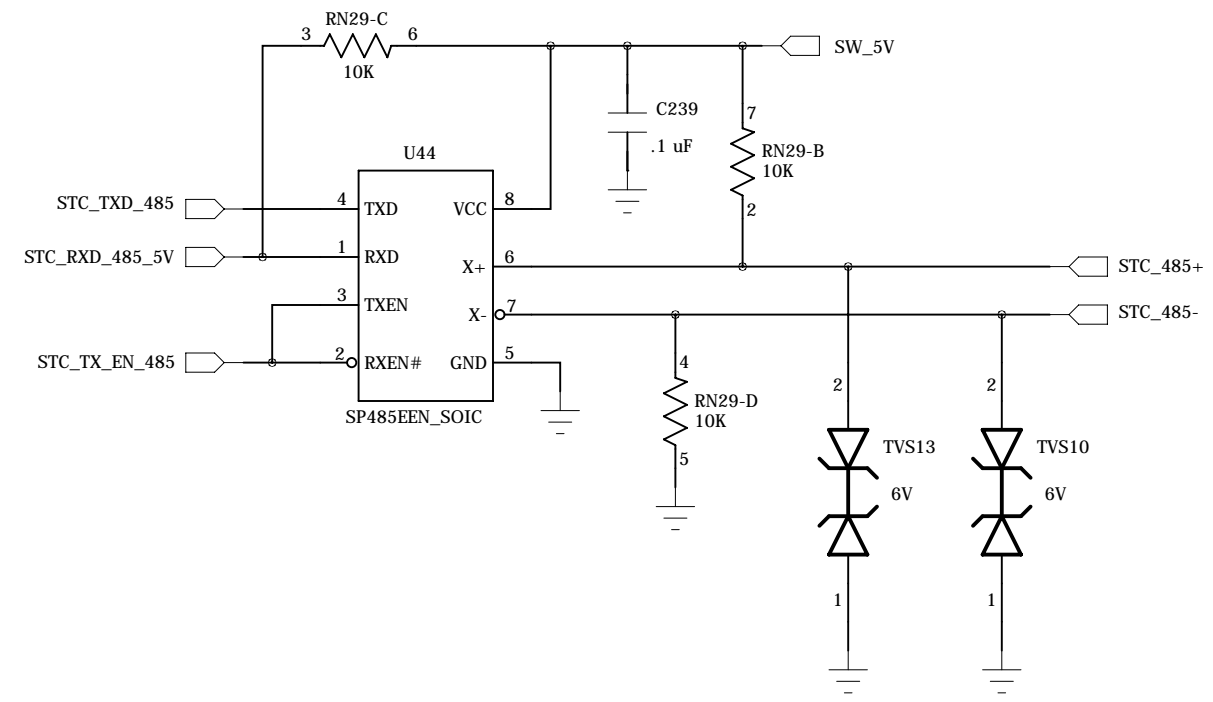
Top Row



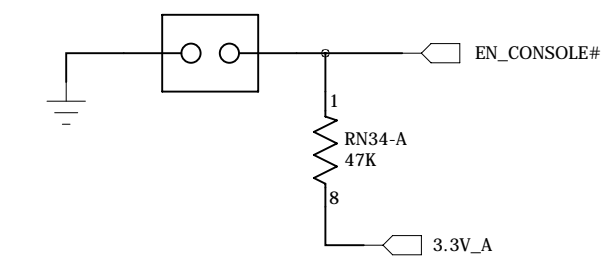
Bottom Row



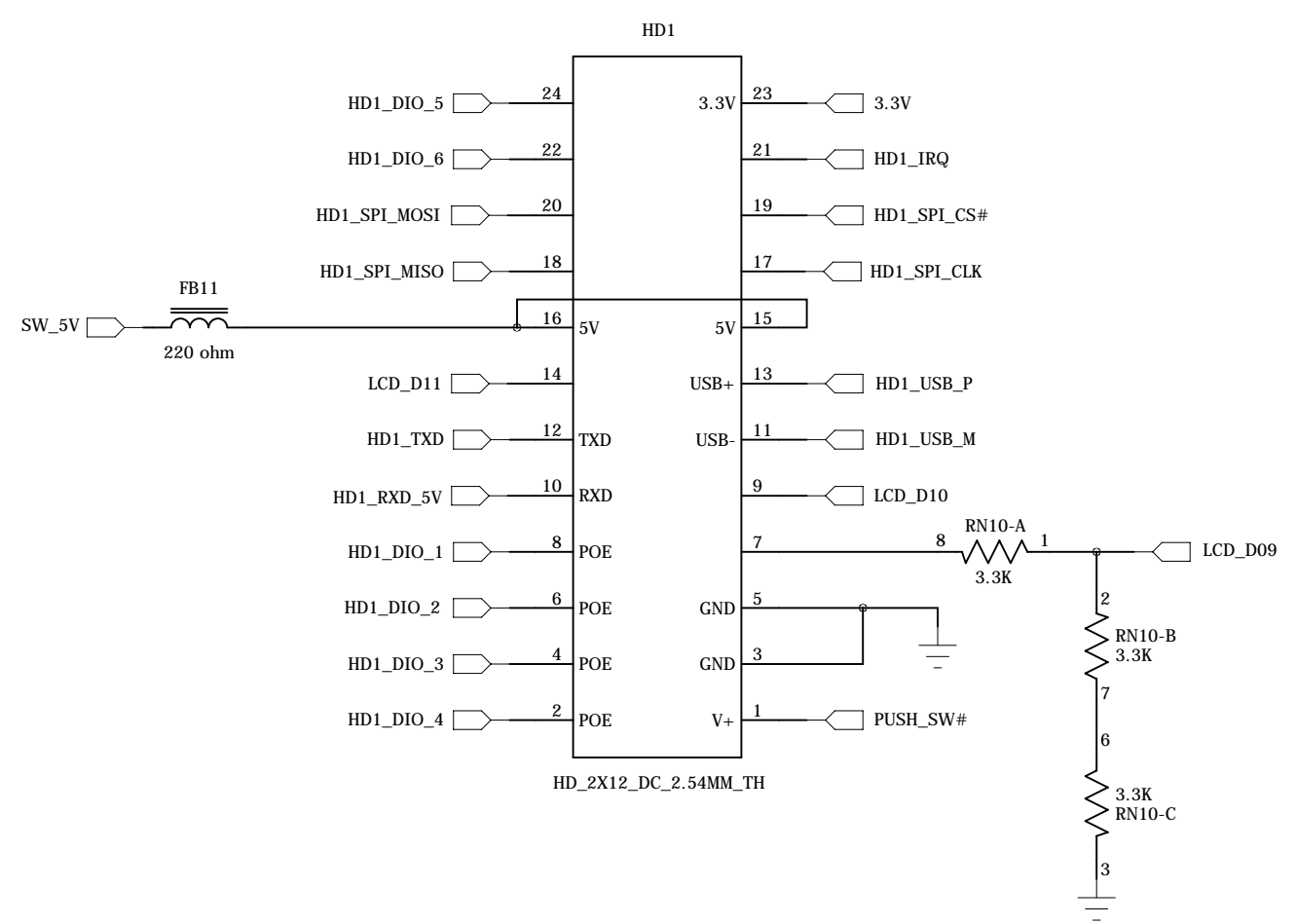
STC RS-485 Driver



Enable USB Console



Daughter Card Interface HD1



Daughter Card Interface HD2

