

## Rev.B Changes

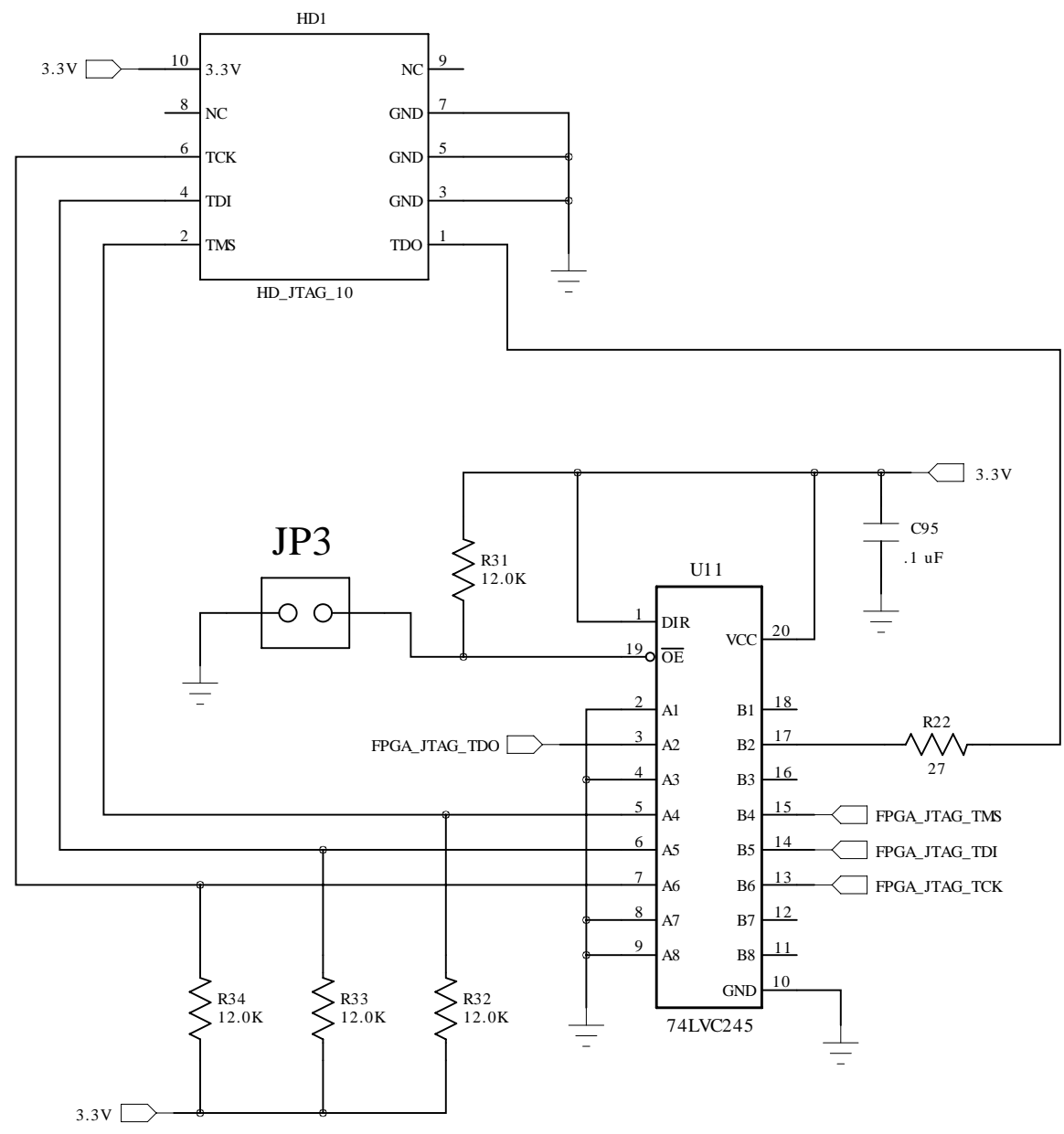
Added R77 (1K resistor)

This is because TS-4200 has 1.8V logic level on CAN\_RXD

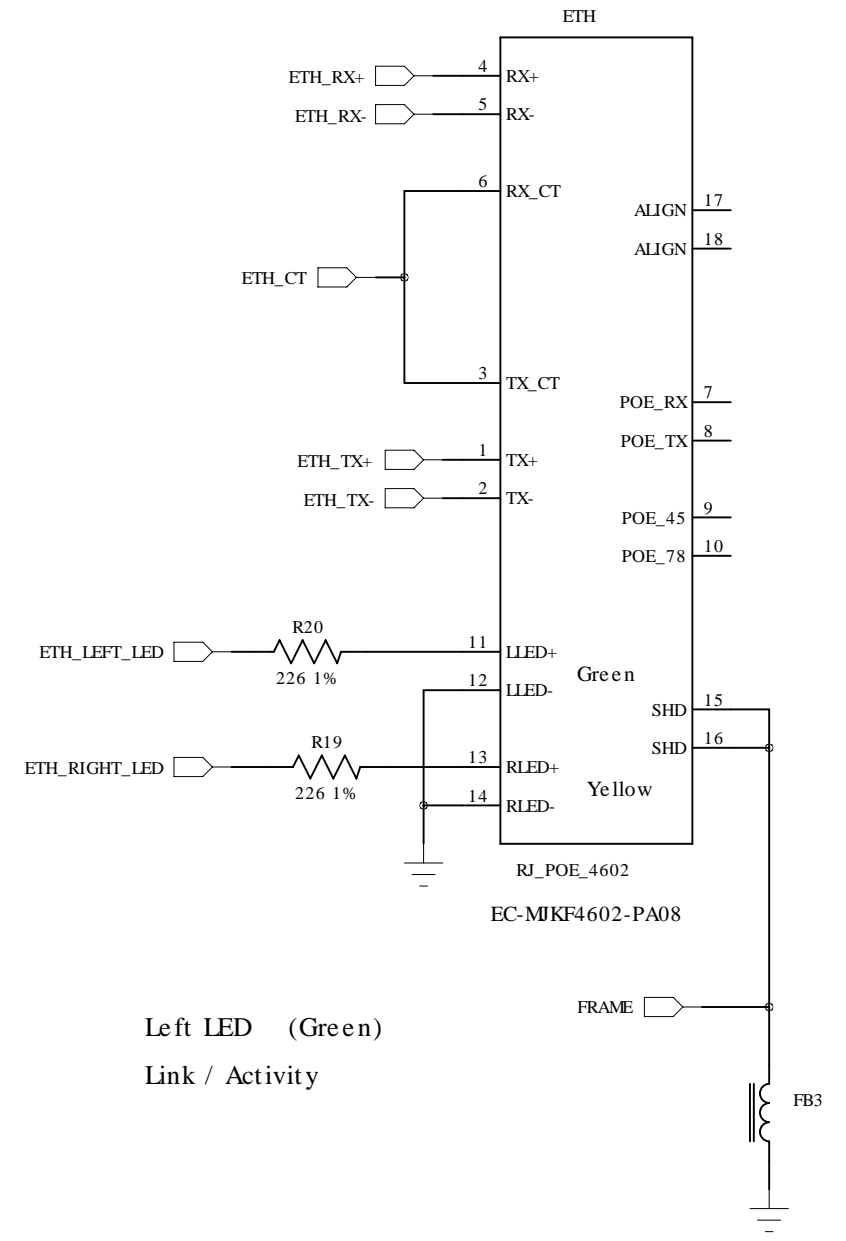
Technologic Systems	Date	Jan. 11, 2016
Title: TS-8200 Documentation		
Rev:	Designer RLM	Sheet 0 of 6

# TS-8200

## FPGA JTAG Header

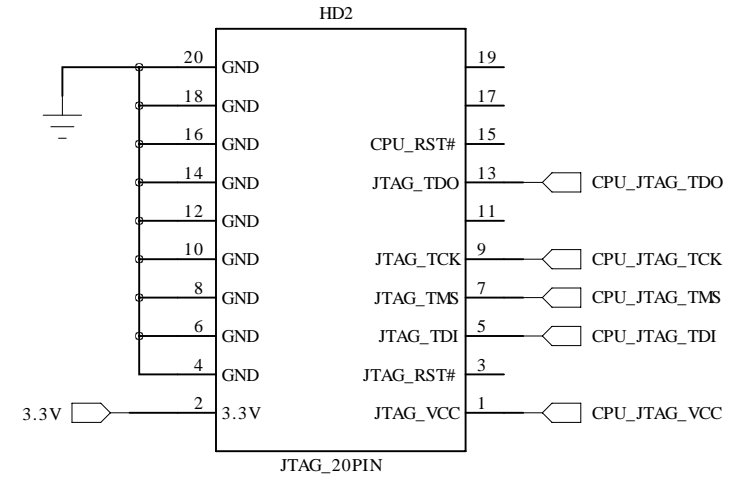


## 10/100 Ethernet



Left LED (Green)  
Link / Activity

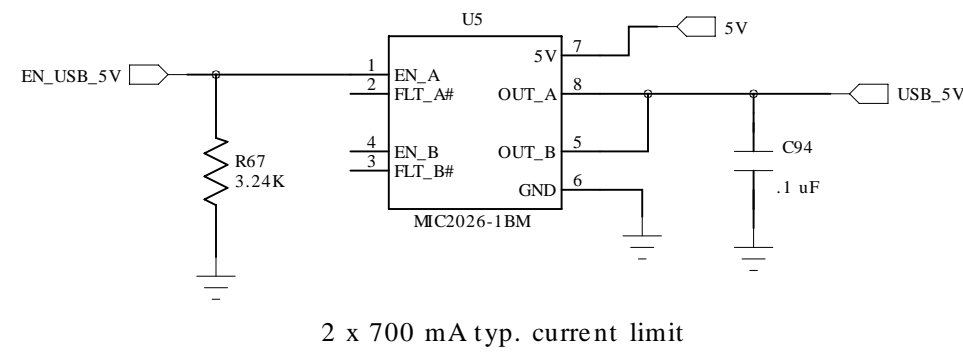
## CPU JTAG Header



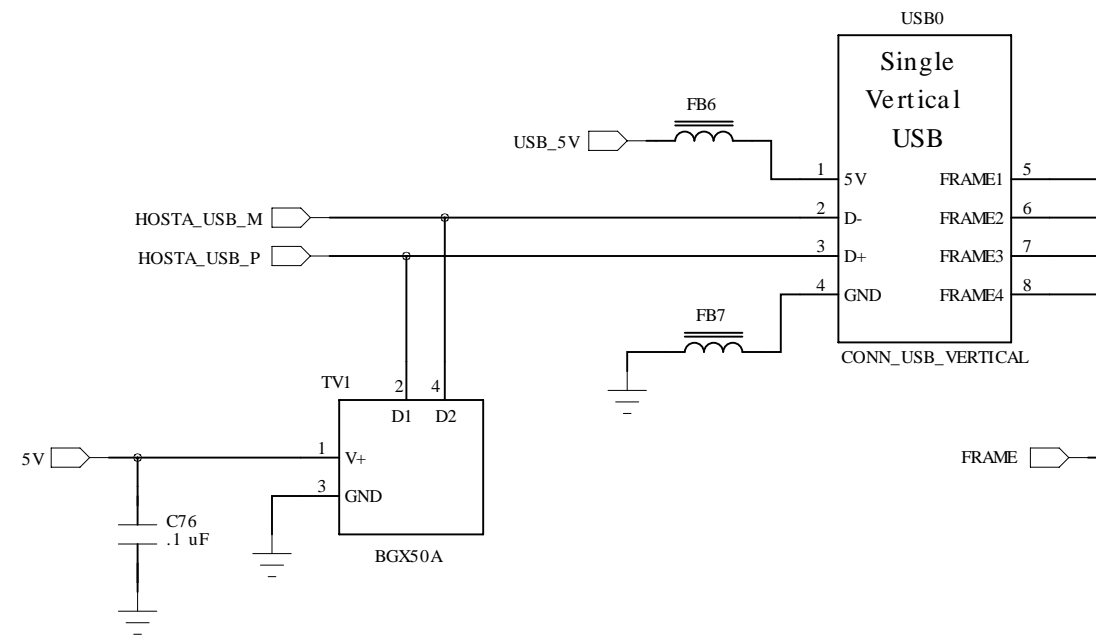
Not Populated

Technologic Systems	Date	March 15, 2010
Title: TS-8200 Ethernet, FPGA JTAG		
Rev:	Designer	Sheet 1 of 6

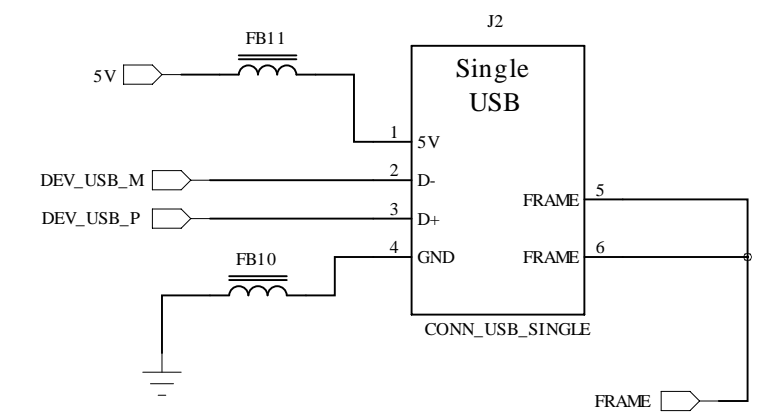
# USB Power Switch



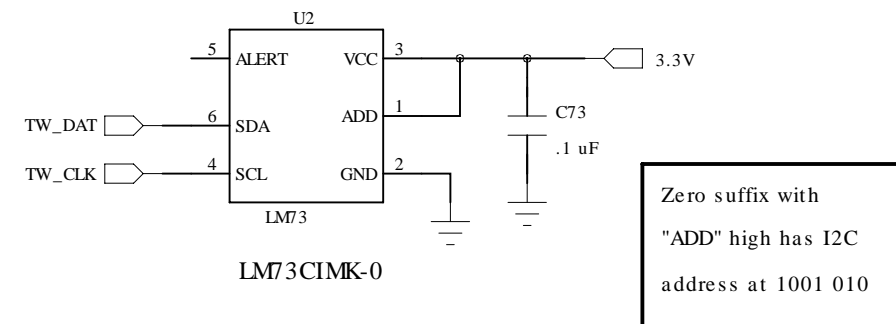
# Host USB



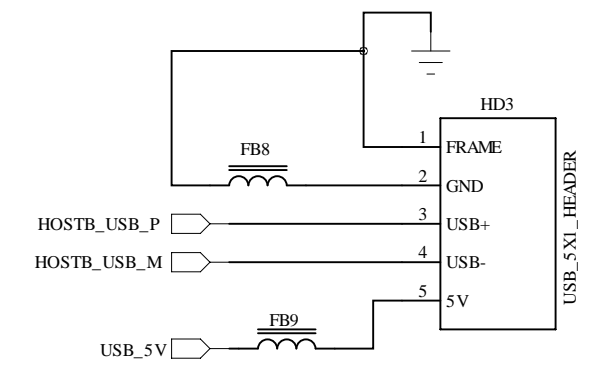
# USB Device



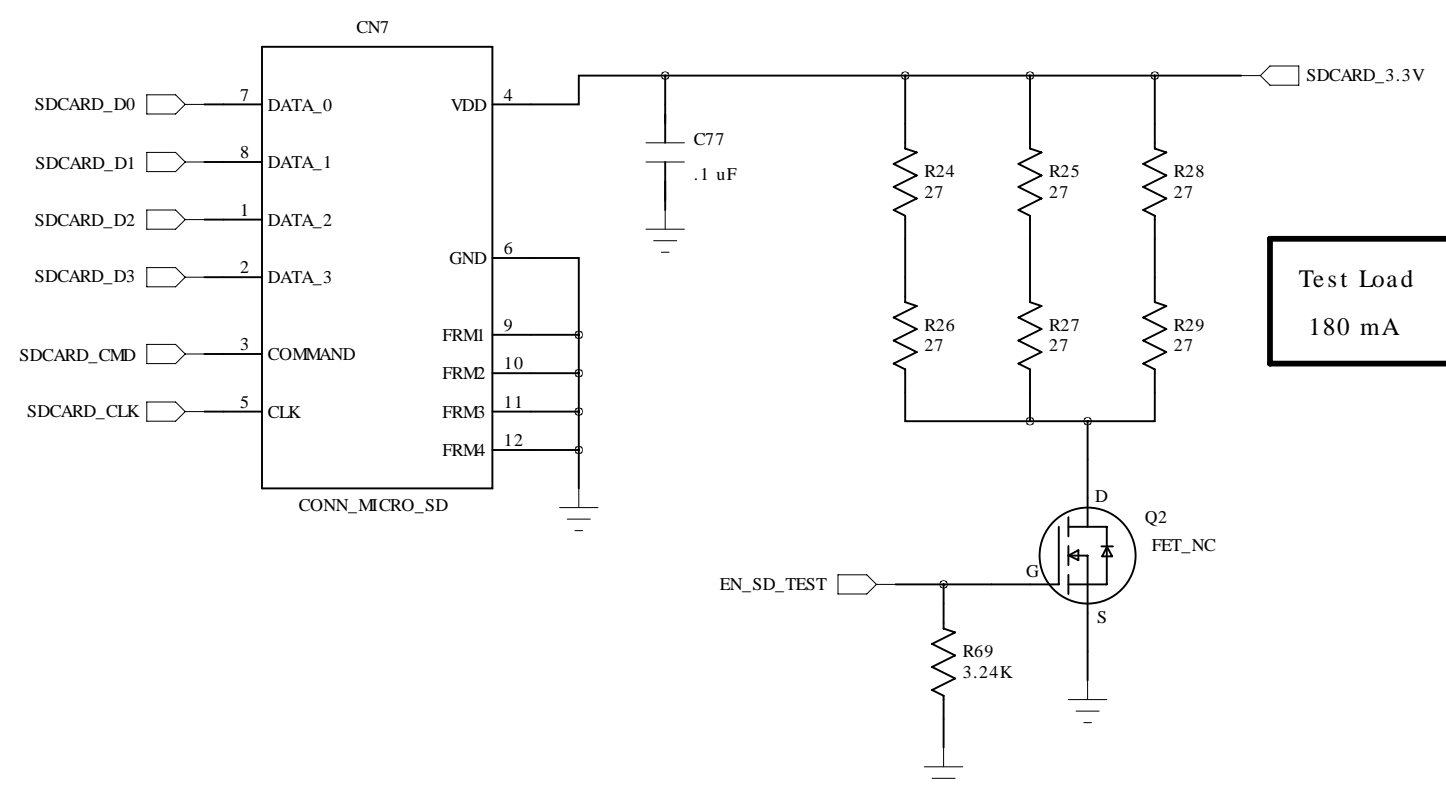
# Temp Sensor



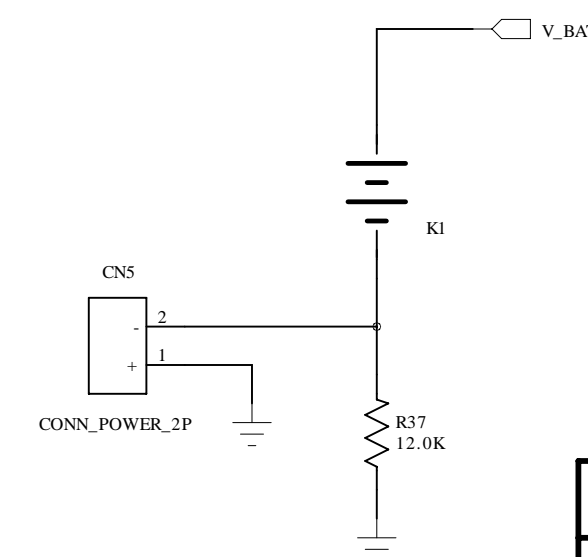
# USB\_B Header



# Micro SD Card Socket



# RTC Battery

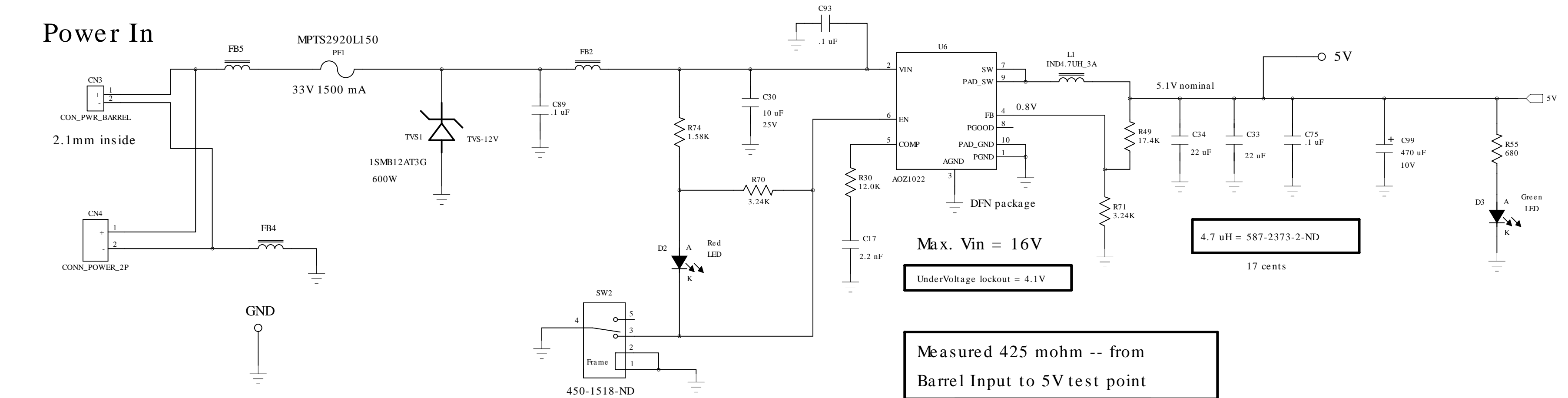


Technologic Systems	Date	March 15, 2010
Title: TS-8200 USB, Serial Flash, SD Card		
Rev:	Designer	Sheet 2 of 6

# 5V to 12V

Power In

# 5V Regulator



Power Switch

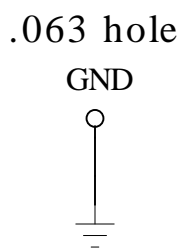
For Production Test  
Fixture only

Max. Vin = 16V  
UnderVoltage lockout = 4.1V

Measured 425 mohm -- from  
Barrel Input to 5V test point  
with 5.0V at Input

PolyFuse	mohms
1500 mA 33V	122
1100 mA 6V	160
750 mA 13V	212

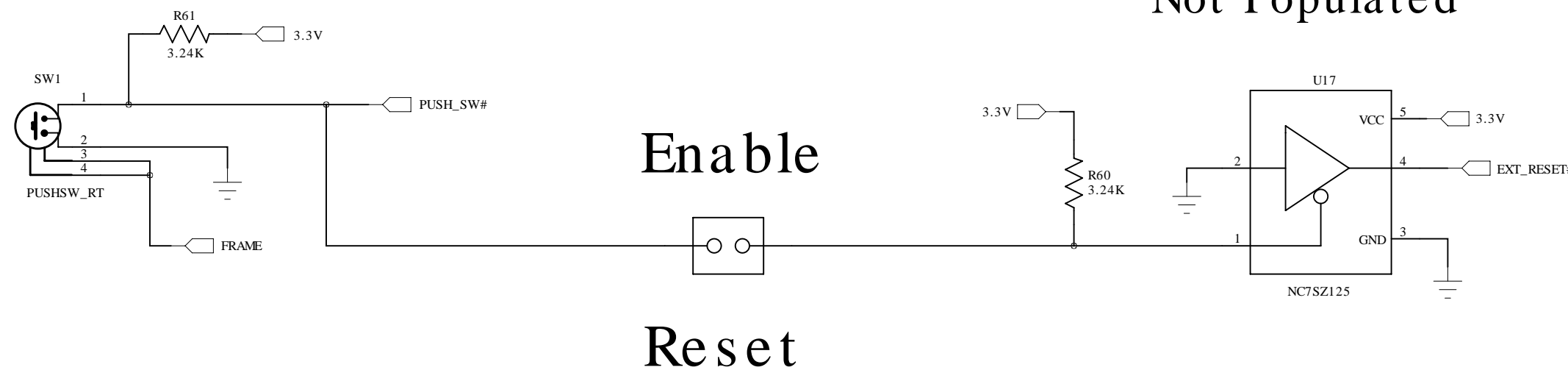
Ferrite beads = 32 mohm



Force Boot  
to SD card

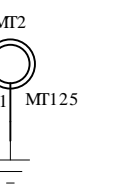
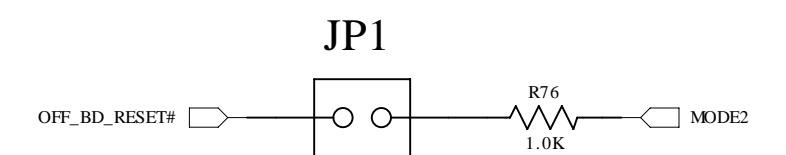
# Push Switch

Not Populated



Enable

Reset



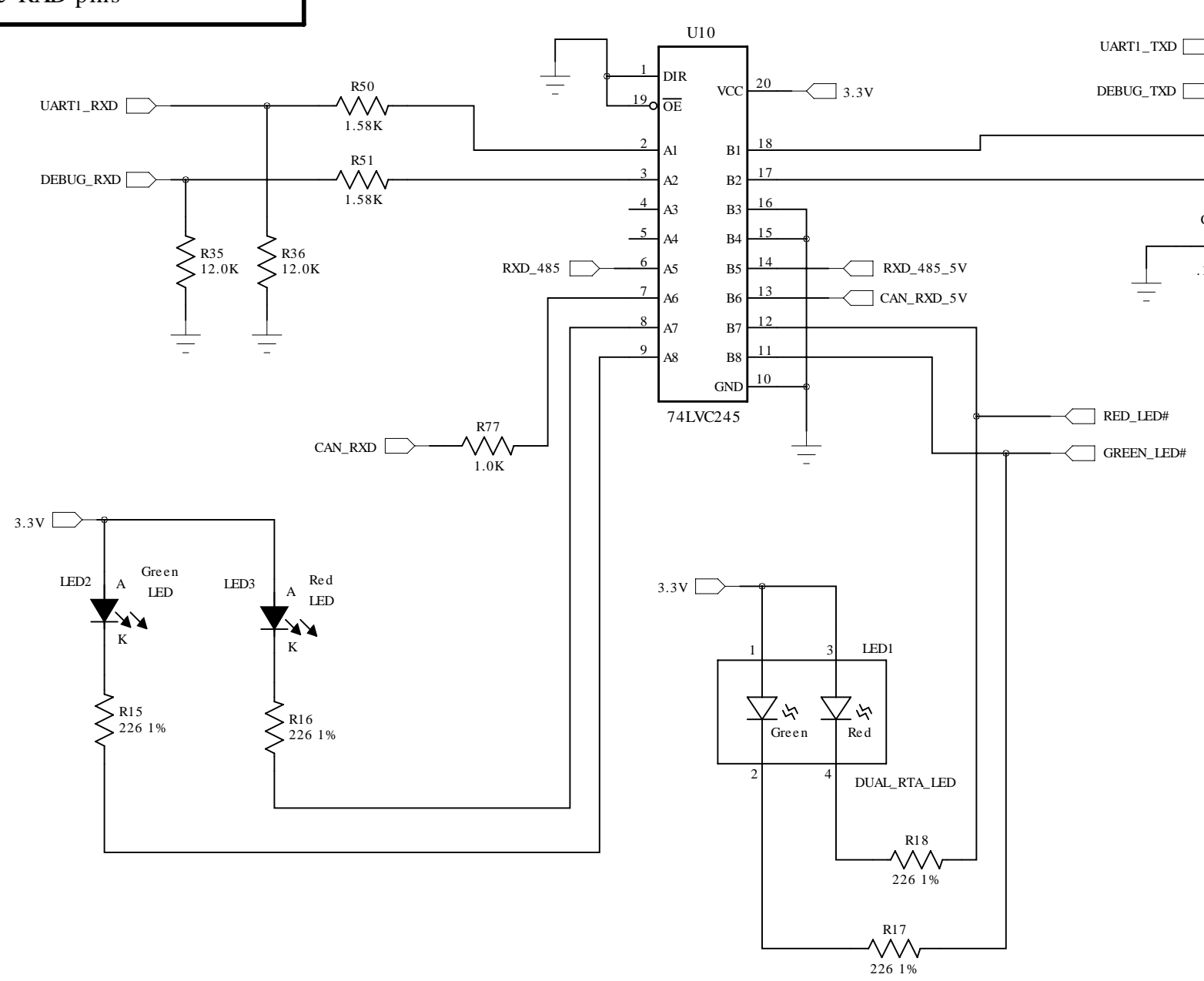
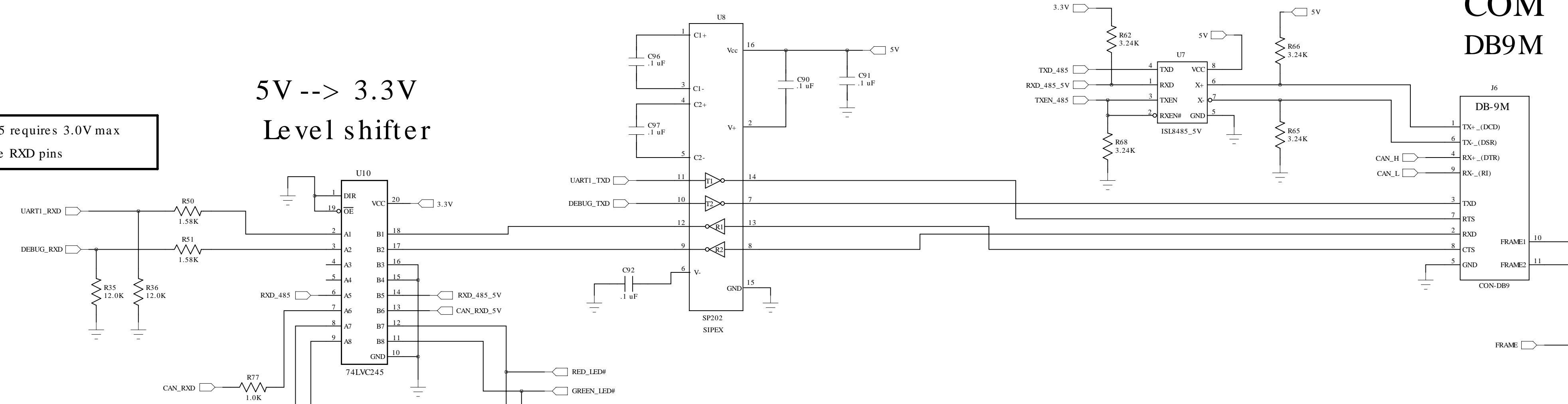
# RS-232 Transceiver

# RS-485 Driver

COM  
DB9M

MX515 requires 3.0V max  
on the RXD pins

5V --> 3.3V  
Level shifter



## For Production Test Fixtures only

### Write Protect 8200 Flash

### 64KB Serial Boot Flash

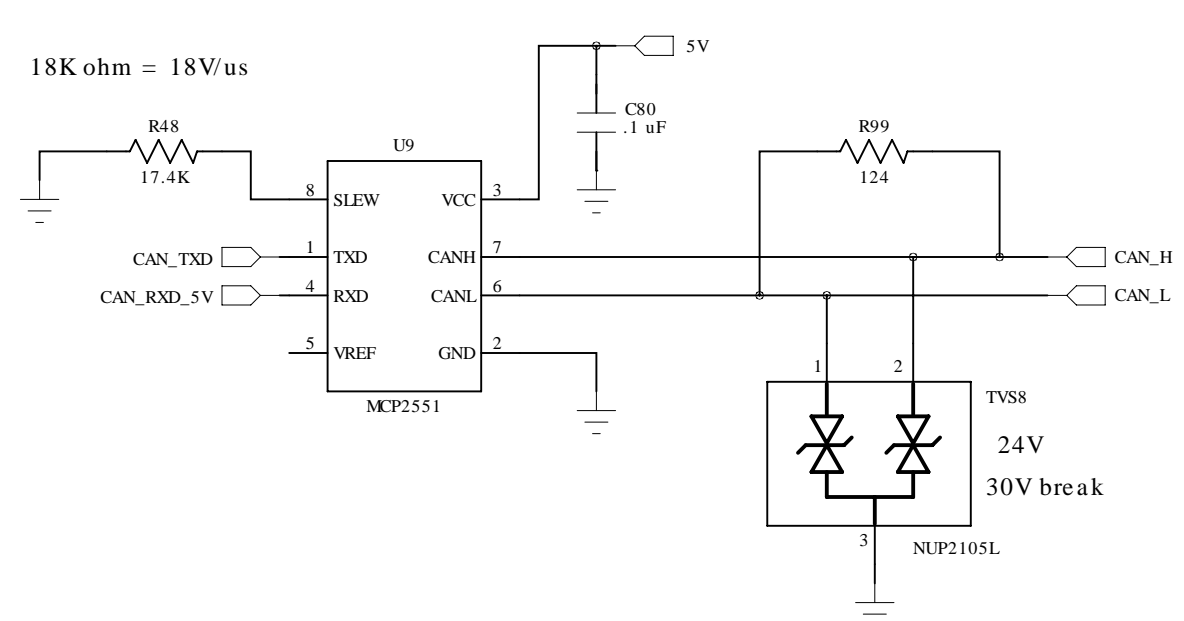
TS-4200 Boot using SPI0 Port

M25P05-AVM = 64Kx8  
50 MHz max. Clock

### Low = select 8200 Flash

SOT-23 package

# CAN Transceiver



# Two 100-pin Module Connectors

"5V" pins supply all power to the module  
Apply 4.5V to 5.5V to these pins

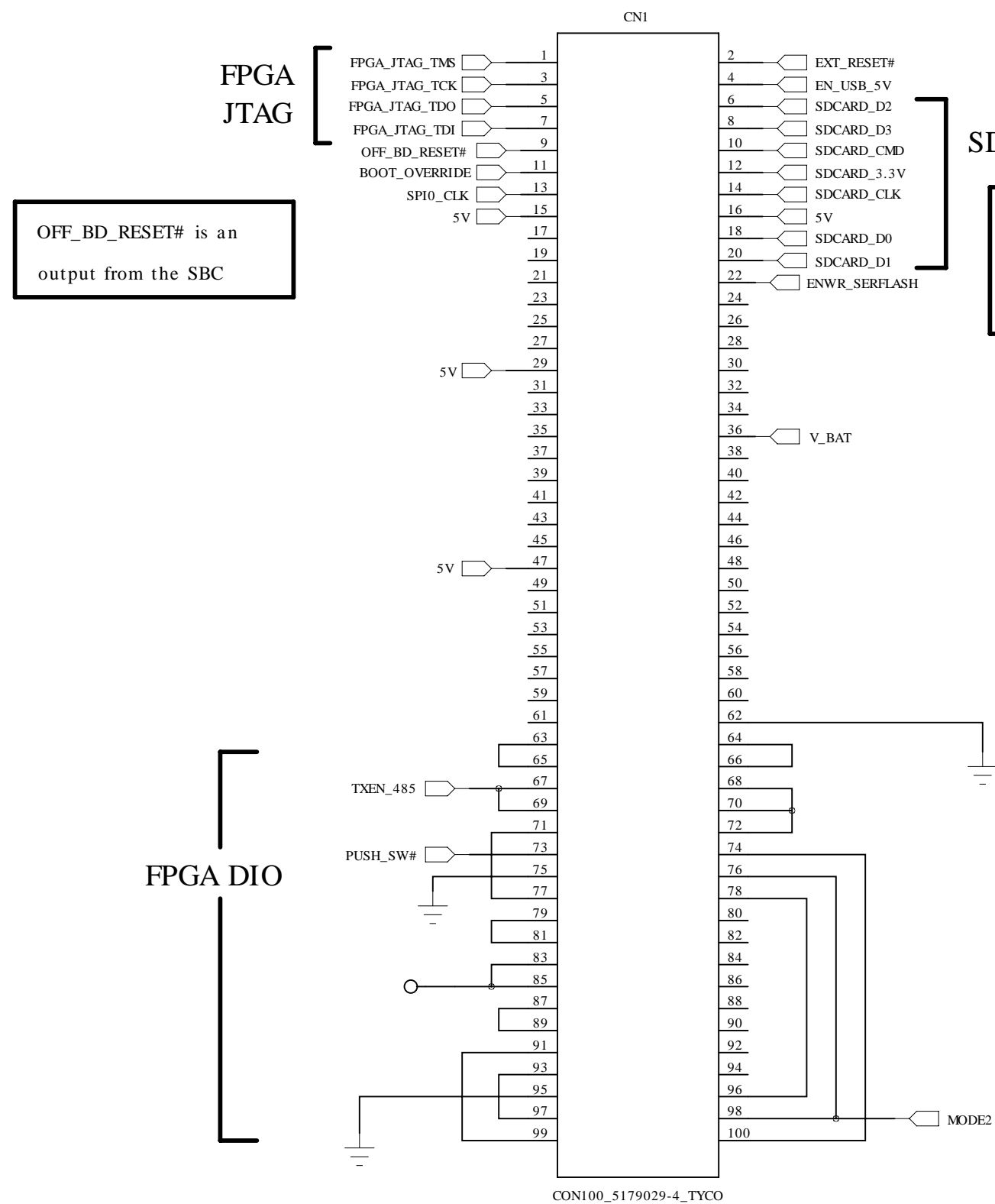
Current drain is < 600 mA  
(less than 3 Watts)

EXT\_RESET# is an Input to the  
SBC used to reboot the CPU

Do not drive active high  
(use open drain)

Left

Right



OFF\_BD\_RESET# is an  
output from the SBC

SD Card

SD card signals on connector  
are wired in parallel with  
SD card socket. Only one  
can be populated with SD card

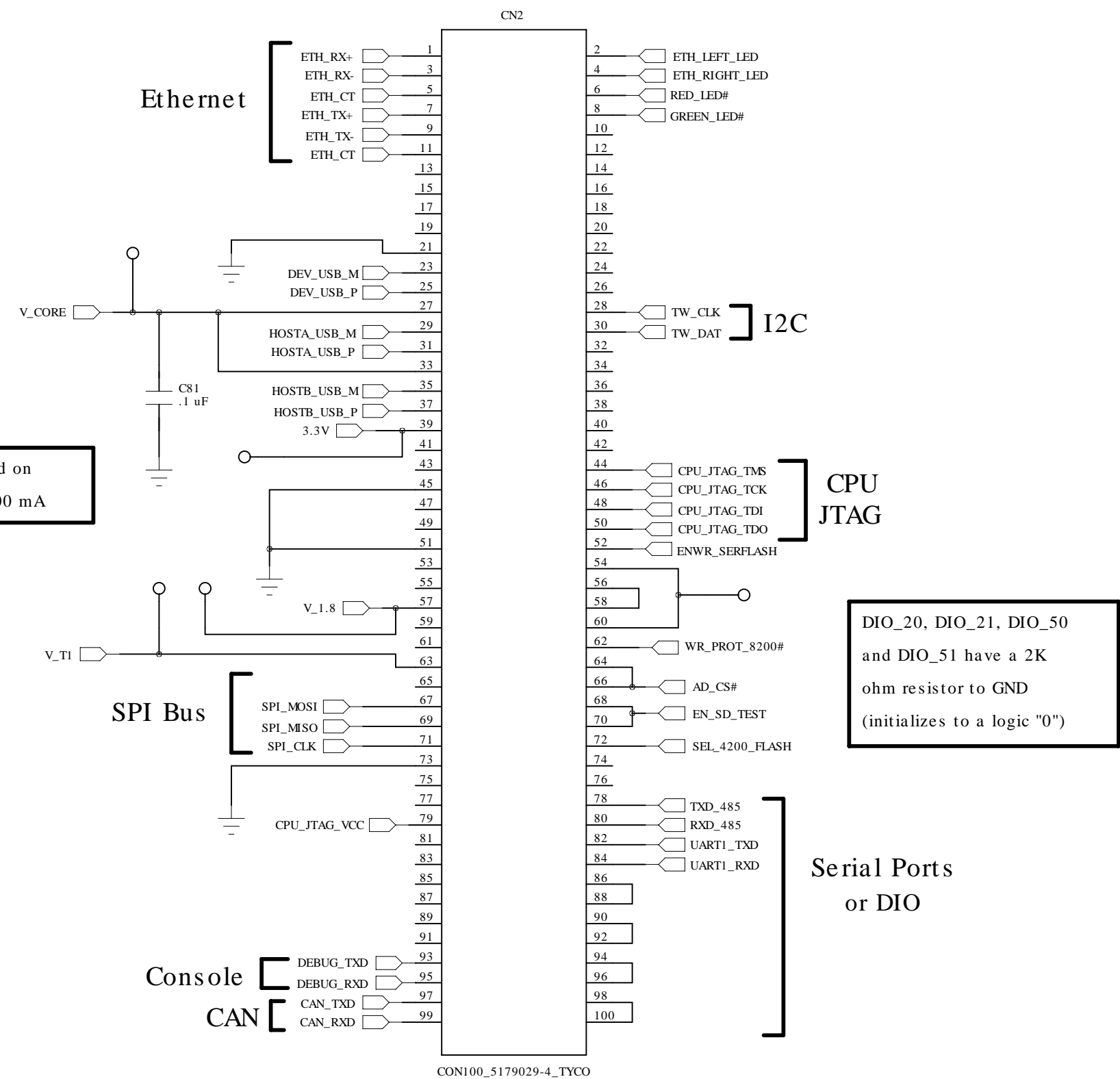
FPGA DIO

Mode 2	Boots from
1	NAND Flash
0	SD Card

MODE1 and MODE2 states  
are latched prior to  
OFF\_BD\_RESET# deasserted

MODE1 and MODE2  
have PU resistors  
on the SBC module

Use 1.5K ohm resistor  
to GND to set low

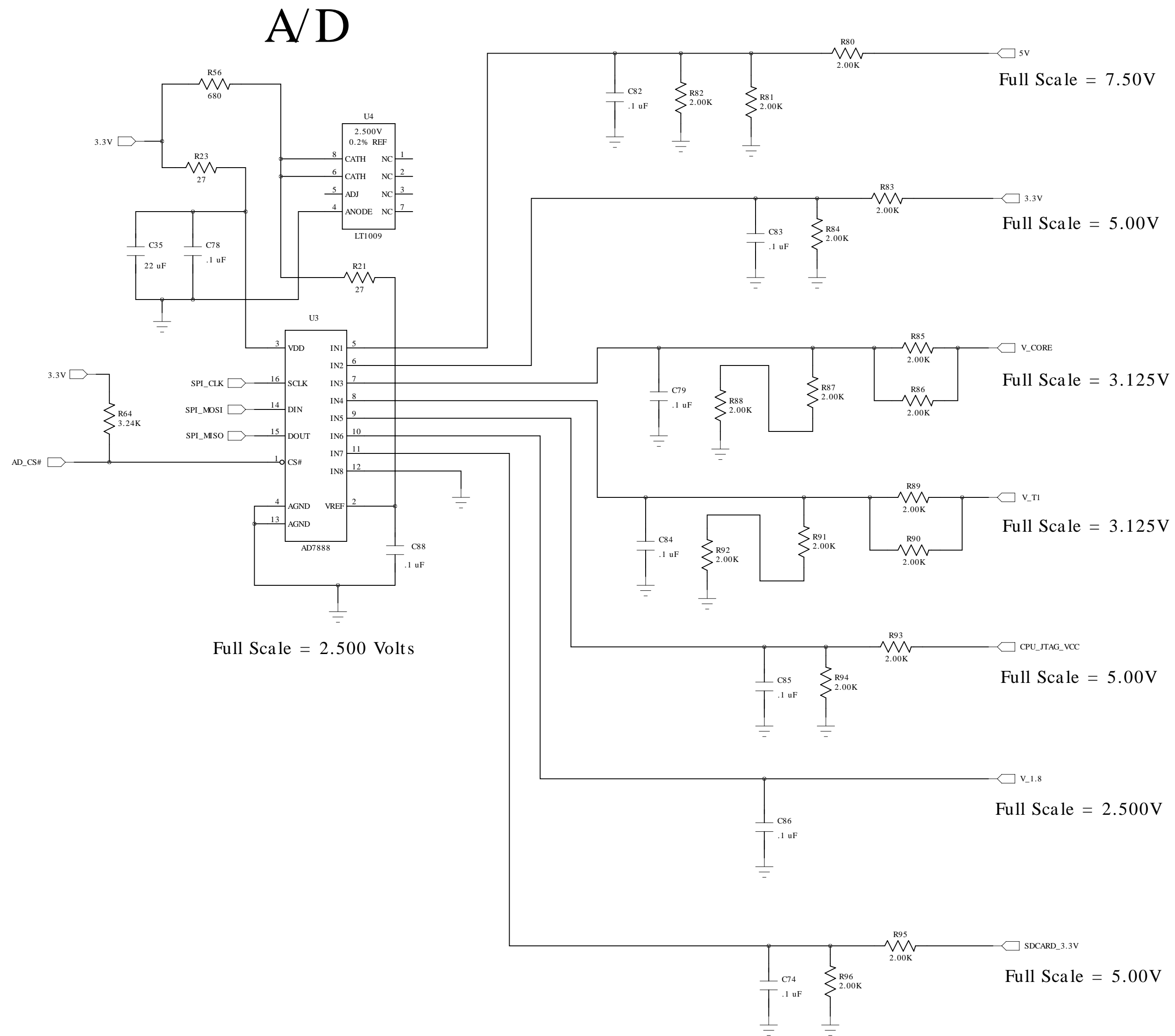


Maximum load on  
3.3V pin is 300 mA

DIO\_20, DIO\_21, DIO\_50  
and DIO\_51 have a 2K  
ohm resistor to GND  
(initializes to a logic "0")

Serial Ports  
or DIO

# For Production Test Fixture Only



R80-R96 0.1% tolerance

P2.0KDBDKR-ND = .1% 0603  
5K Reel is .05 each