Changes from TS-8500 to TS-8550

Changed primary MagJack to 1 Gigabit

Added 2nd MagJack

Removed USB Device port

Fixed CAN problem with TS-4200 (add res)

SATA pins changed on CN2

Add caps to SATA Diff pairs

Allow half-size PCIe conn.

Change to different 5V reg

Add TS-4900 SPI Flash for booting

Add 2x10 JTAG Header (for CPU)

Remove PCIe clock generator

Add USB Hub - 3 external Host ports

Add USB interface to mini-PCIe

Add 1.5V Reg. to mini-PCIe

Remove Temp sensor

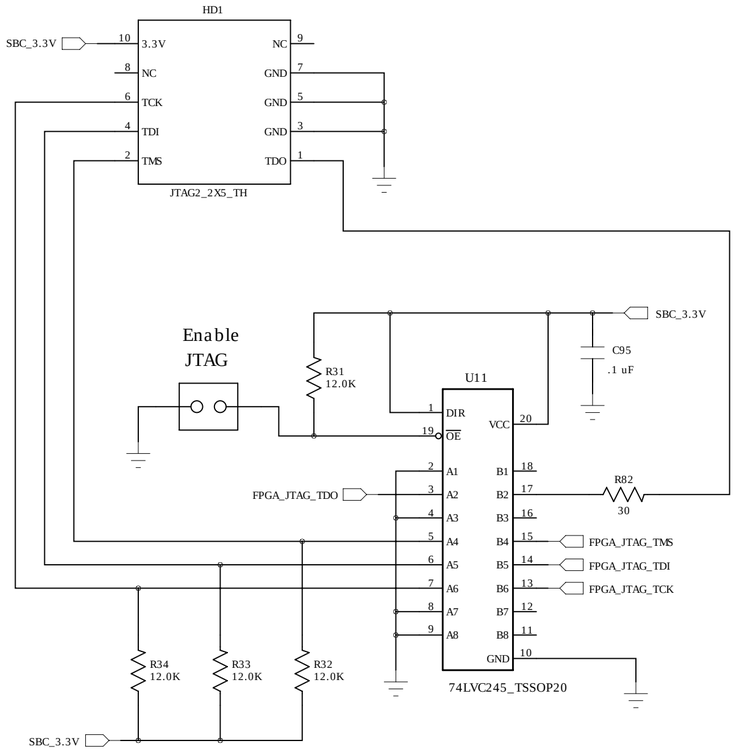
Add Bias Resistors for TS-4900 Boot

Change board ID to Hex 13

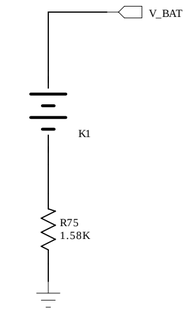
Add Test Point hooks for GND ?

Technologic Systems	Date May 8, 2014	
Title: TS-8550 Documentation		
Rev: A	Designer	Sheet 1 of 9

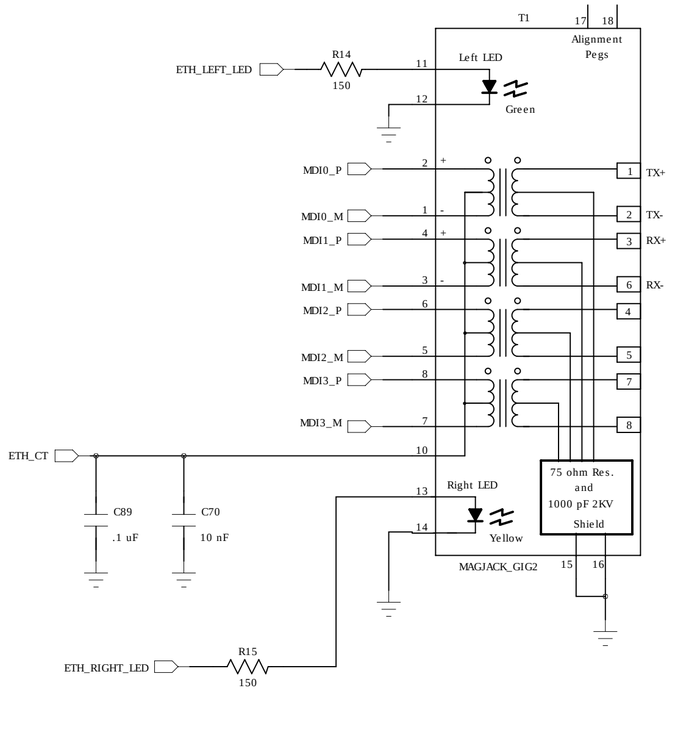
FPGA JTAG Header



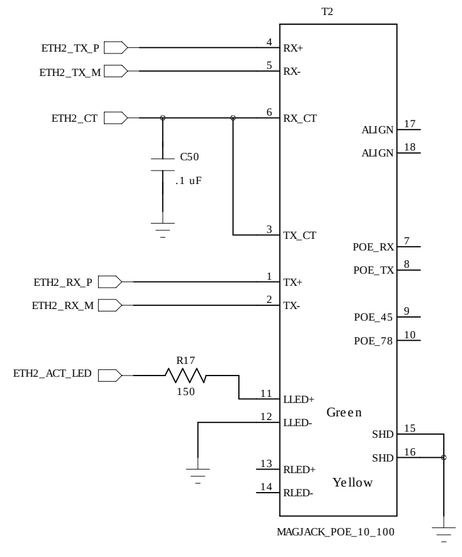
RTC Battery



Gig MagJack



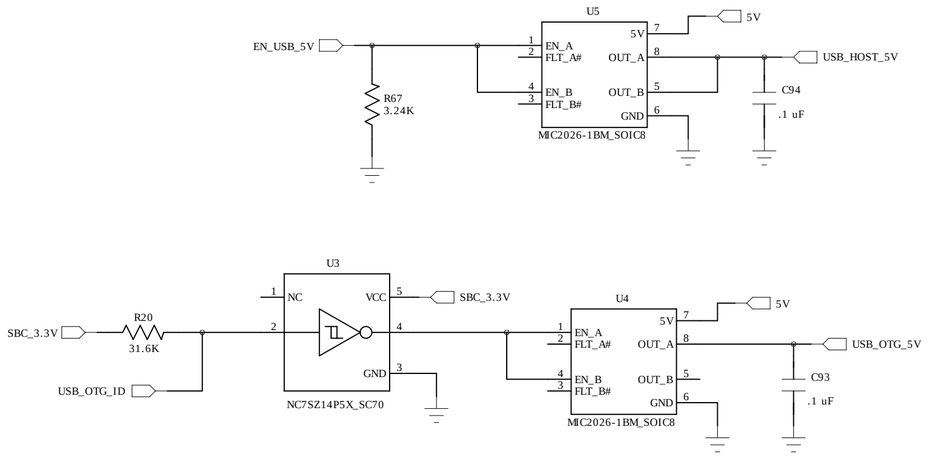
10/100 MagJack



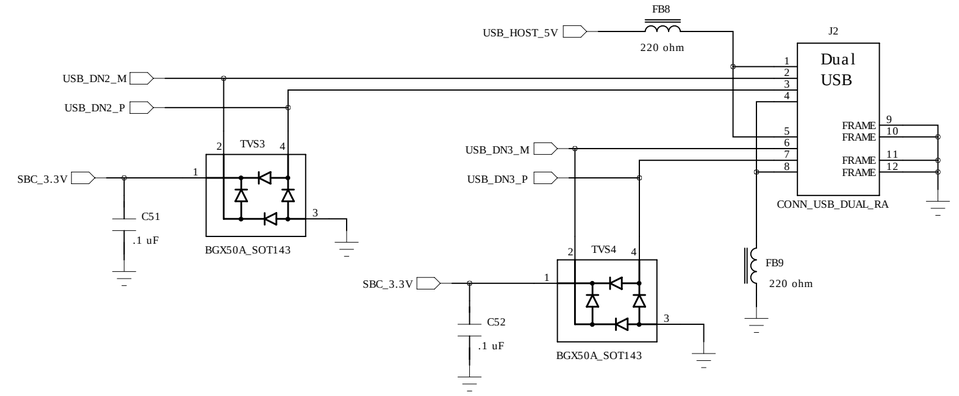
Swapped RX and TX Pairs

Technologic Systems	Date May 8, 2014	
Title: TS-8550 MagJacks, JTAG, Battery		
Rev: A	Designer	Sheet 2 of 9

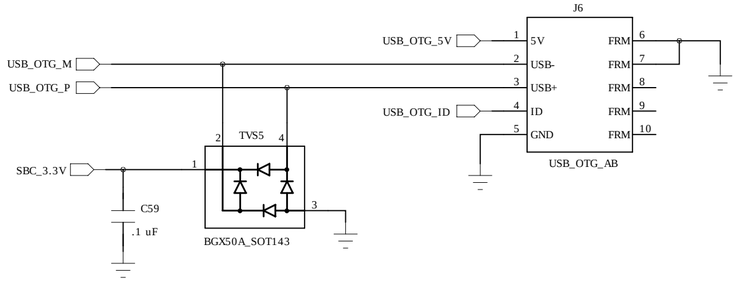
USB Power Switches



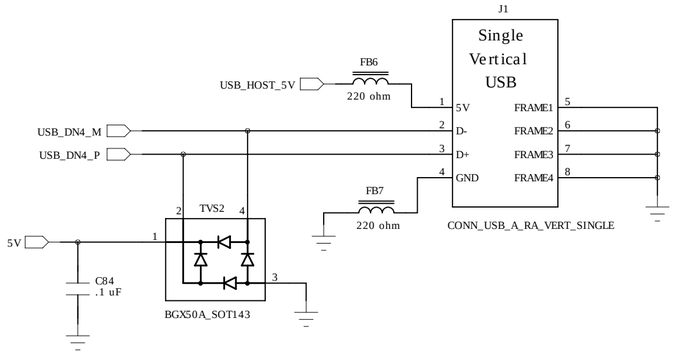
Dual Host USB



USB Micro A/B OTG Port



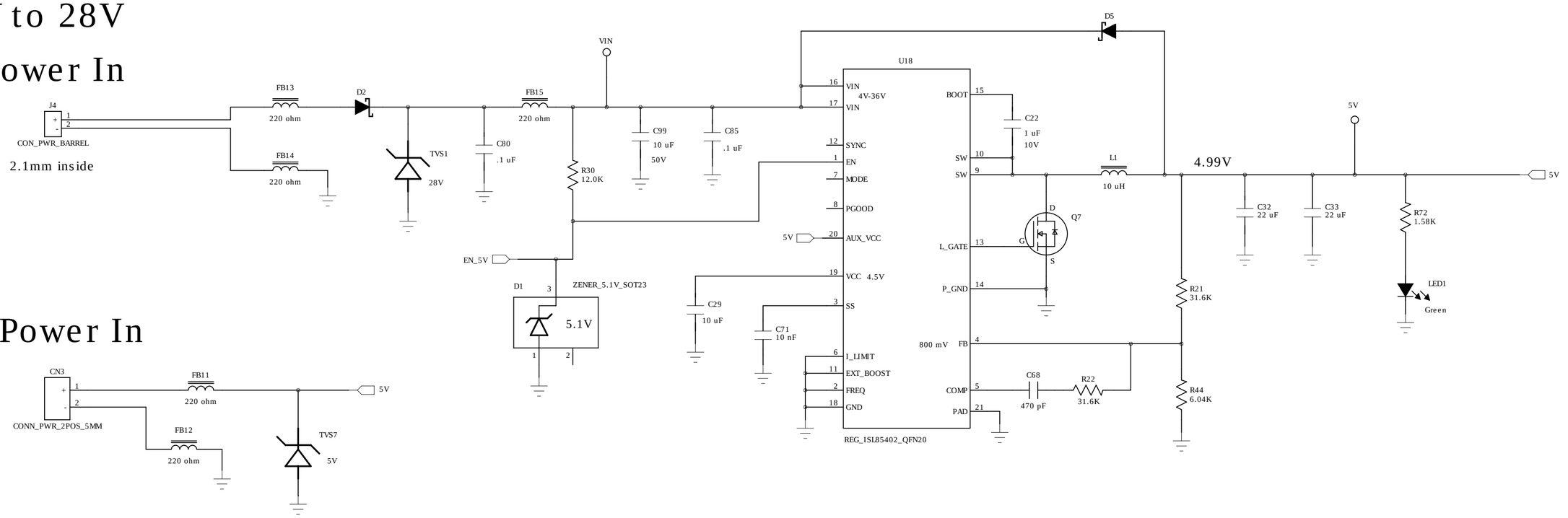
Host USB



Technologic Systems		Date May 8, 2014
Title: TS-8550 USB Ports, USB Power		
Rev: A	Designer	Sheet 3 of 9

5V Power Supply (2000 mA)

8V to 28V Power In



5V Power In

5011K-ND = Black

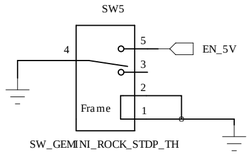
.063 hole

GND

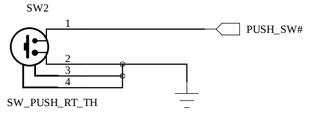
3.3V

SBC_3.3V

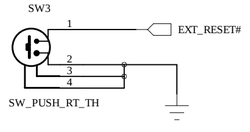
Power Switch

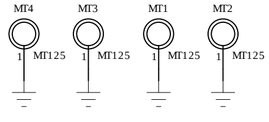


Push Switch



Reset Switch

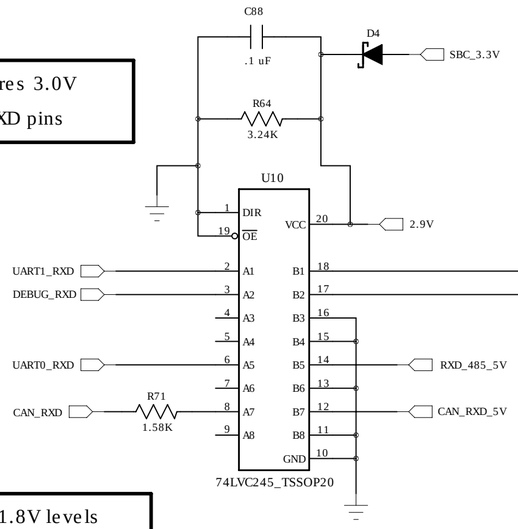




Technologic Systems	Date May 8, 2014	
Title: TS-8550 Power IN, 5V Reg, Switches		
Rev: A	Designer RLM	Sheet 4 of 9

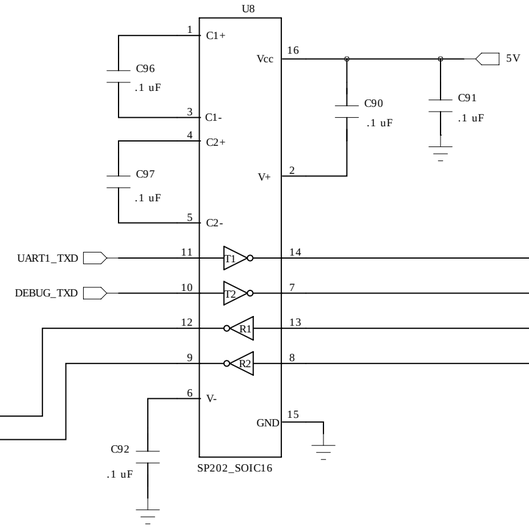
2.9V <-- 5V Level shifter

TS-4800 requires 3.0V max on the RXD pins

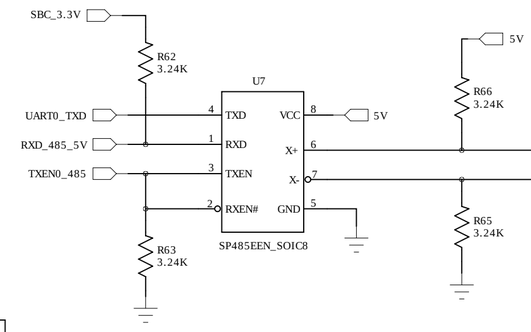


TS-4200 has 1.8V levels on the CAN RXD

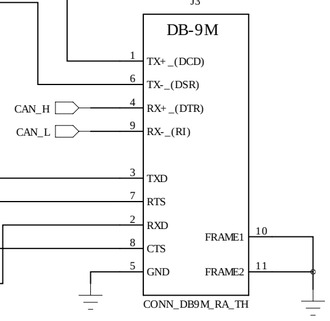
RS-232 Transceiver



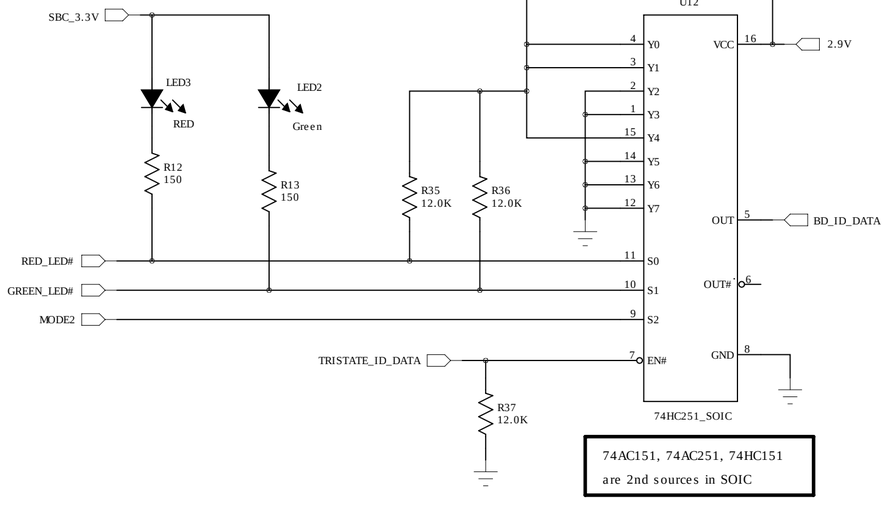
RS-485 Driver



COM DB9M



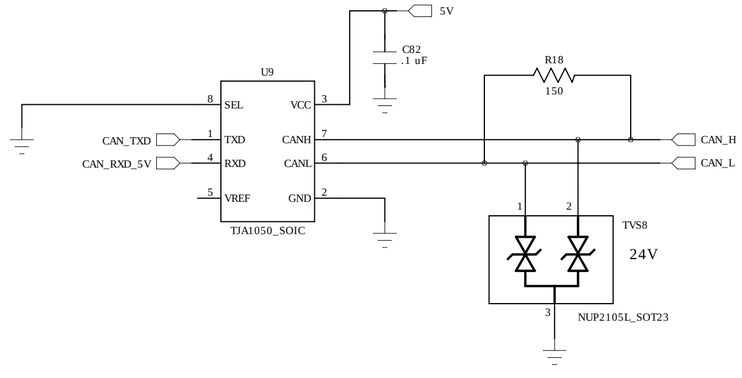
LEDs



Board ID = 19

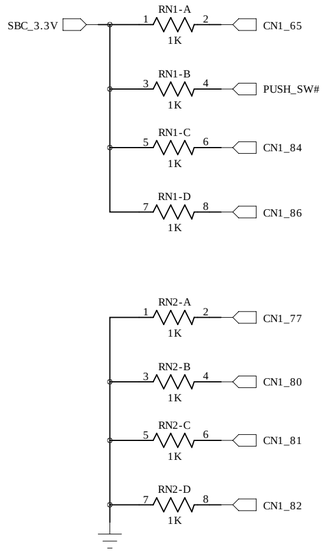
74AC151, 74AC251, 74HC151 are 2nd sources in SOIC

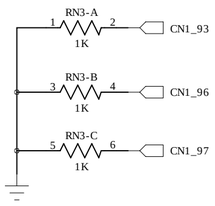
CAN Tranceiver



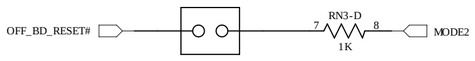
Technologic Systems		Date May 8, 2014
Title: TS-8550 COM Port, CAN, RS-485, ID		
Rev: A	Designer RLM	Sheet 5 of 9

Bias Res.

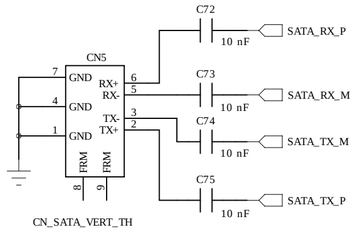




Boot to SD

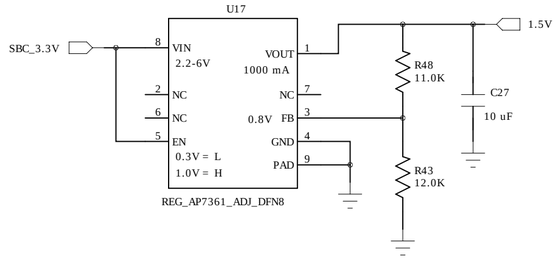


SATA Port



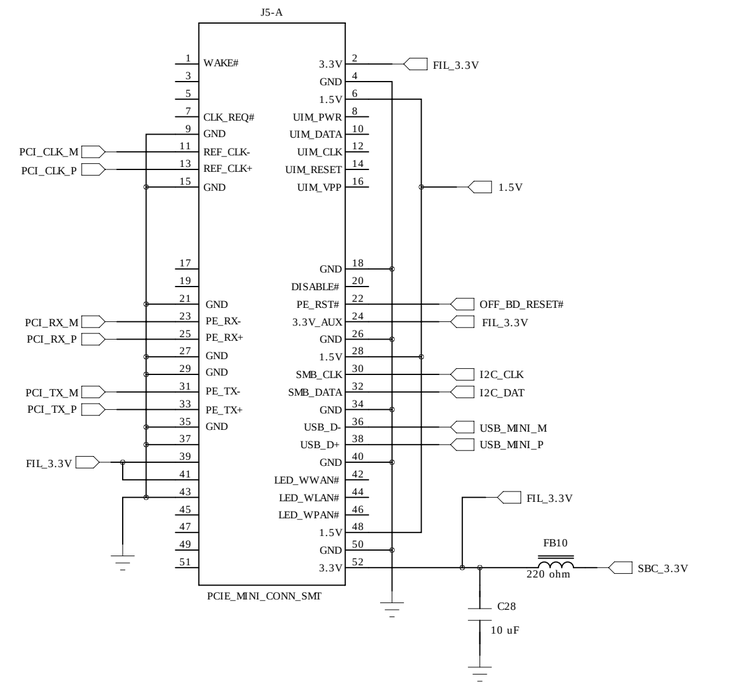
Mini PCIe

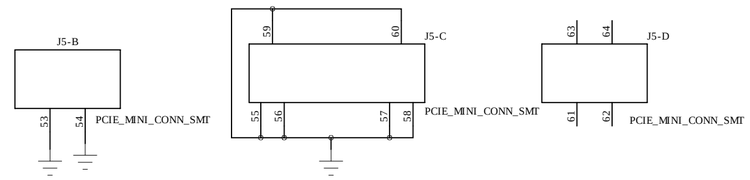
1.5V Reg.

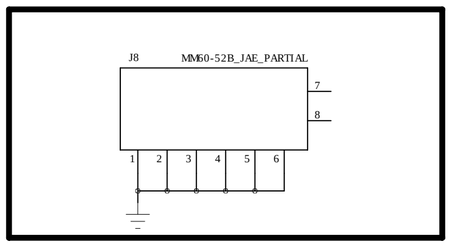


Mini PCIe

Socket





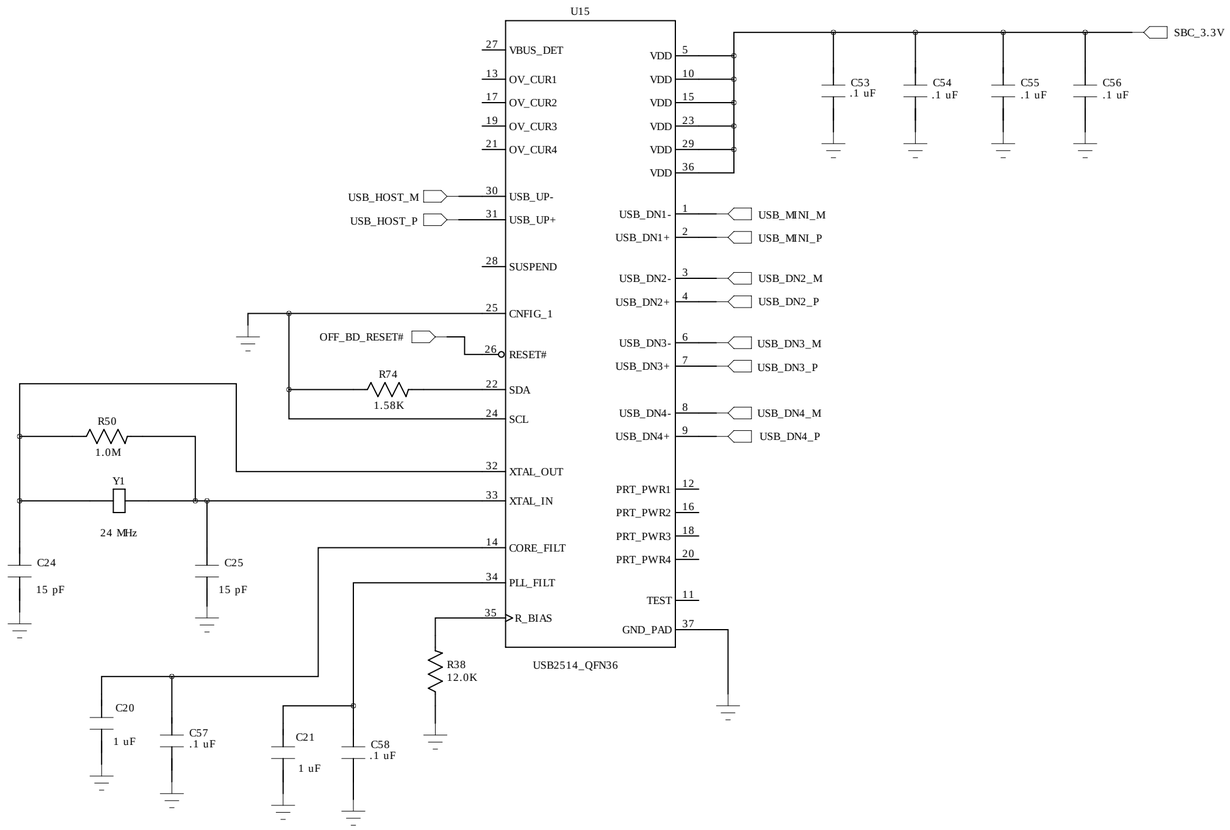


To Support Half-Size Mini-PCIe

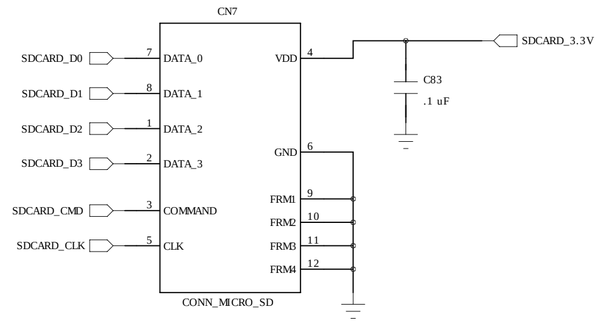
Technologic Systems		Date May 8, 2014
Title: TS-8550 PCIe, SATA, 4900 Bias Res.		
Rev: A	Designer RLM	Sheet 6 of 9

SMSC

USB Hub



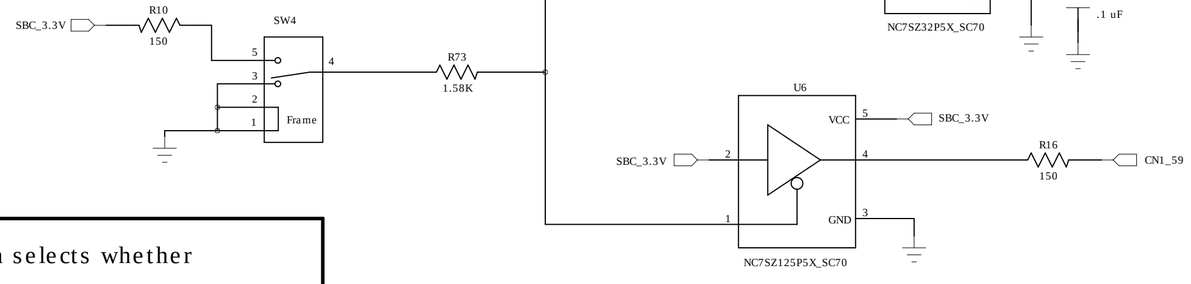
Micro SD Card Socket



TS-4900

SPI Boot Flash

Boot Select Switch

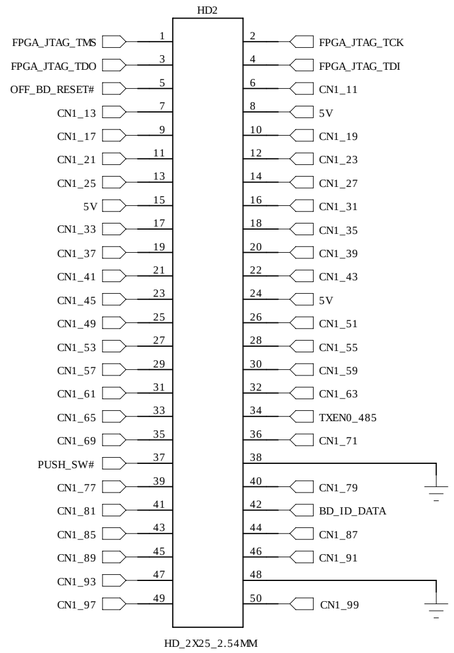


This switch selects whether the TS-4900 SPI Flash or the Base Bd. Flash is used to Boot

CN1_87 allows software to take control of which SPI Flash chip is accessed

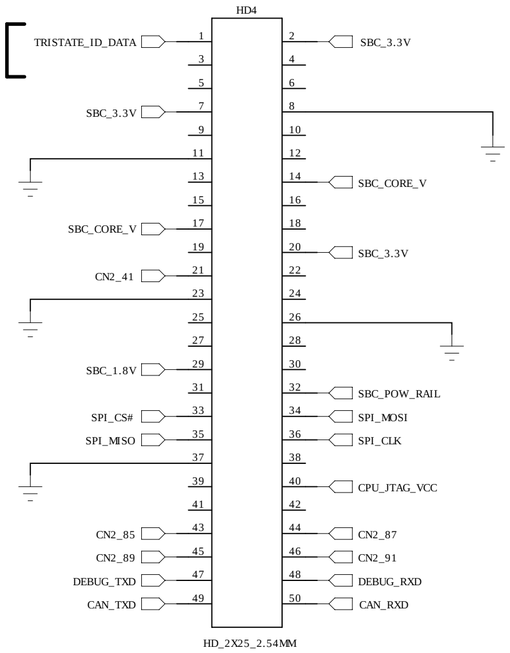
Technologic Systems	Date May 8, 2014	
Title: TS-8550 SPI Flash for 4900, USB Hub		
Rev: A	Designer RLM	Sheet 7 of 9

CN1 Odd Pins



CN2 Odd Pins

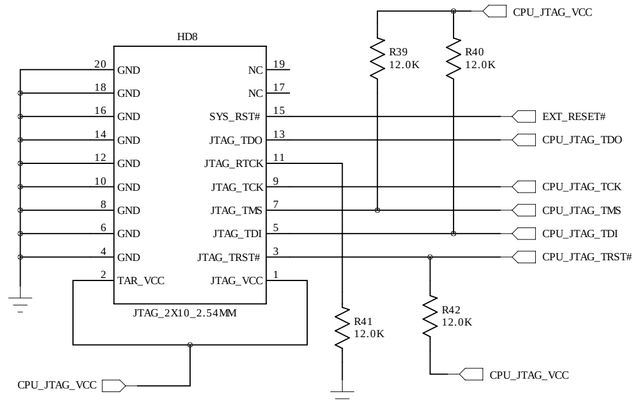
Special signals
Not on CN2



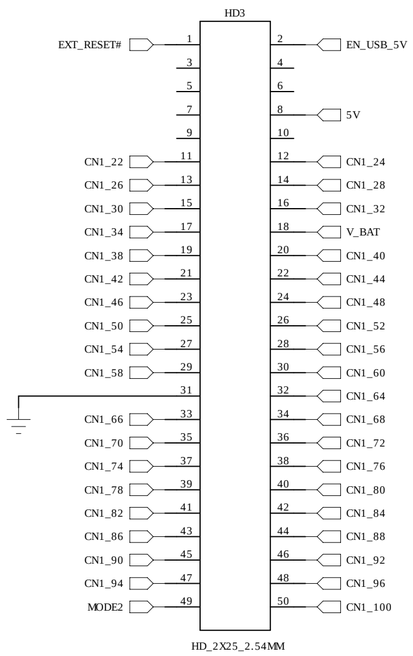
High-speed differential pairs are not routed to these headers

USB, SATA, Ethernet, SD card, PCIe and Ethernet pairs are not connected because this would mismatch the transmission lines.

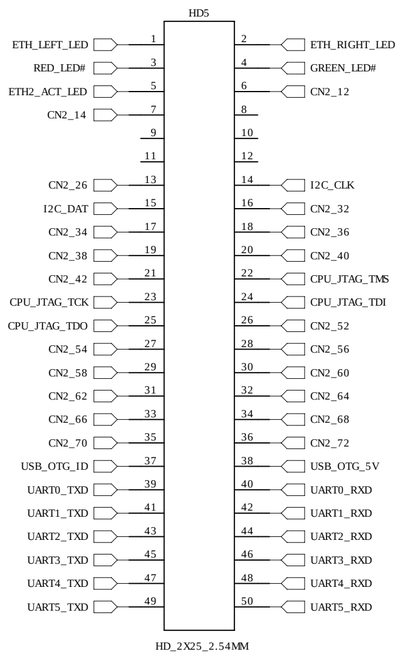
CPU JTAG



CN1 Even Pins



CN2 Even Pins



Technologic Systems	Date May 8, 2014	
Title: TS-8550 CPU JTAG, Headers for SBC		
Rev: A	Designer	Sheet 8 of 9

Two 100-pin Module Connectors

"5V" pins supply all power to the module
Apply 4.5V to 5.5V to these pins

Current drain is < 800 mA
(less than 4 Watts)

EXT_RESET# is an Input to the SBC used to reboot the CPU

Do not drive active high
(use open drain)

Left

CN1

FPGA JTAG: FPGA_JTAG_TMS 1, FPGA_JTAG_TCK 3, FPGA_JTAG_TDO 5, FPGA_JTAG_TDI 7

OFF_BD_RESET# 9

SD Card: SDCARD_D2 6, SDCARD_D3 8, SDCARD_CMD 10, SDCARD_3.3V 12, SDCARD_CLK 14, 5V 16, SDCARD_D0 18, SDCARD_D1 20

SD card signals on connector are wired in parallel with SD card socket. Only one can be populated with SD card

CN1_11	11	2	EXT_RESET#
CN1_13	13	4	EN_USB_5V
5V	15	6	SDCARD_D2
CN1_17	17	8	SDCARD_D3
CN1_19	19	10	SDCARD_CMD
CN1_21	21	12	SDCARD_3.3V
CN1_23	23	14	SDCARD_CLK
CN1_25	25	16	5V
CN1_27	27	18	SDCARD_D0
5V	29	20	SDCARD_D1
CN1_31	31	22	CN1_22
CN1_33	33	24	CN1_24
CN1_35	35	26	CN1_26
CN1_37	37	28	CN1_28
CN1_39	39	30	CN1_30
CN1_41	41	32	CN1_32
CN1_43	43	34	CN1_34
CN1_45	45	36	V_BAT
5V	47	38	CN1_38
CN1_49	49	40	CN1_40
CN1_51	51	42	CN1_42
CN1_53	53	44	CN1_44
CN1_55	55	46	CN1_46
CN1_57	57	48	CN1_48
CN1_59	59	50	CN1_50
CN1_61	61	52	CN1_52
CN1_63	63	54	CN1_54
CN1_65	65	56	CN1_56
TXEN0_485	67	58	CN1_58
CN1_69	69	60	CN1_60
CN1_71	71	62	
PUSH_SW#	73	64	CN1_64
	75	66	CN1_66
CN1_77	77	68	CN1_68
CN1_79	79	70	CN1_70
CN1_81	81	72	CN1_72
BD_ID_DATA	83	74	CN1_74
CN1_85	85	76	CN1_76
CN1_87	87	78	CN1_78
CN1_89	89	80	CN1_80
CN1_91	91	82	CN1_82
CN1_93	93	84	CN1_84
	95	86	CN1_86
CN1_97	97	88	CN1_88
CN1_99	99	90	CN1_90
		92	CN1_92
		94	CN1_94
		96	CN1_96
		98	MODE2
		100	CN1_100

TYCO_100PIN_BASEBOARD

OFF_BD_RESET# is an output from the SBC

Mode 2	Boots from
1	NAND Flash
0	SD Card

MODE2 state is latched prior to OFF_BD_RESET# deasserted

MODE2 has a 12K PU on the SBC module

Right

CN2

Maximum load on 3.3V pin is 500 mA

Gigabit Ethernet: MDI0_P 1, MDI0_M 3, ETH_CT 5, MDI1_P 7, MDI1_M 9, ETH_CT 11

SBC_3.3V 13

MDI2_P 17, MDI2_M 19

MDI3_P 23, MDI3_M 25

SBC_CORE_V 27

C81 .1 uF

USB_HOST_M 29, USB_HOST_P 31

USB_OTG_M 35, USB_OTG_P 37

SBC_3.3V 39

CN2_41 41

CPU_JTAG_TRST# 43

PCI_TX_M 47, PCI_TX_P 49

PCI_RX_M 53, PCI_RX_P 55

SBC_1.8V 57

PCI_CLK_M 59, PCI_CLK_P 61

SBC_POW_RAIL 63

SPI Bus: SPI_CS# 65, SPI_MOSI 67, SPI_MISO 69, SPI_CLK 71

SATA_RX_M 75, SATA_RX_P 77

CPU_JTAG_VCC 79

SATA_TX_M 81, SATA_TX_P 83

CN2_85 85, CN2_87 87, CN2_89 89, CN2_91 91

Console: DEBUG_TXD 93, DEBUG_RXD 95

CAN: CAN_TXD 97, CAN_RXD 99

CN2_63 ??

2nd Ethernet: ETH2_RX_P 16, ETH2_RX_M 18, ETH2_CT 20, ETH2_TX_P 22, ETH2_TX_M 24

I2C: I2C_CLK 28, I2C_DAT 30

CPU JTAG: CPU_JTAG_TMS 44, CPU_JTAG_TCK 46, CPU_JTAG_TDI 48, CPU_JTAG_TDO 50

Serial Ports or DIO: UART0_TXD 78, UART0_RXD 80, UART1_TXD 82, UART1_RXD 84, UART2_TXD 86, UART2_RXD 88, UART3_TXD 90, UART3_RXD 92, UART4_TXD 94, UART4_RXD 96, UART5_TXD 98, UART5_RXD 100

MDI0_P	1	2	ETH_LEFT_LED
MDI0_M	3	4	ETH_RIGHT_LED
ETH_CT	5	6	RED_LED#
MDI1_P	7	8	GREEN_LED#
MDI1_M	9	10	ETH2_ACT_LED
ETH_CT	11	12	CN2_12
SBC_3.3V	13	14	CN2_14
	15	16	ETH2_RX_P
MDI2_P	17	18	ETH2_RX_M
MDI2_M	19	20	ETH2_CT
	21	22	ETH2_TX_P
MDI3_P	23	24	ETH2_TX_M
MDI3_M	25	26	CN2_26
SBC_CORE_V	27	28	I2C_CLK
USB_HOST_M	29	30	I2C_DAT
USB_HOST_P	31	32	CN2_32
	33	34	CN2_34
USB_OTG_M	35	36	CN2_36
USB_OTG_P	37	38	CN2_38
SBC_3.3V	39	40	CN2_40
CN2_41	41	42	CN2_42
CPU_JTAG_TRST#	43	44	CPU_JTAG_TMS
	45	46	CPU_JTAG_TCK
PCI_TX_M	47	48	CPU_JTAG_TDI
PCI_TX_P	49	50	CPU_JTAG_TDO
	51	52	CN2_52
PCI_RX_M	53	54	CN2_54
PCI_RX_P	55	56	CN2_56
SBC_1.8V	57	58	CN2_58
PCI_CLK_M	59	60	CN2_60
PCI_CLK_P	61	62	CN2_62
SBC_POW_RAIL	63	64	CN2_64
SPI_CS#	65	66	CN2_66
SPI_MOSI	67	68	CN2_68
SPI_MISO	69	70	CN2_70
SPI_CLK	71	72	CN2_72
	73	74	USB_OTG_ID
SATA_RX_M	75	76	USB_OTG_5V
SATA_RX_P	77	78	UART0_TXD
CPU_JTAG_VCC	79	80	UART0_RXD
SATA_TX_M	81	82	UART1_TXD
SATA_TX_P	83	84	UART1_RXD
CN2_85	85	86	UART2_TXD
CN2_87	87	88	UART2_RXD
CN2_89	89	90	UART3_TXD
CN2_91	91	92	UART3_RXD
DEBUG_TXD	93	94	UART4_TXD
DEBUG_RXD	95	96	UART4_RXD
CAN_TXD	97	98	UART5_TXD
CAN_RXD	99	100	UART5_RXD

TYCO_100PIN_BASEBOARD

Technologic Systems	Date May 8, 2014	
Title: TS-8550 Dual 100-pin Module Connectors		
Rev: A	Designer RLM	Sheet 9 of 9