The TS-8551 is an evaluation platform for the TS-4100 and TS-4400. This platform brings out all major features of these Computer on Modules for development and evaluation purposes. This platform can also be used as a reference design for creating a custom carrier/baseboard solution for the TS-4100 and/or the TS-4400.
Warning:
The TS-8551 was designed for the TS-4100 and TS-4400
Other macrocontrollers can be used, but
care must be exercised when SuperCap is charged

Rev. A Changes

Removed rechargeable battery
FRAM (U35) write protect to 3.3V always
Changed C68 to 1000 pF (quieter)
Changed both SW2 and SW3 to top push button
Removed silkscreen label for FRAM Prot

Added for TS-4400 support:

CN99-2 for virgin TS-4400 bring up
M.2 SATA conn (CN5) added
Battery jumper to CN1 pin 36
Gig MagJack

10/100 MagJack

CPU JTAG

FRAM Memory

2K Bytes
Host USB Power Switch

USB OTG Micro AB

Host USB Single Vertical USB
3.3V <-- 5V
Level shifter

RS-232 Transceiver

Board ID = Hex 16
Identifies board to TS-4100 and TS-4400 as being the TS-8551
Refer to the Users Guides for these products for information on setting a custom ID

CAN Transceiver

RS-485 Driver

COM DB9M
Jumpers

SD Boot
No SupCap Charge
U-Boot

Internal Test

2 x 25 Farad Super Caps

R21, 22 will discharge SuperCaps
These Resistors are Not Recommended for Custom Baseboards

Super Cap balance circuit

ST Micro RTC

Only installed for TS-4400
**M2 SATA Conn.  TS-4400 Only**

**SSD Current**

200 mA at 500 mA load

500 mV @ 500 mA

**M2 SSD**

SSD Activity

**Boot Switch**

LED On = USB Boot

"1" = USB Boot

**M2 Mount**

22 x 80mm

2 mm height

No SATA support on TS-4100

TS-4400 Supports SATA at 3 Gbit/sec

"1" = USB Boot

Allows TS-4100 booting to either eMMC or over the USB OTG port
Breakout Connectors for all I/O on the TS-4100 and/or TS-4400

CN1 Odd Pins

CN2 Odd Pins

High-speed differential pairs (USB and Ethernet) and SD card are not routed to these headers

CN1 Even Pins

CN2 Even Pins
Two 100-pin Module Connectors

- "5V" pins supply all power to the module. Apply 4.5V to 5.5V to these pins. Current drain is < 400 mA (less than 4 Watts).
- Do not drive active high (use open drain).
- OFF_BD_RESET# is an output from the SBC used to reboot the CPU.
- EXT_RESET# is an input to the SBC.
- JTAG_Ethernet FPGA (less than 4 Watts)

SBC Current

- 100 mA at 500 mA load
- 500 mV @ 500 mA

All signals driving DIO on CN1 & CN2 must be powered by the 3.3V on CN2, or remain at 0V until the CN2 3.3V rail is > 3.0V.

Two 100-pin Module Connectors

- TS-4100 FPGA JTAG
- SBC_5V
- OFF_BD_RESET# has weak pullup on the SBC module.
- All signals driving DIO on CN1 & CN2 must be powered by the 3.3V on CN2, or remain at 0V until the CN2 3.3V rail is > 3.0V.