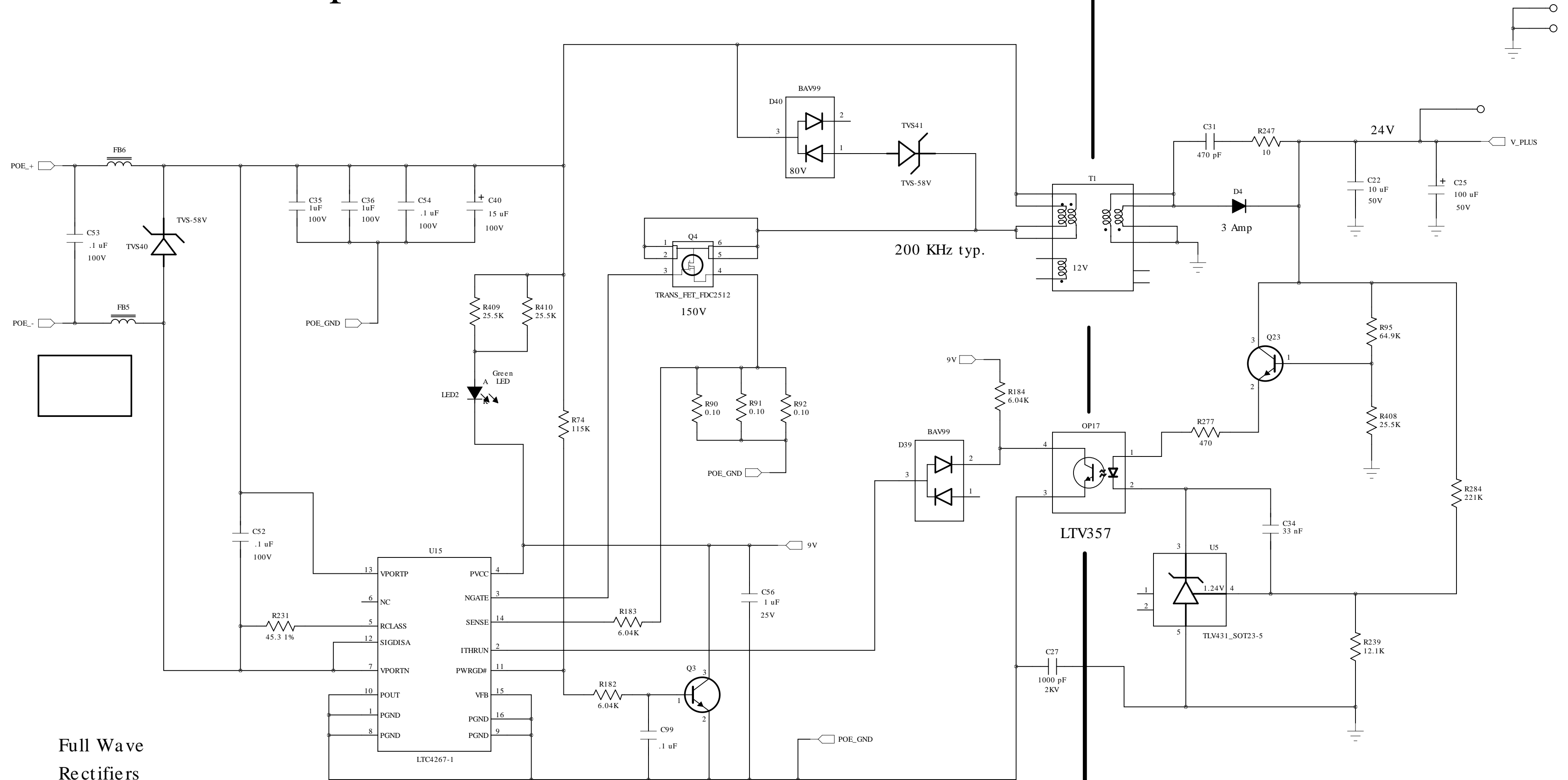


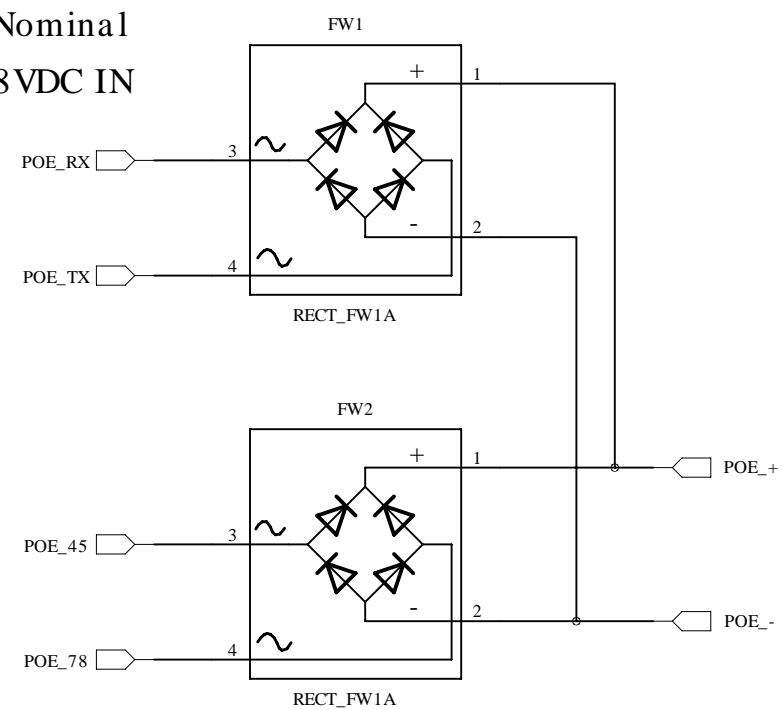
POE Side 48V DC Input

Reg. 24V Out



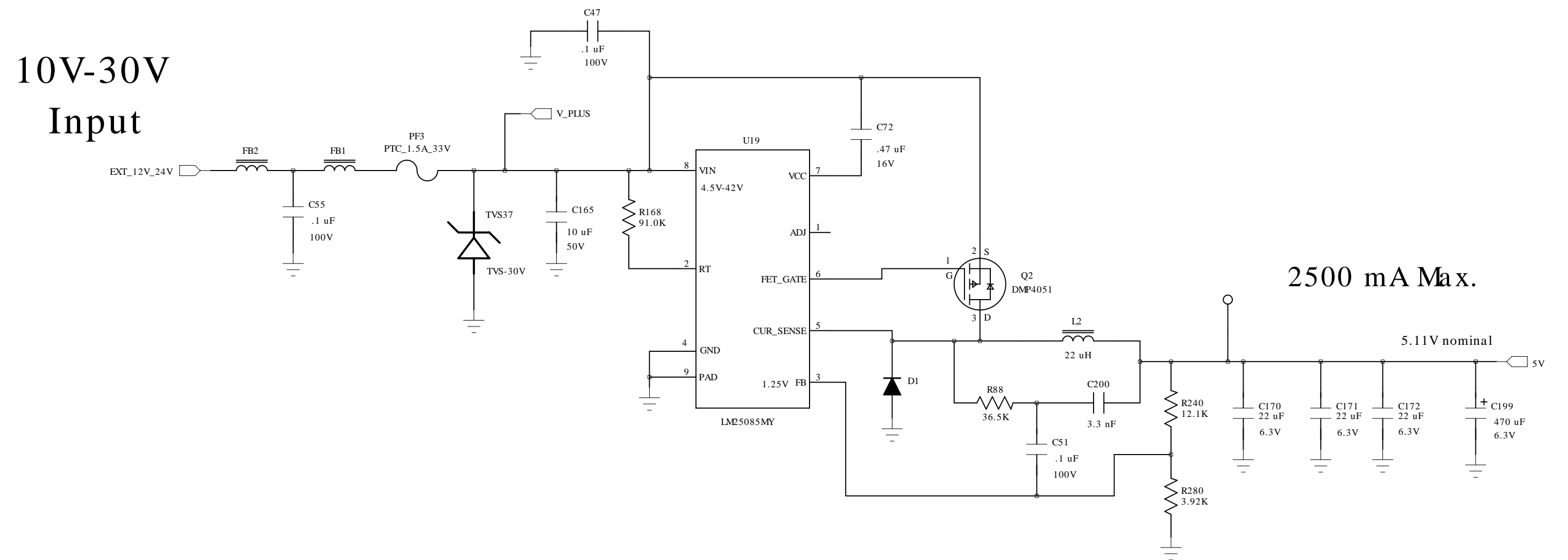
Full Wave Rectifiers

Nominal
48VDC IN

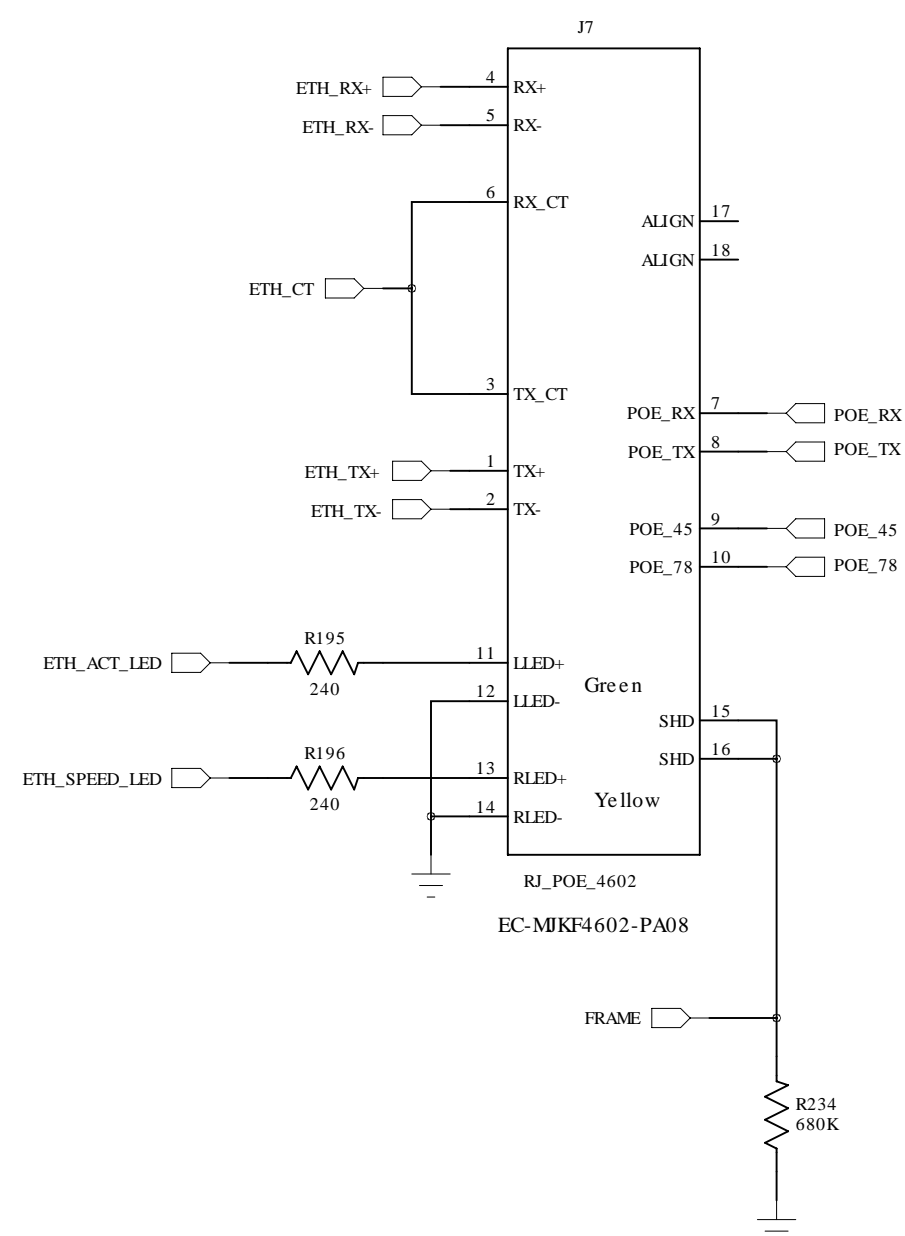


Technologic Systems	Aug. 10, 2012
Title: TS-8820 POE	
Rev: A	Designer
Sheet 1 of 18	

Non-isolated 5V Power Supply



10/100 Ethernet Transformer

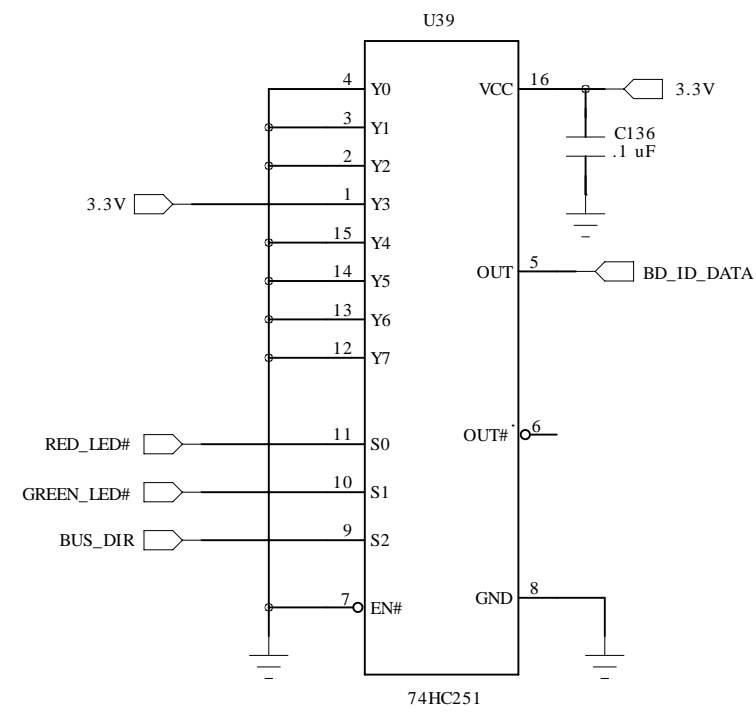


Technologic Systems	Aug. 10, 2012
Title: TS-8820 Ethernet and 5V Power	
Rev: A	Designer
Sheet 2 of 18	

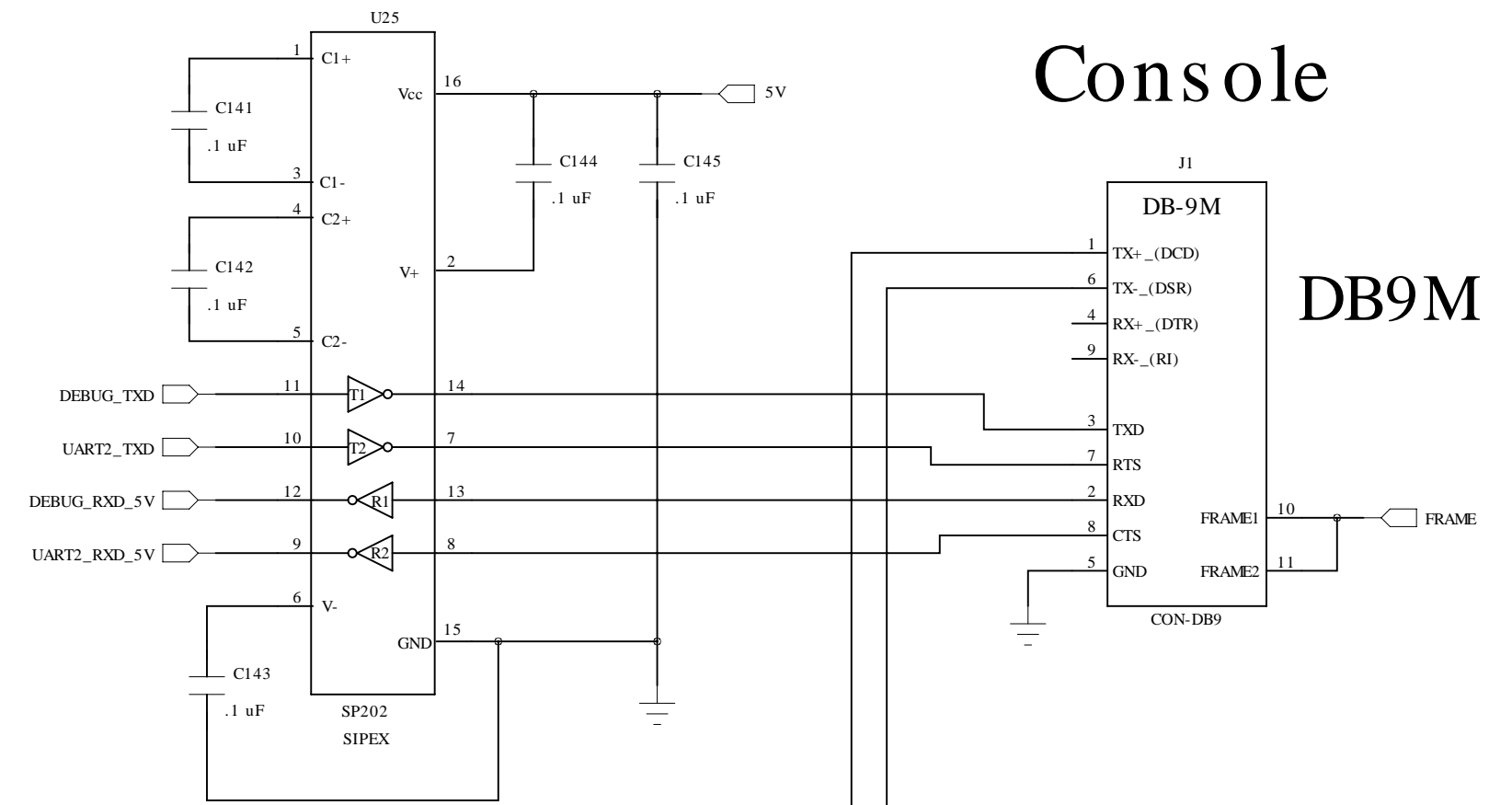
Battery-Backed SRAM

Technologic Systems	Aug. 10, 2012	
Title: TS-8820 Battery and NVRAM		
Rev: A	Designer	Sheet 3 of 18

Board ID = 8



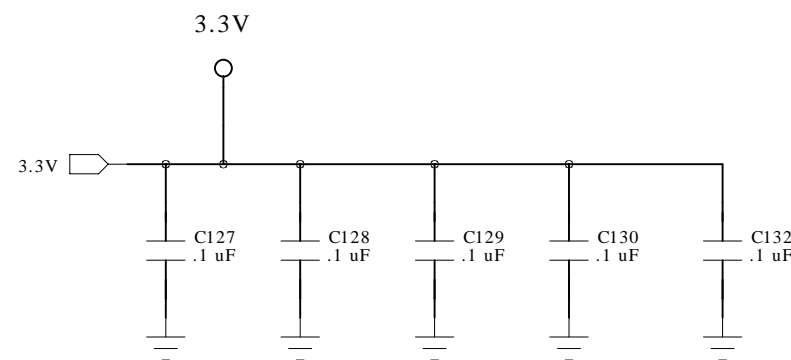
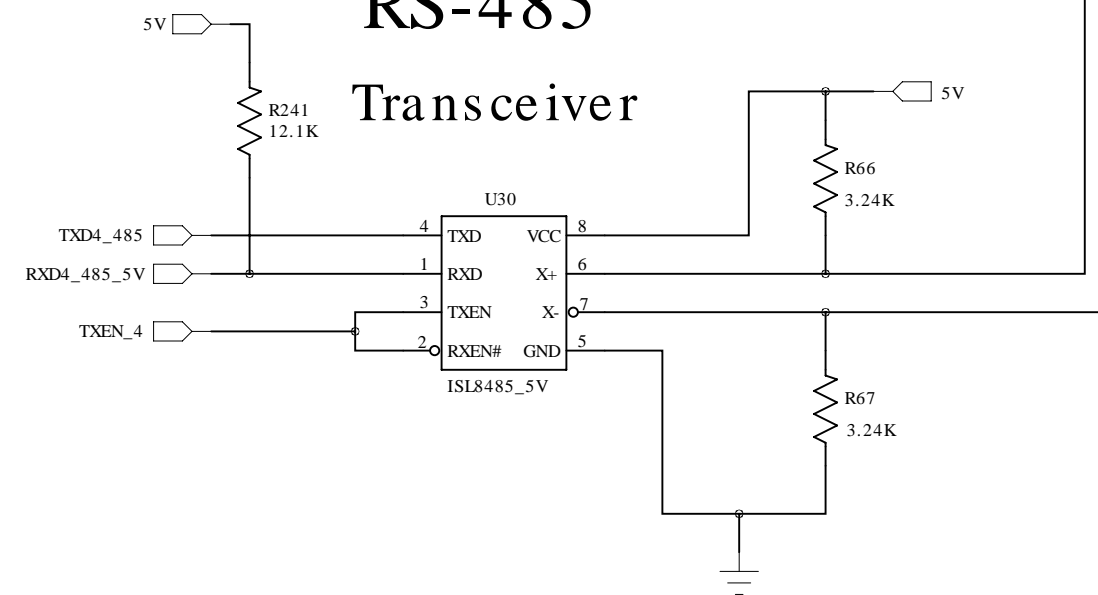
RS-232 Transceiver



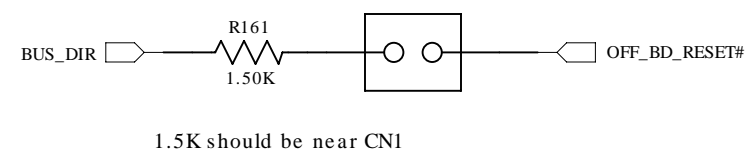
Console

DB9M

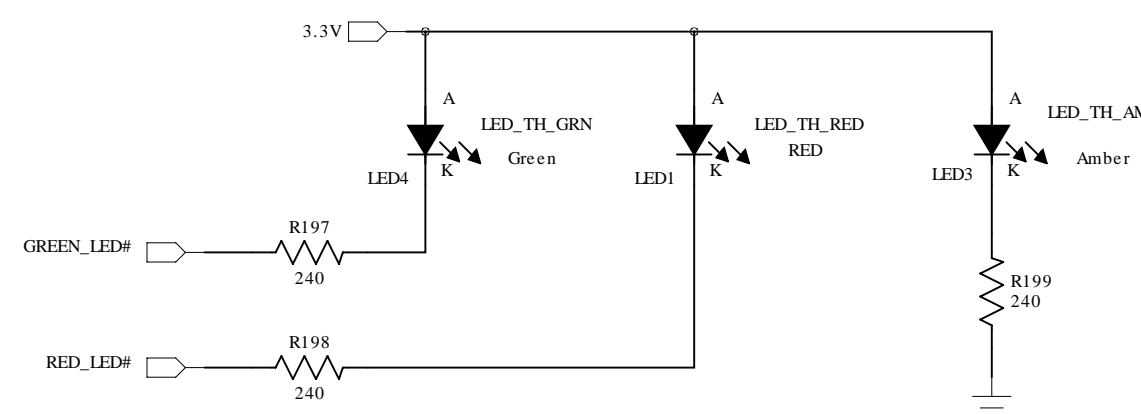
RS-485 Transceiver



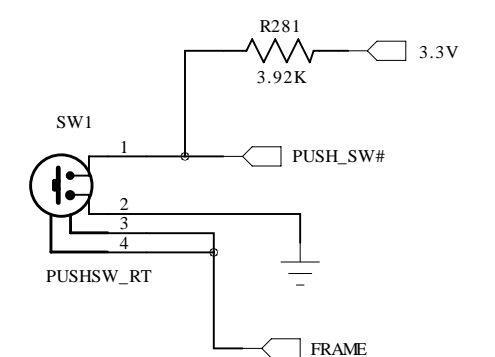
Force Boot to SD card



LEDs



Right Angle Push Switch

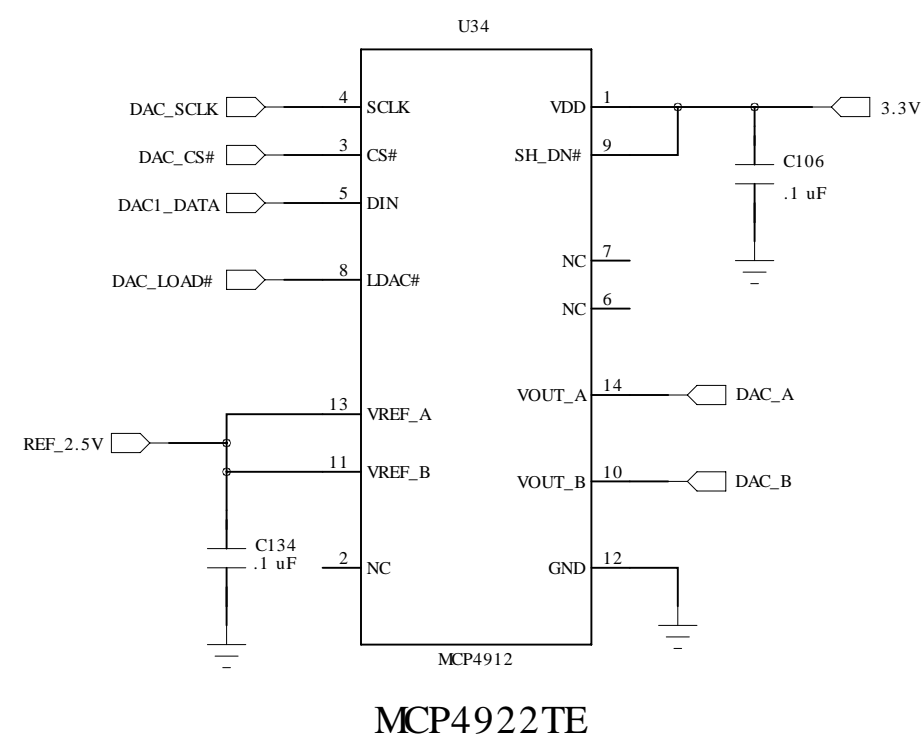


Technologic Systems	Aug. 10, 2012
Title: TS-8820 Console, RS-485, Board ID	
Rev: A	Designer RLM
Sheet 4 of 18	

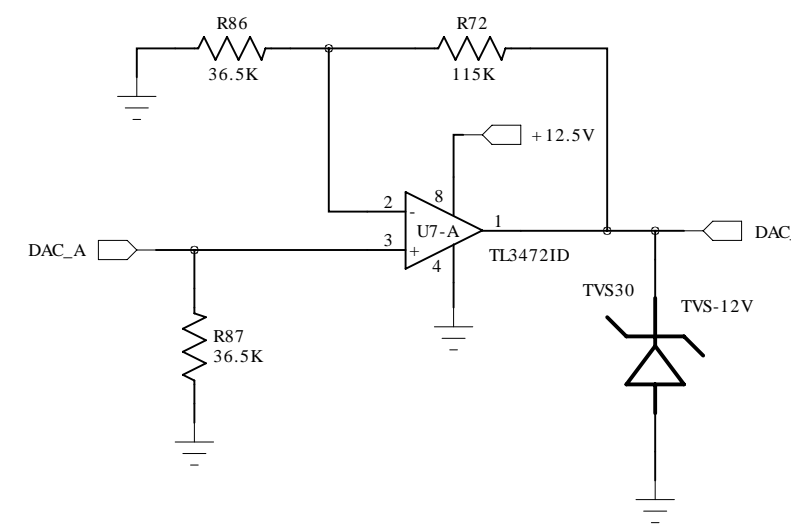
Four 12-bit DAC channels (0-10V Range)

12-bit DAC

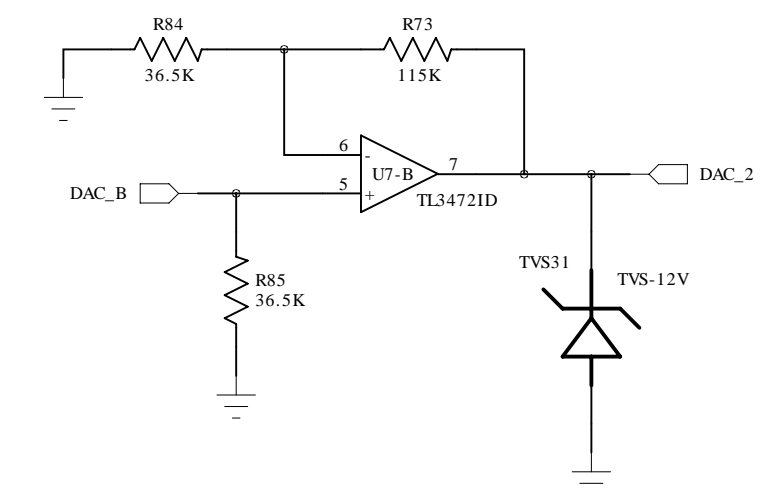
0 to 2.5V levels



Gain = 4.15

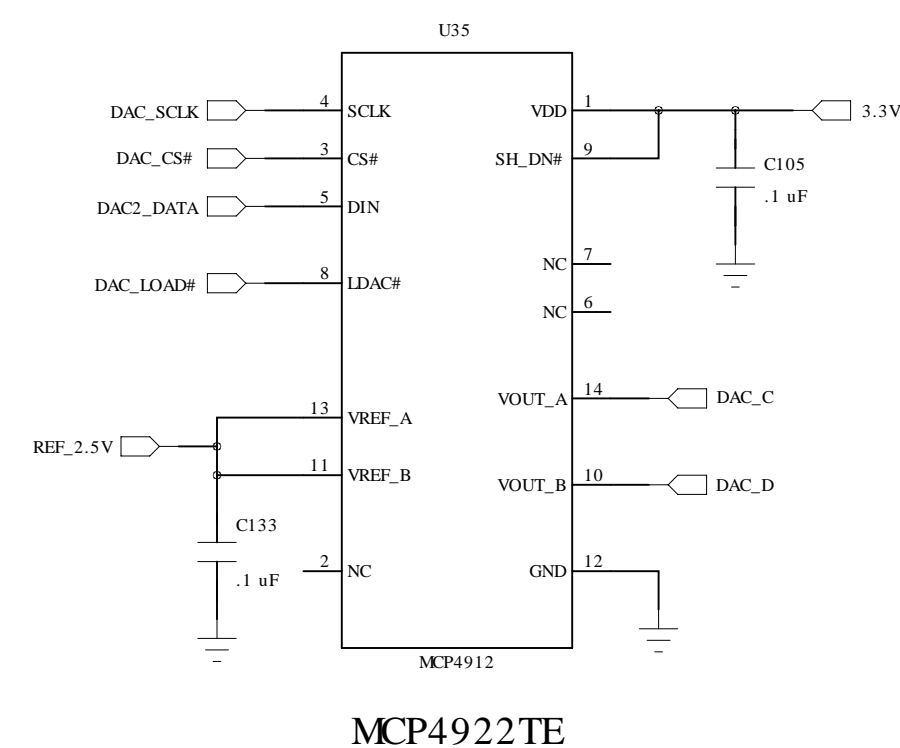


Gain = 4.15

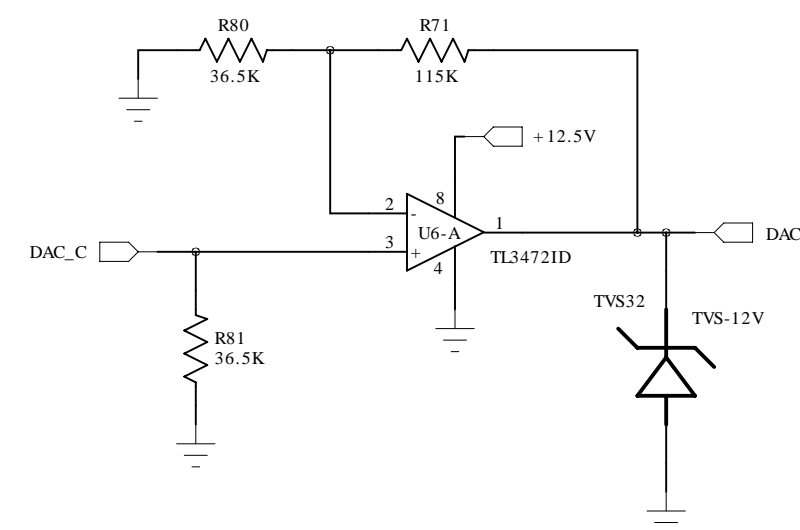


12-bit DAC

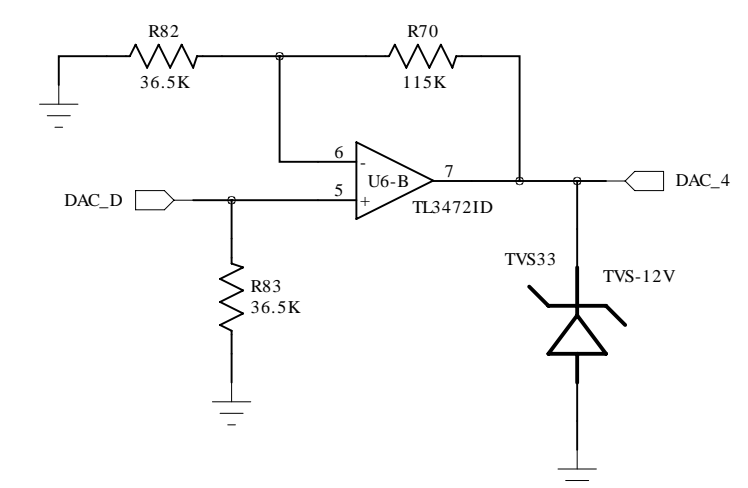
0 to 2.5V levels



Gain = 4.15



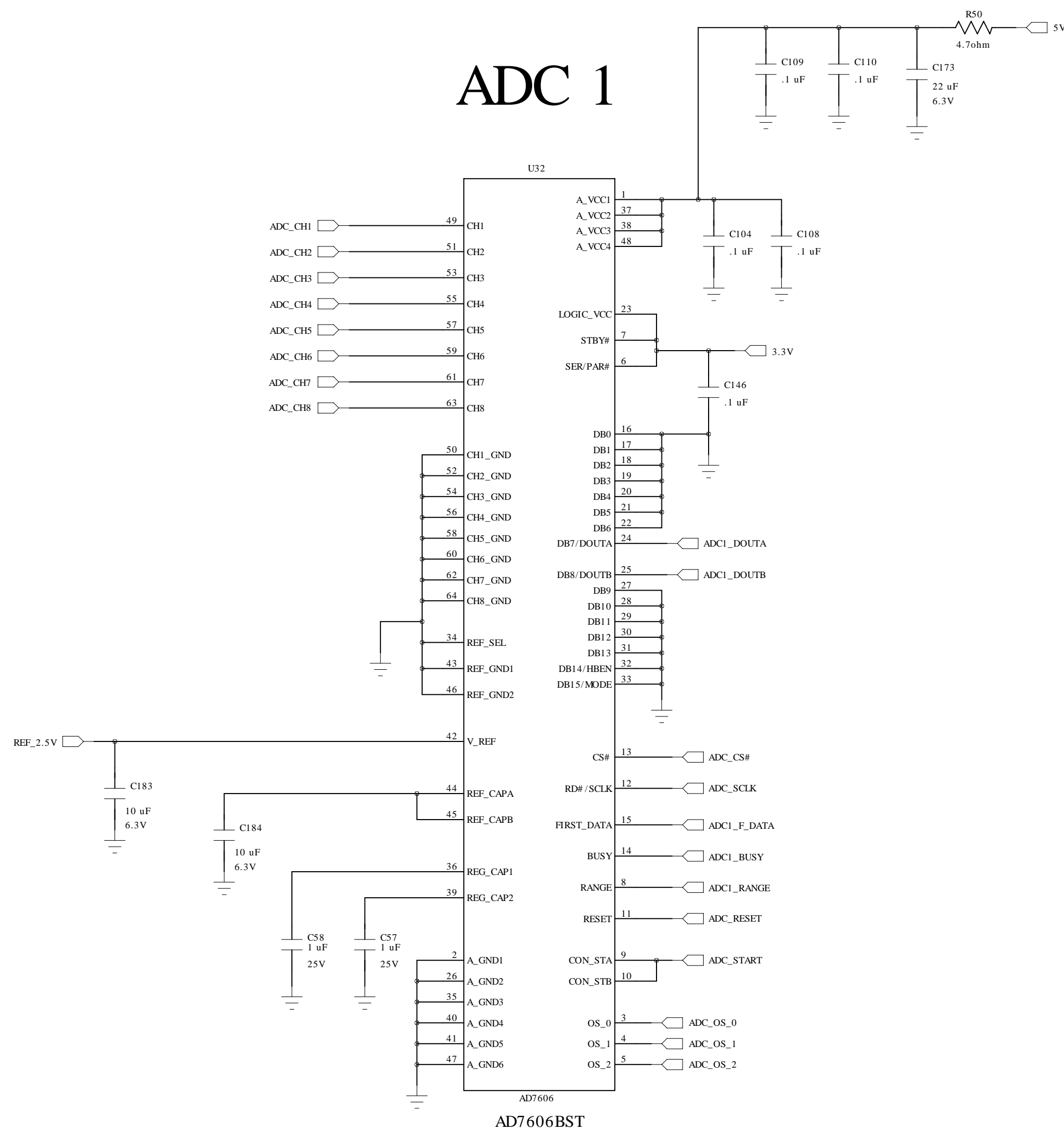
Gain = 4.15



Technologic Systems	Aug. 10, 2012
Title: TS-8820 DAC and Op Amps	
Rev: A	Designer
Sheet 5 of 18	

8 A/D channels

Simultaneous Sampling

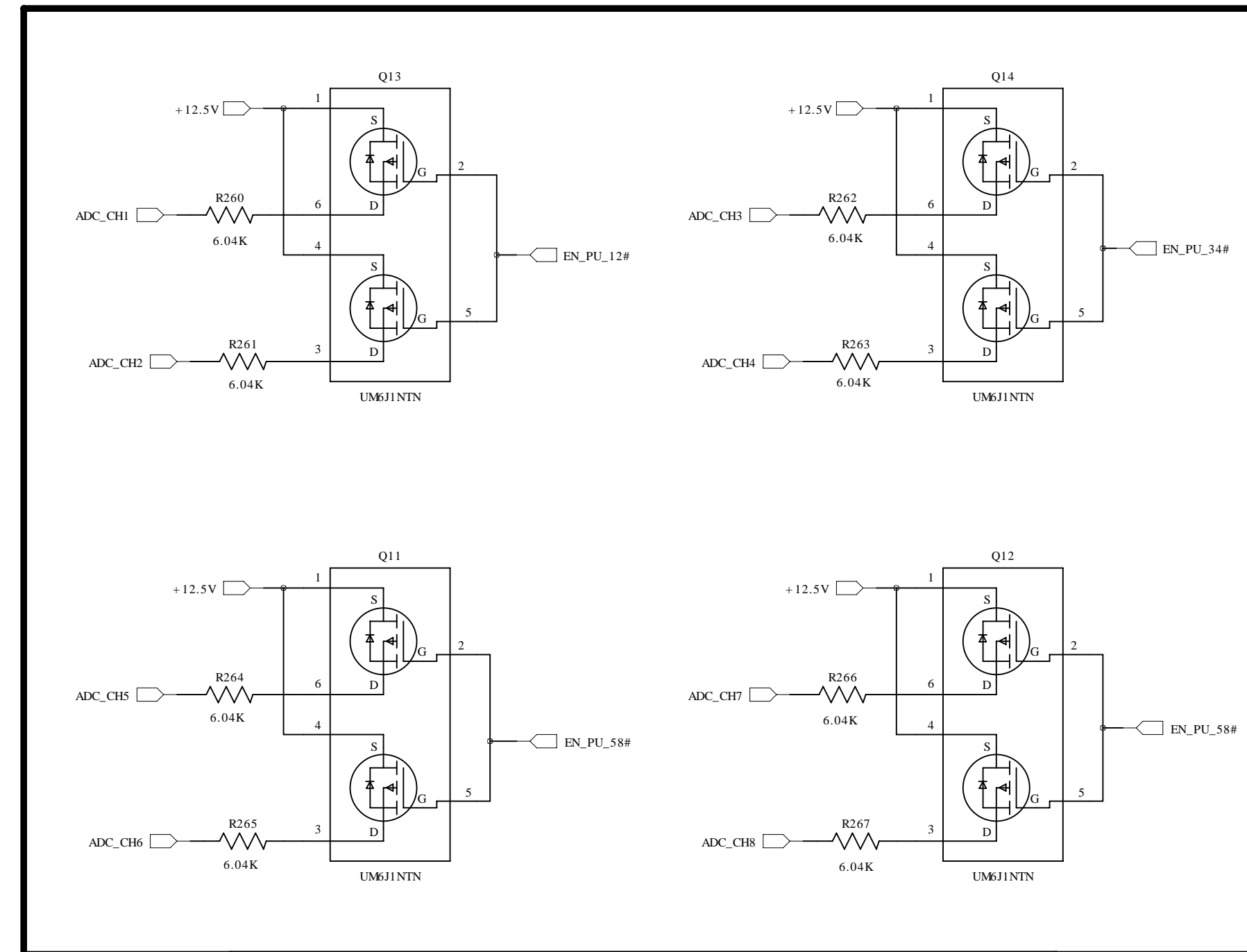


Simultaneous sampling of
 all 8 A/D inputs

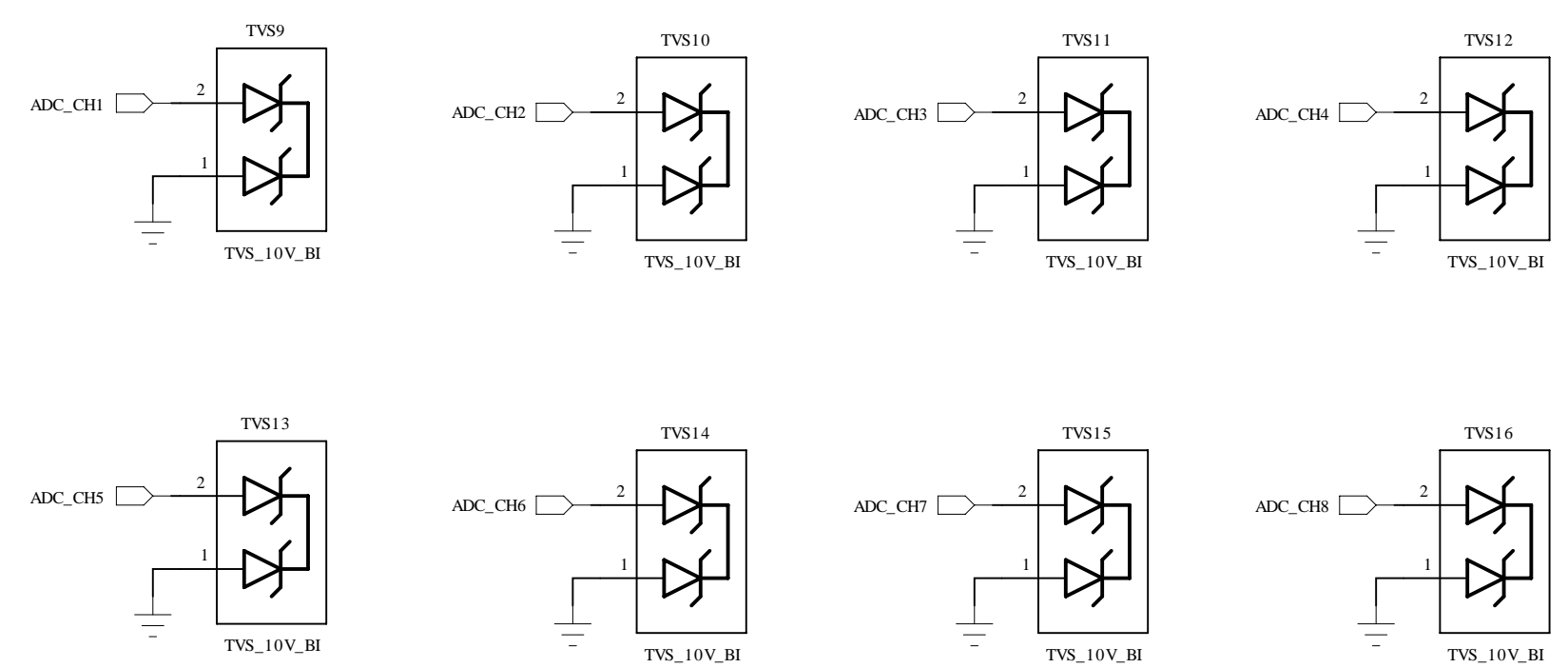
 Software selectable ranges
 +/-5V or +/-10V

 200K samples per second

 >1 Megohm input impedance



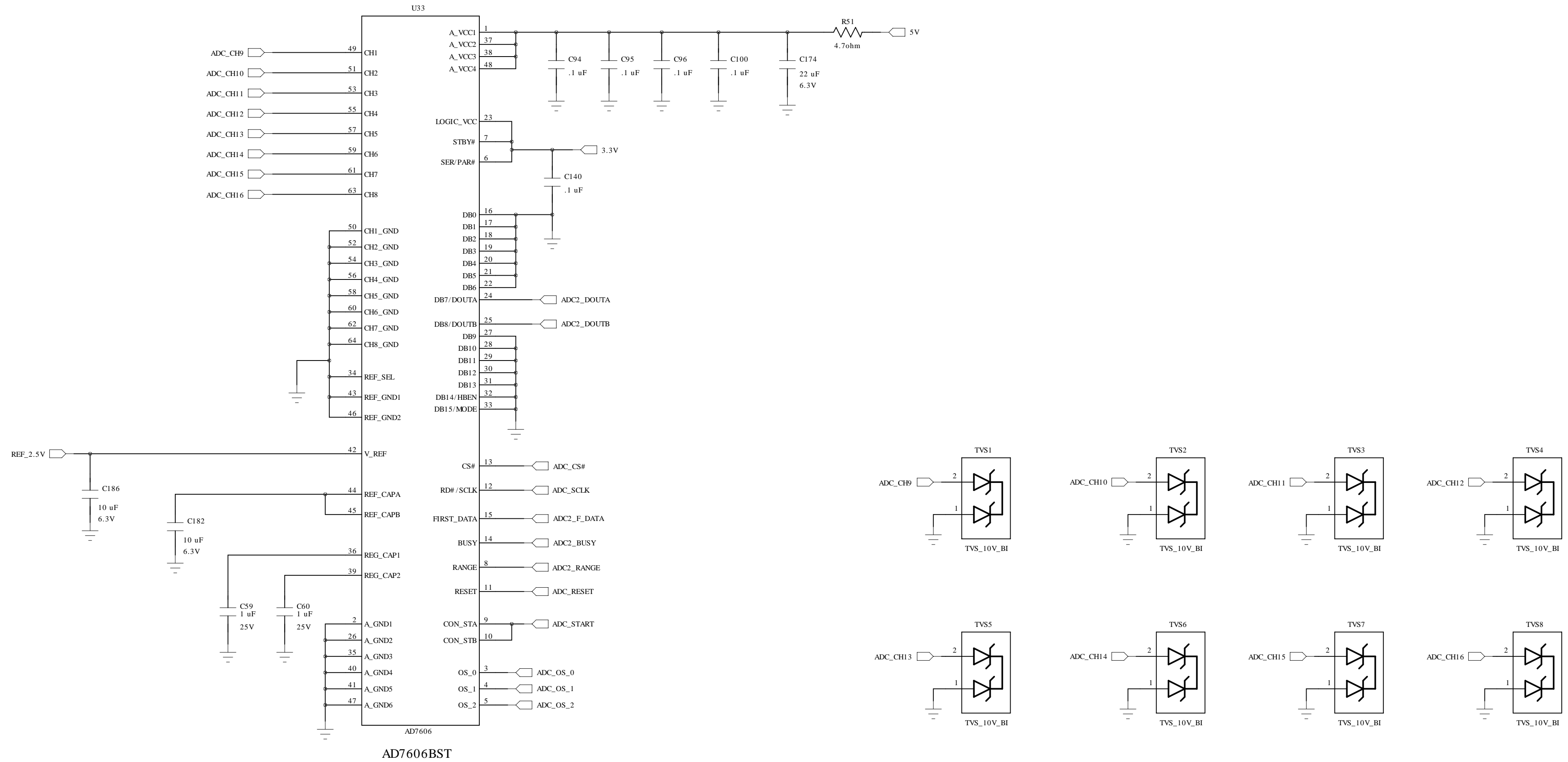
Allows up to 8 Thermistors



8 A/D channels

Simultaneous Sampling

ADC 2



Simultaneous sampling of all 8 A/D inputs

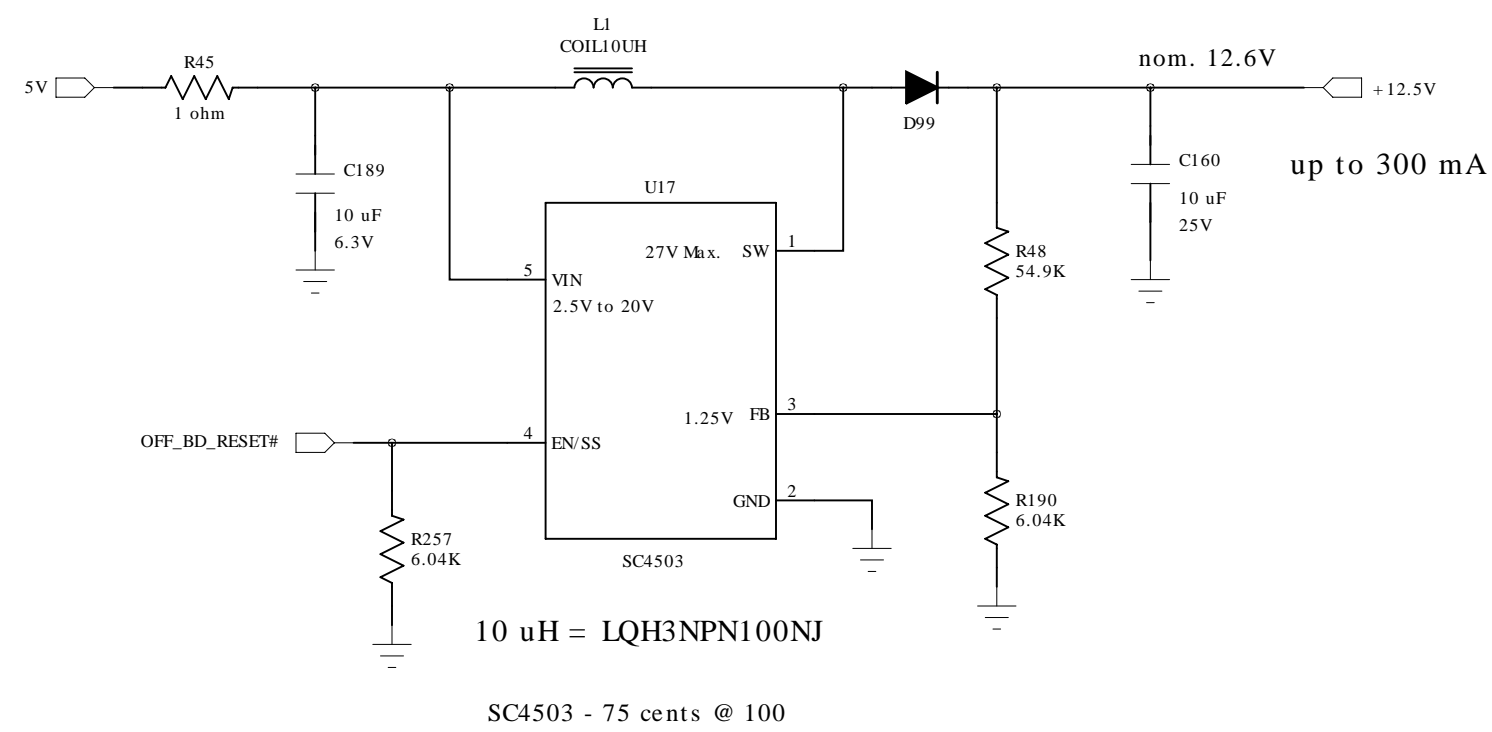
Software selectable ranges
+/-5V or +/-10V

200K samples per second

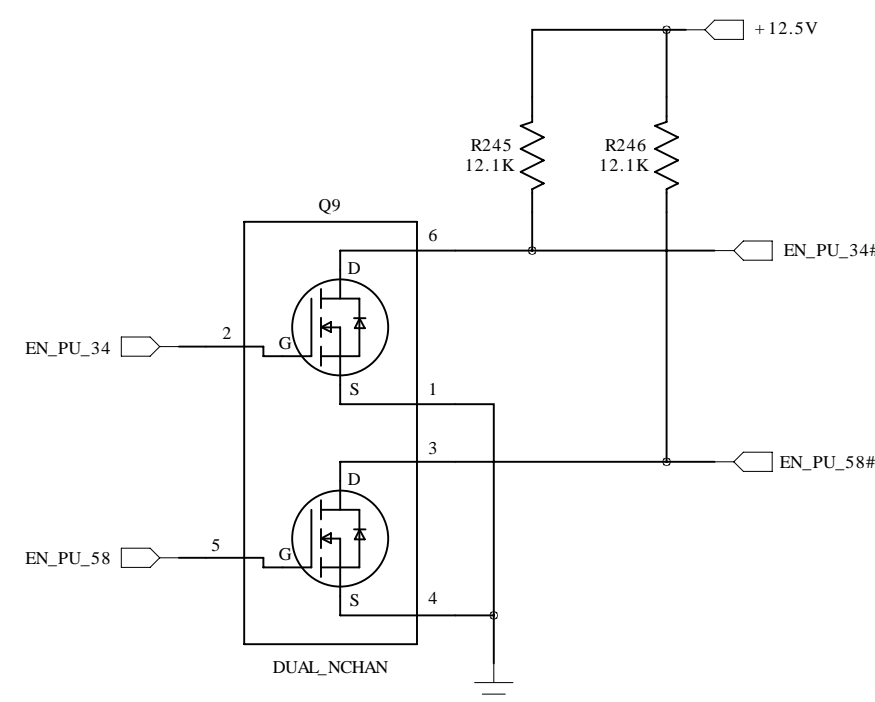
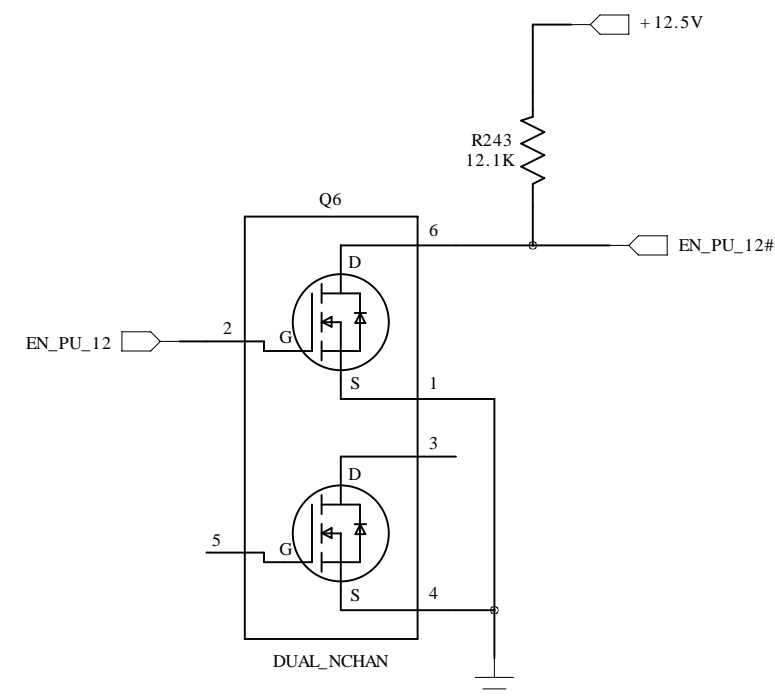
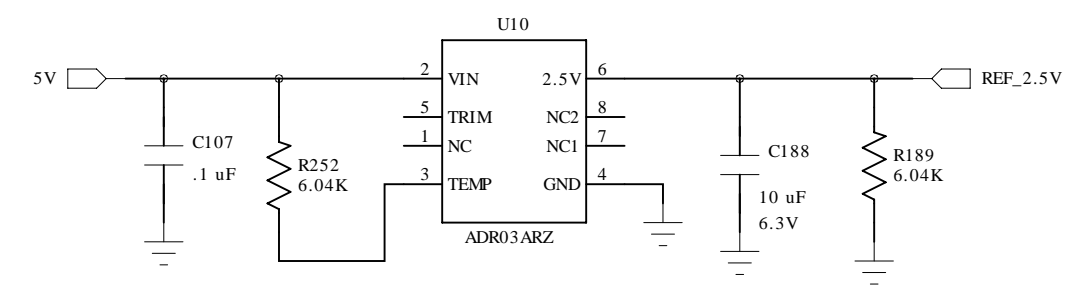
>1 Megohm input impedance

Technologic Systems	Aug. 10, 2012
Title: TS-8820 Analog-to-Digital	
Rev: A	Designer
Sheet 6 of 18	

+ 12.5V Boost Regulator



Precision 2.5V Reference

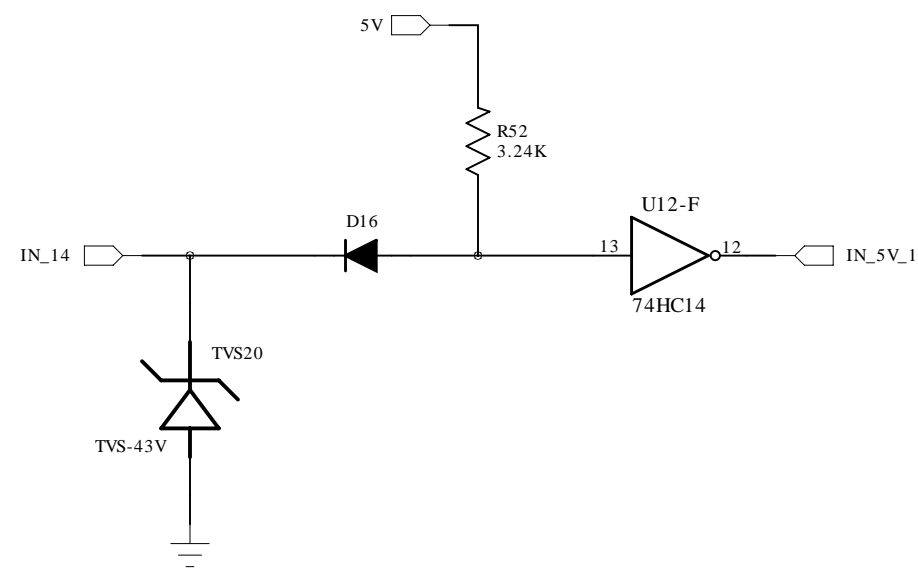
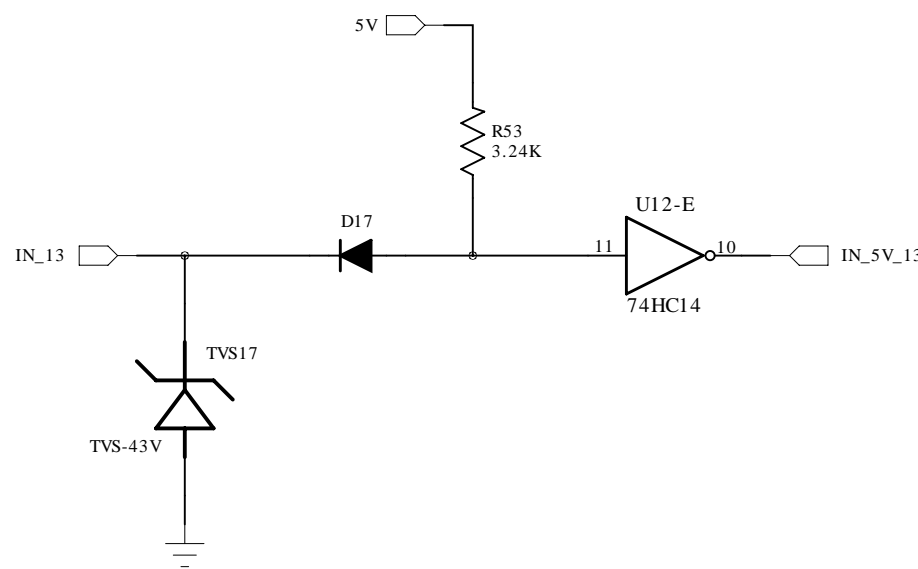
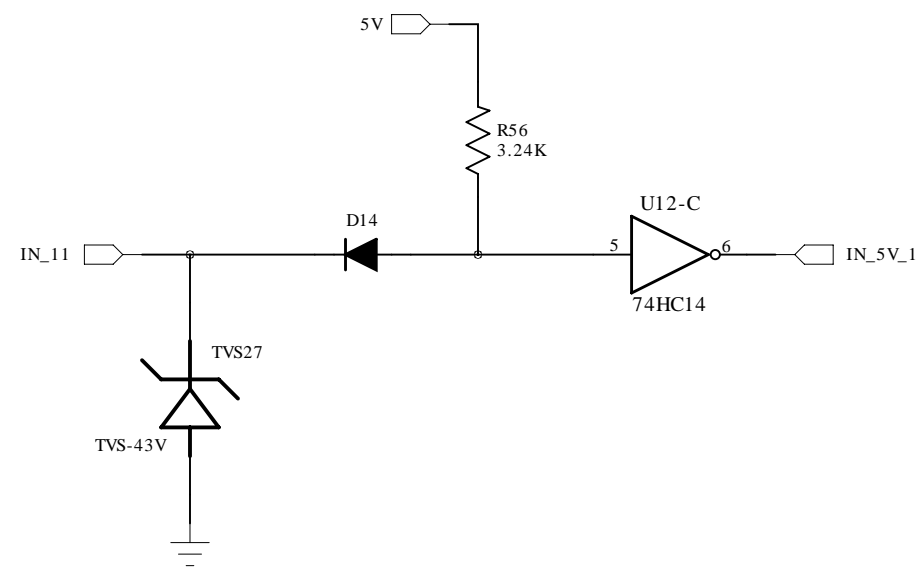
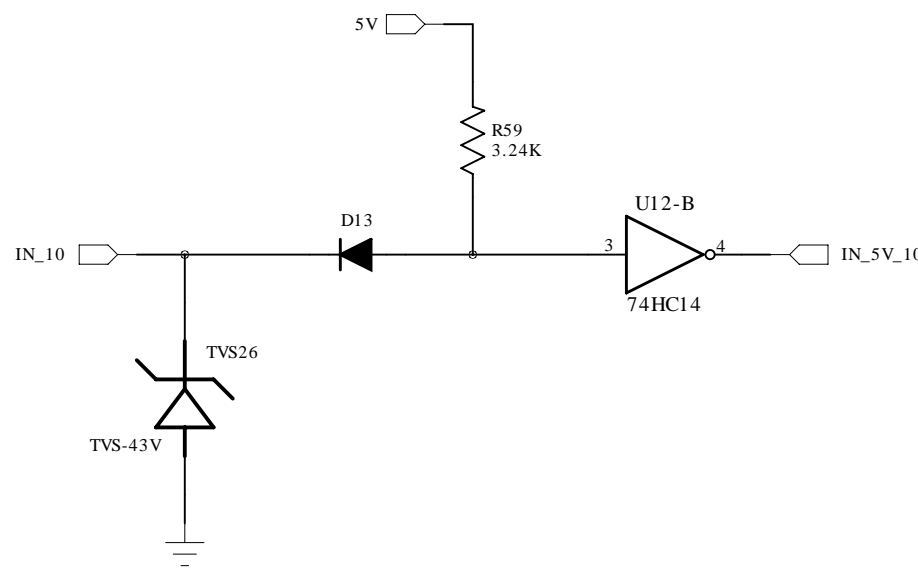
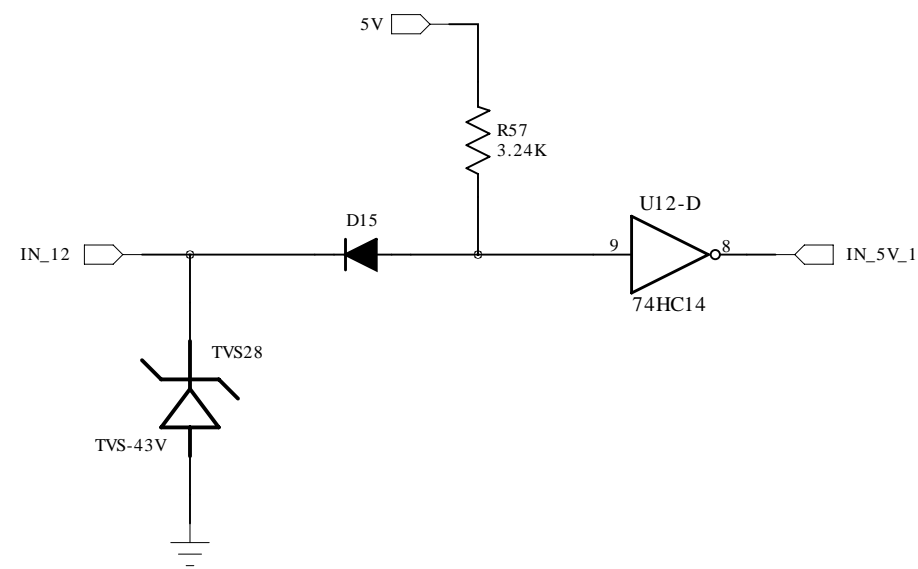
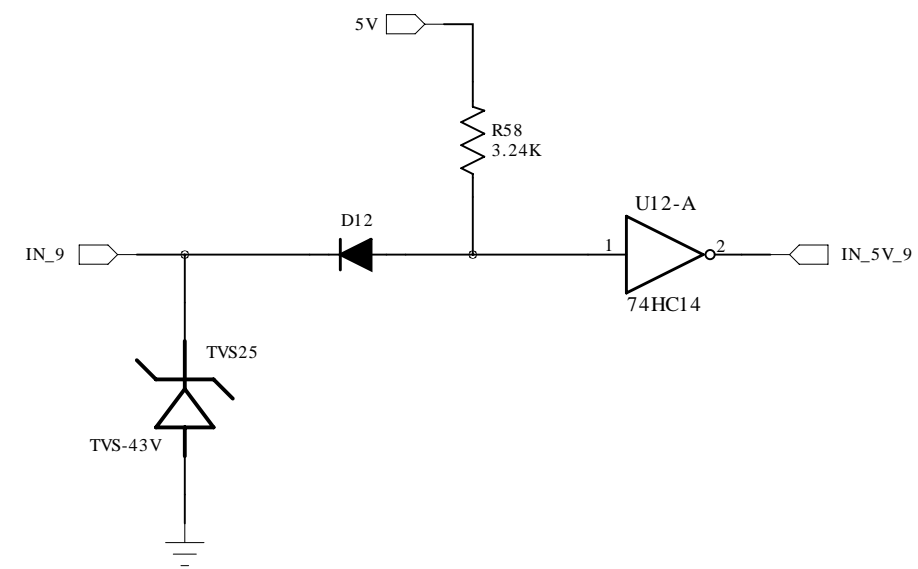


Technologic Systems	Aug. 10, 2012	
Title: TS-8820 DAC, 2.5V Ref.		
Rev: A	Designer	Sheet 8 of 18

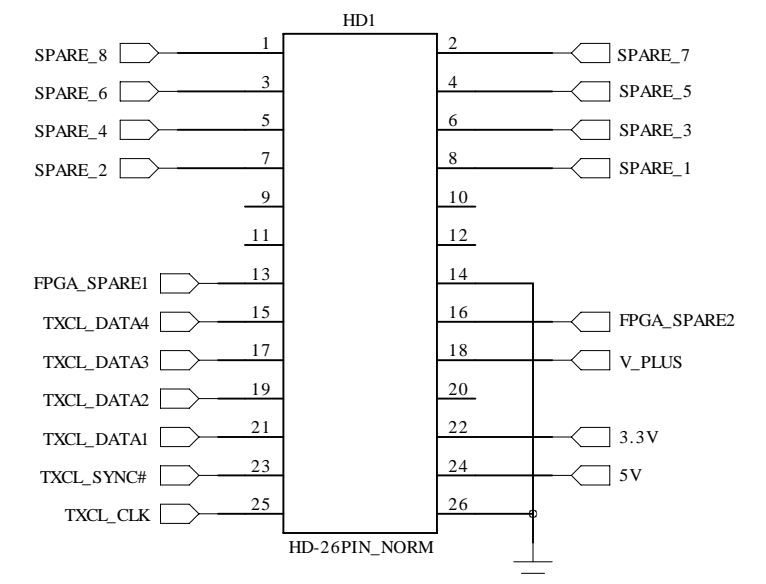
Non-Isolated Inputs

with Pull-up Resistors

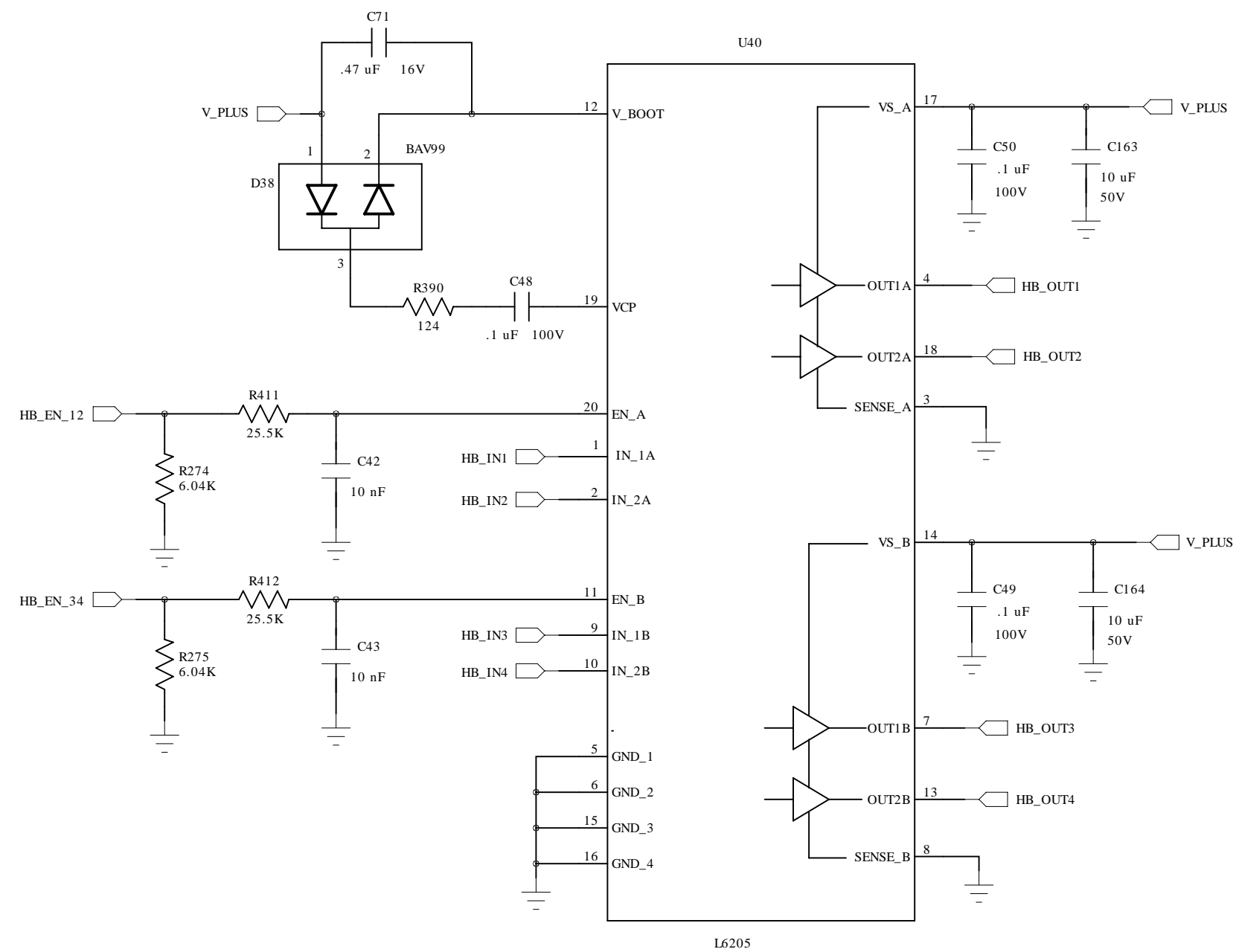
+ 40V tolerant



TX Current Loop Daughter Board Header

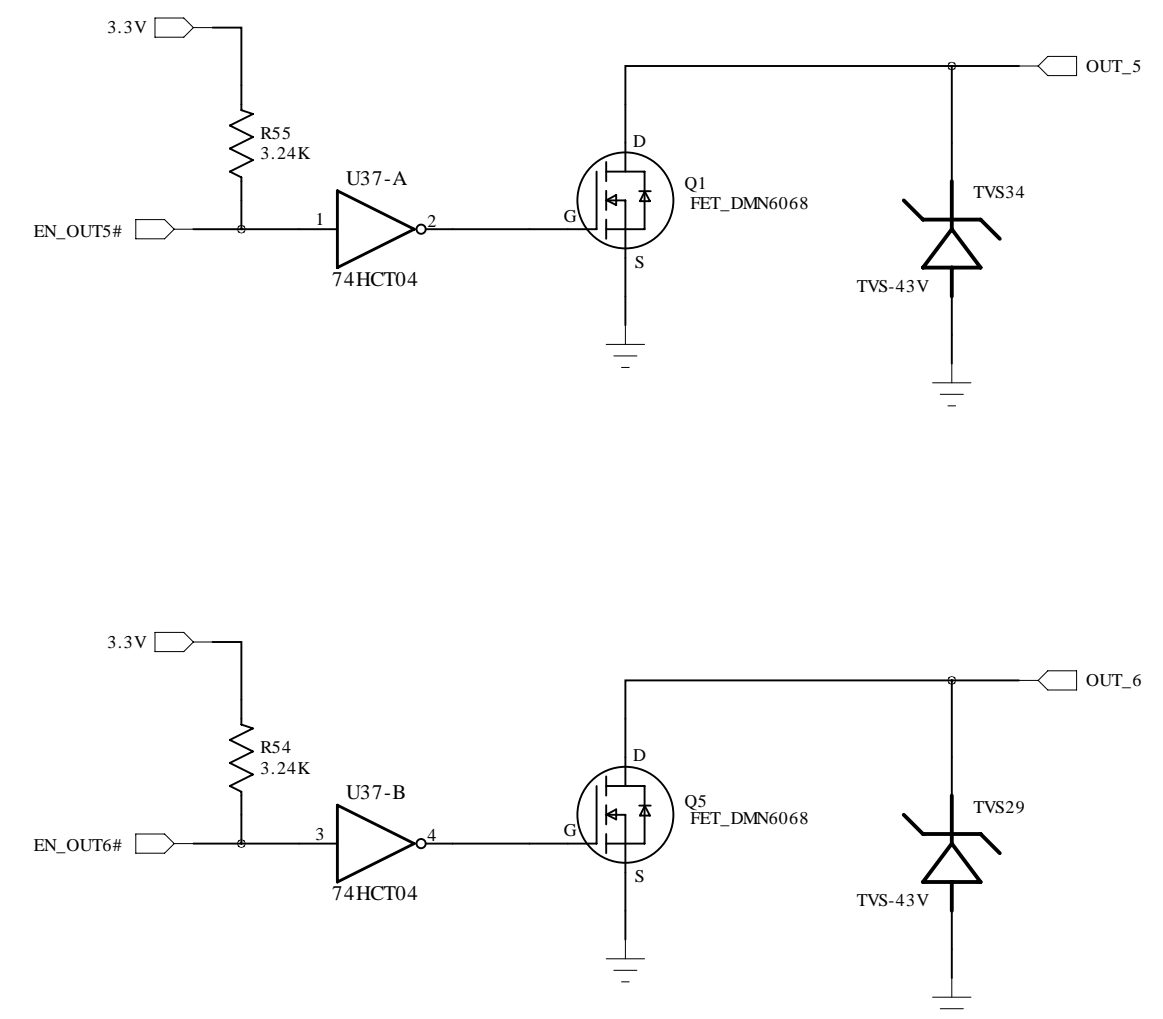


Dual H-bridge

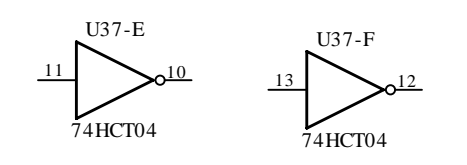
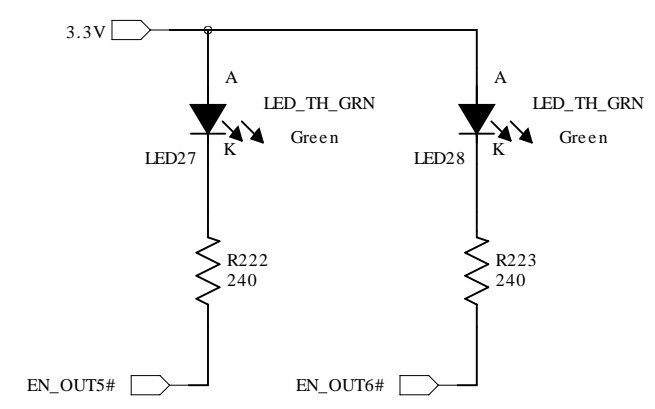


Non-Isolated Outputs

Sinks 1000 mA



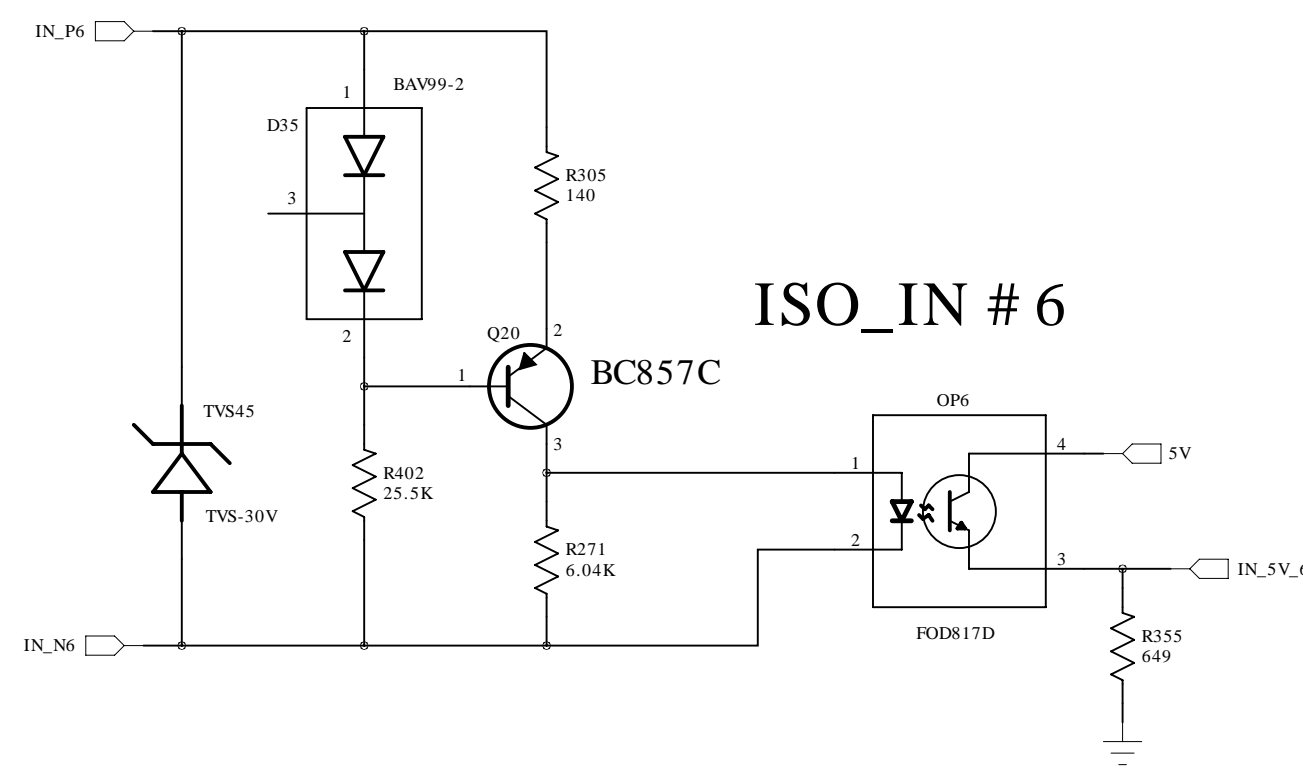
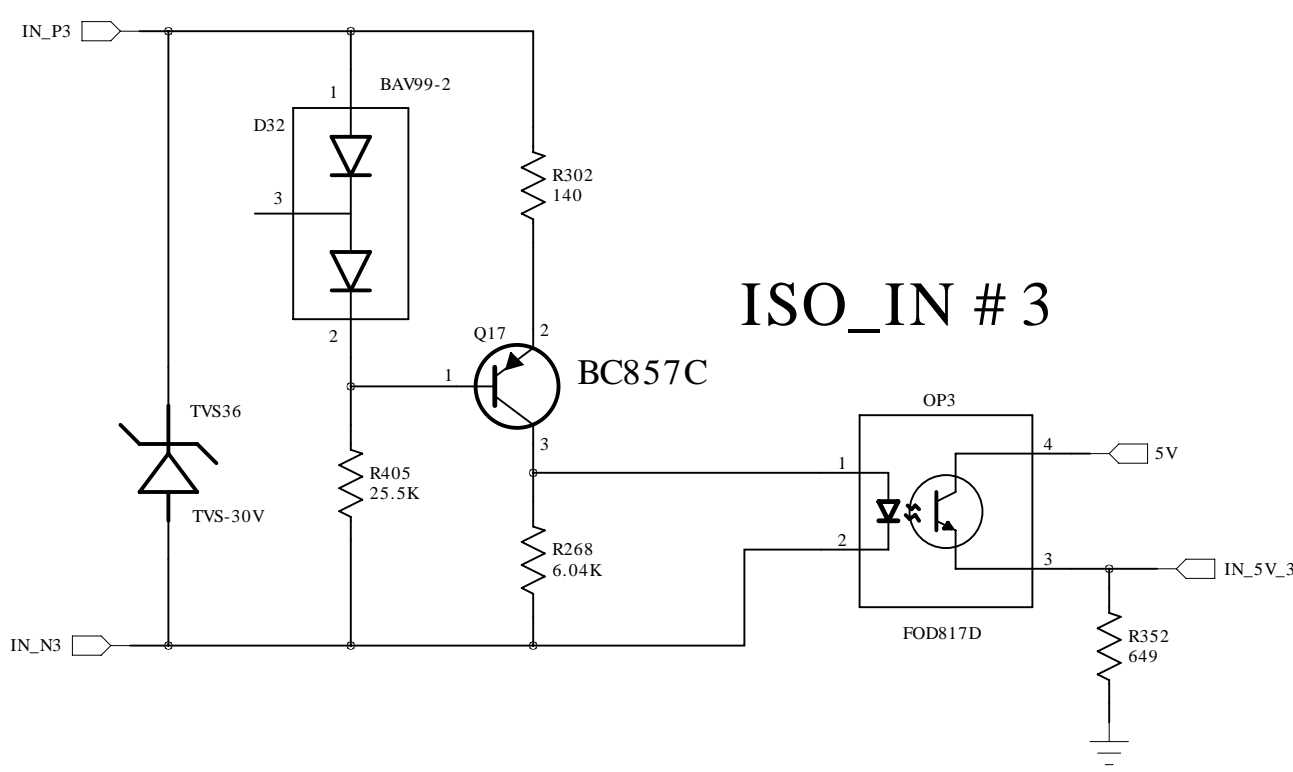
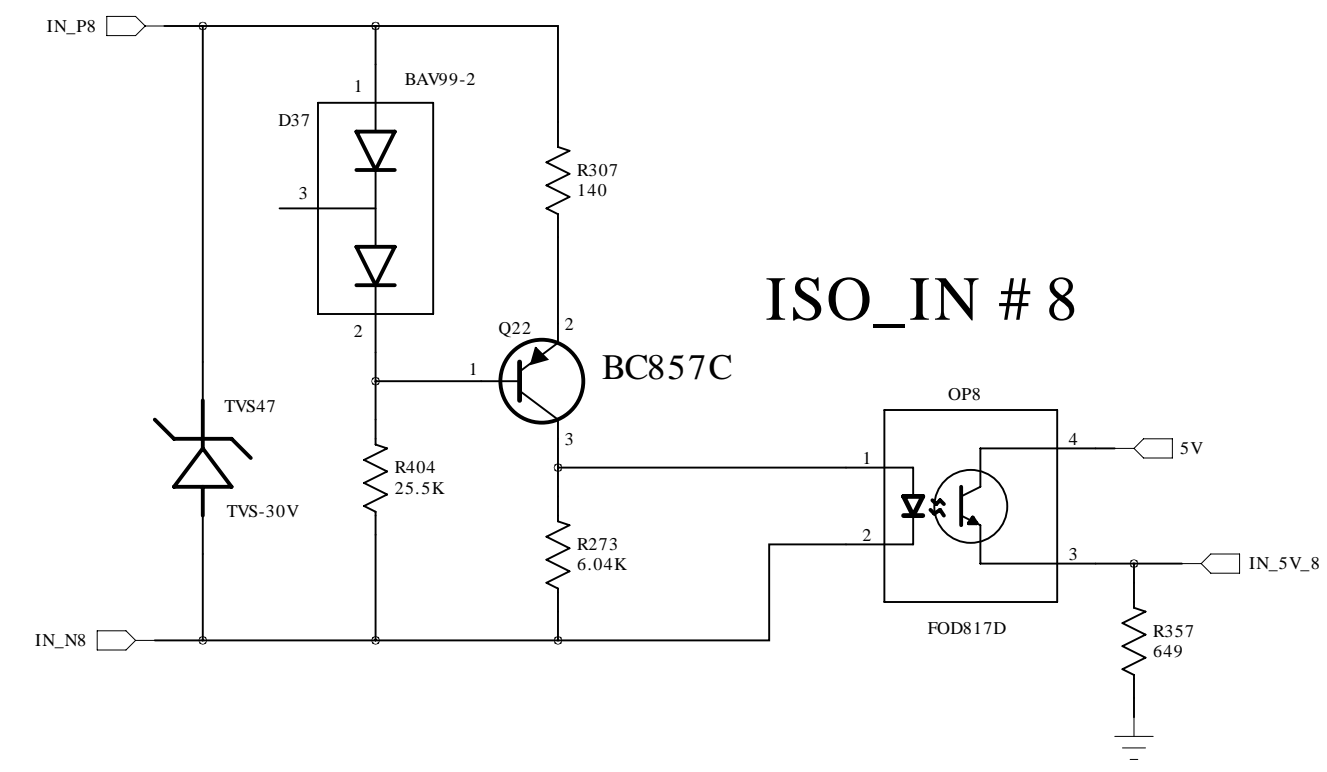
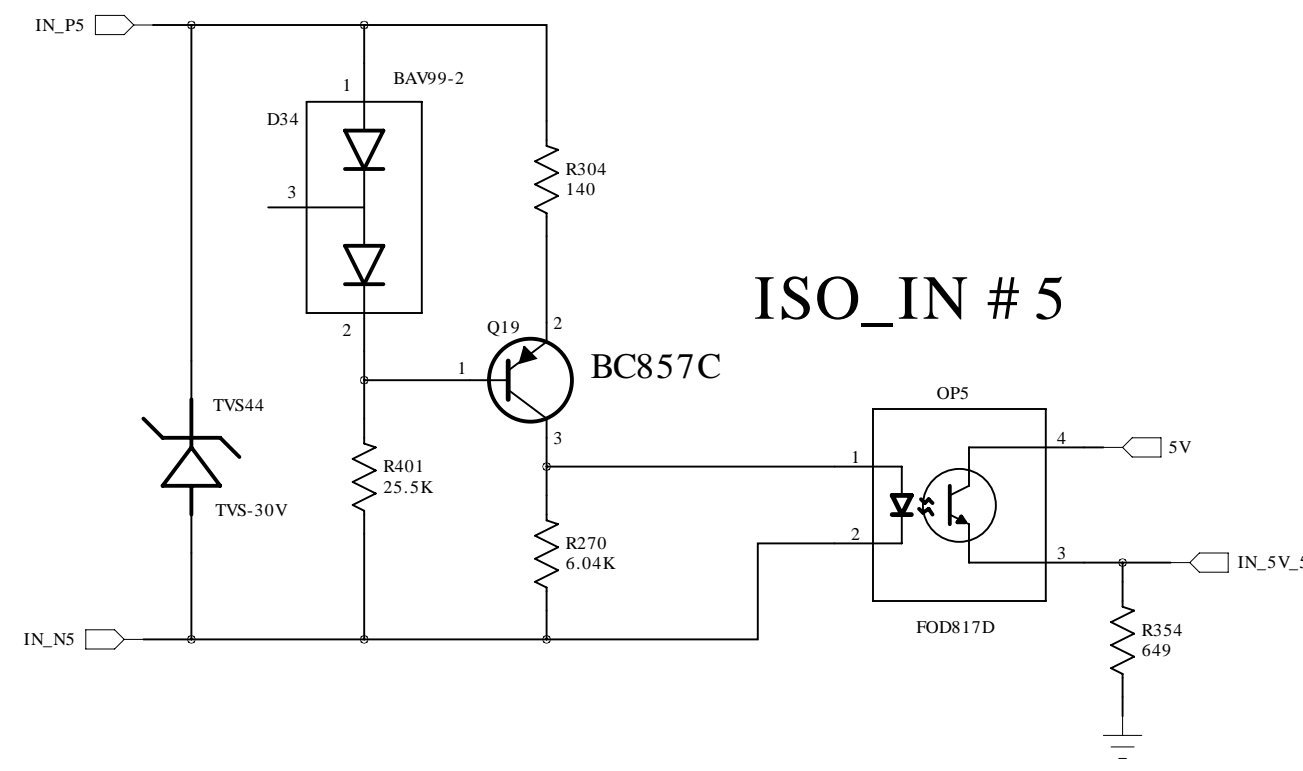
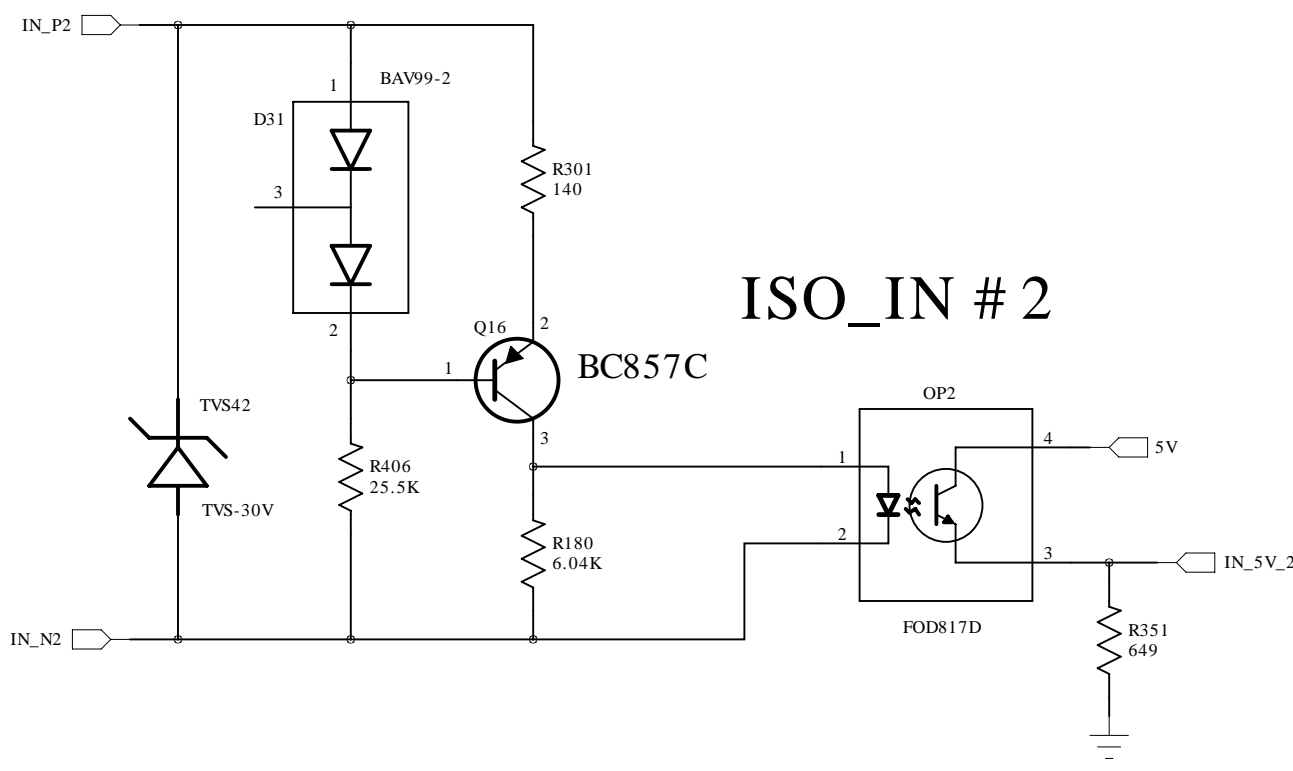
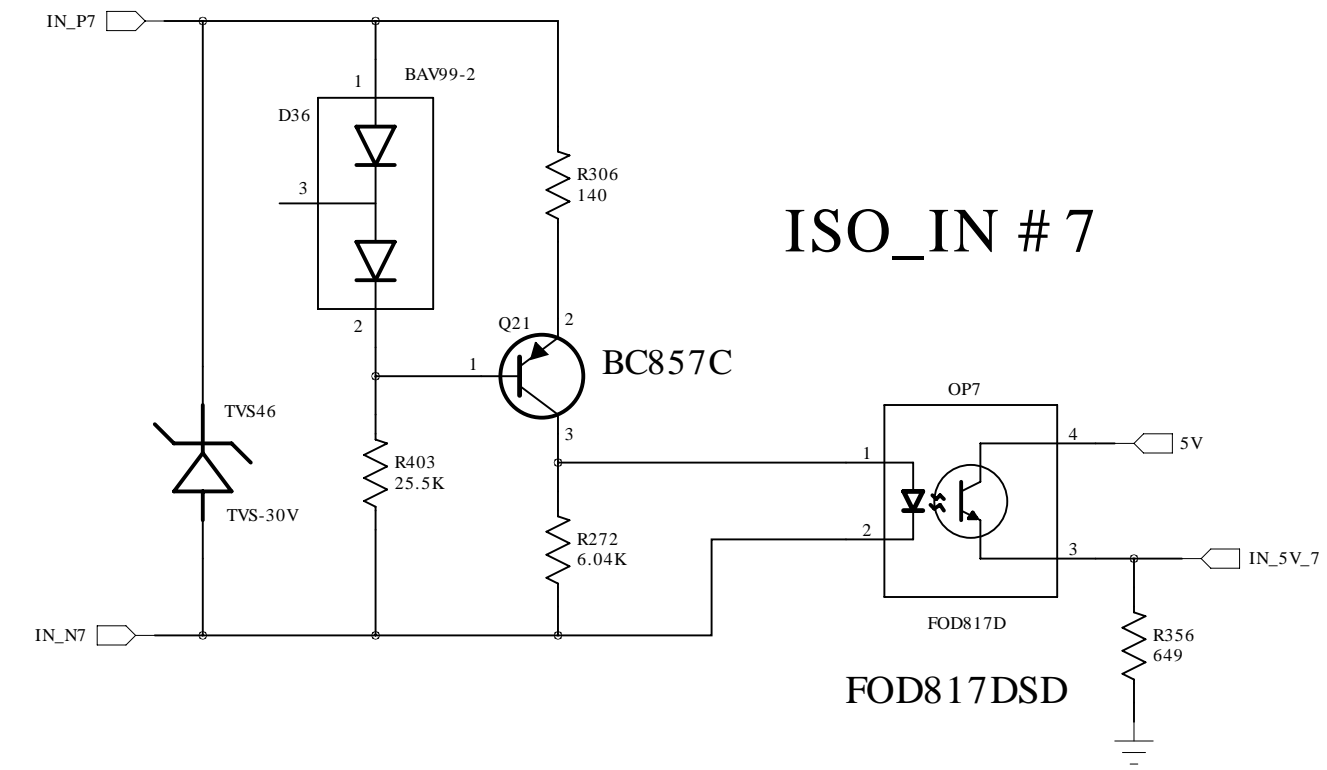
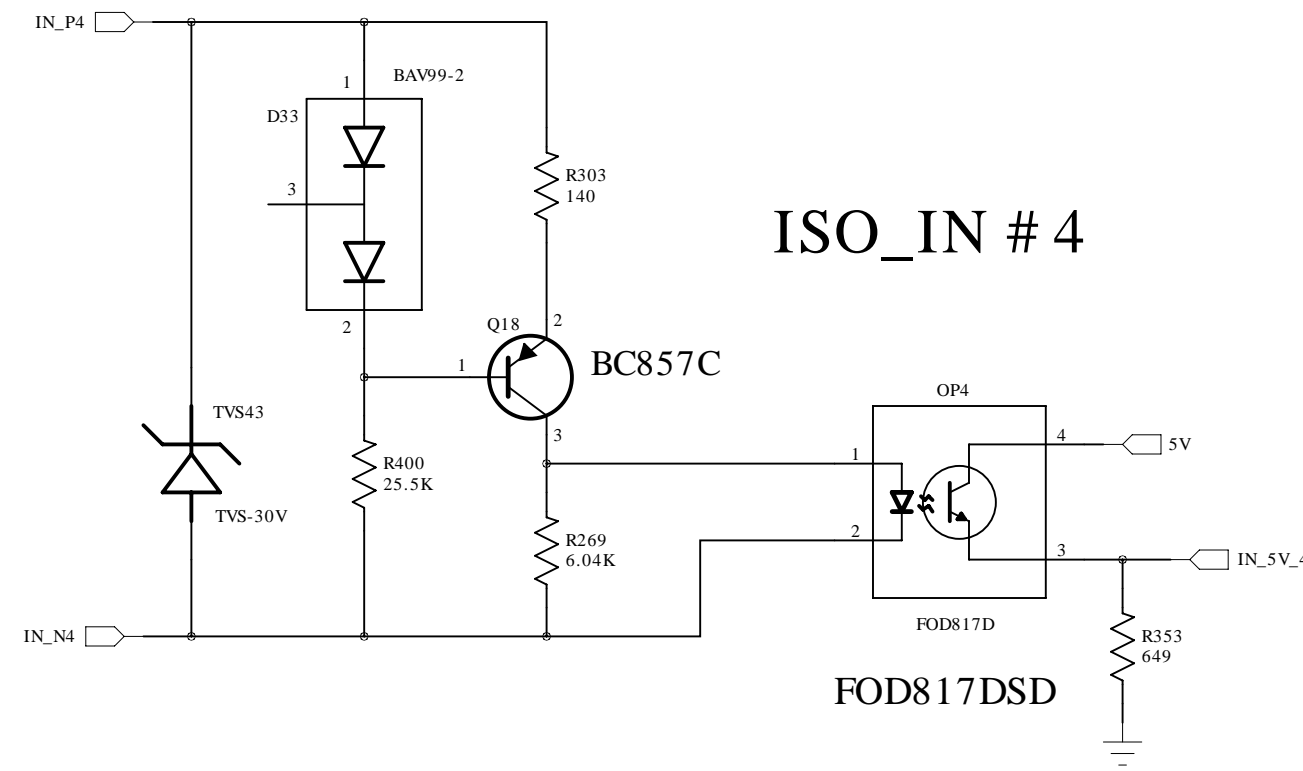
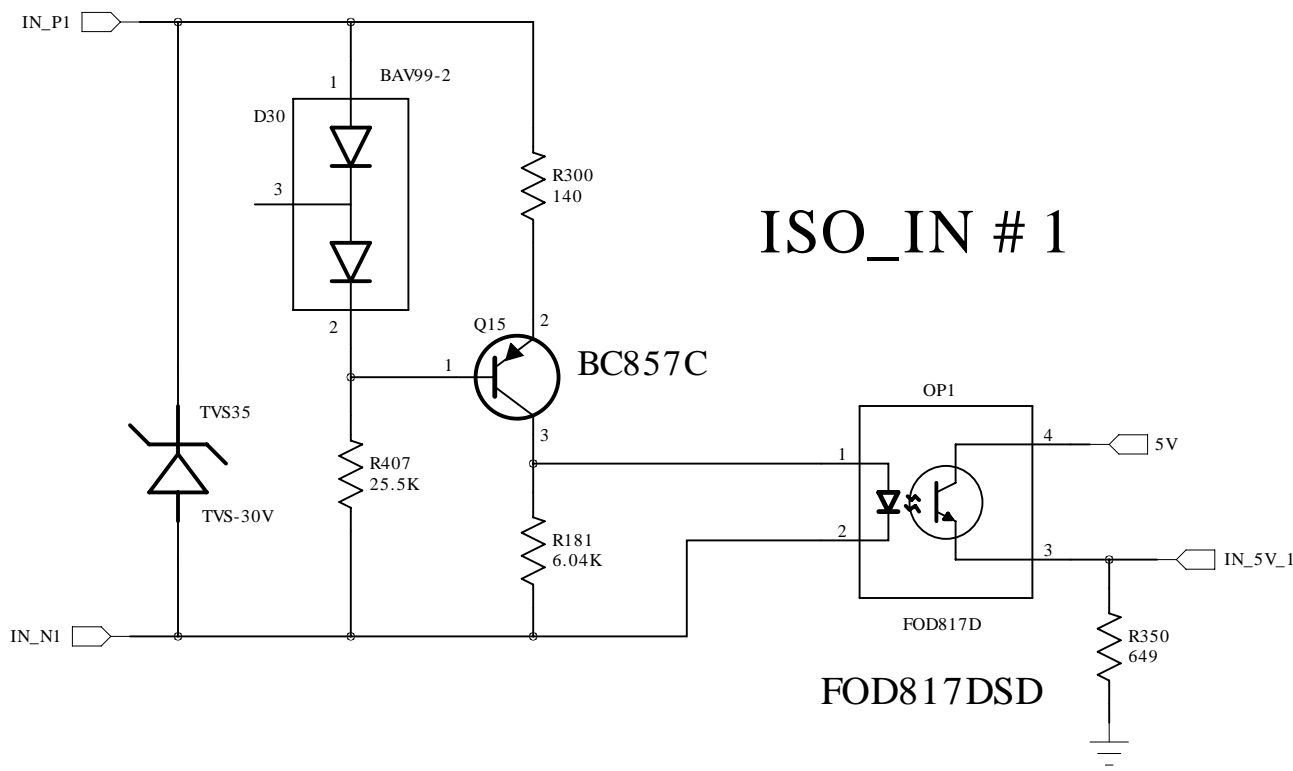
74HCT04 provides level shifting to 5V levels



Isolated Inputs

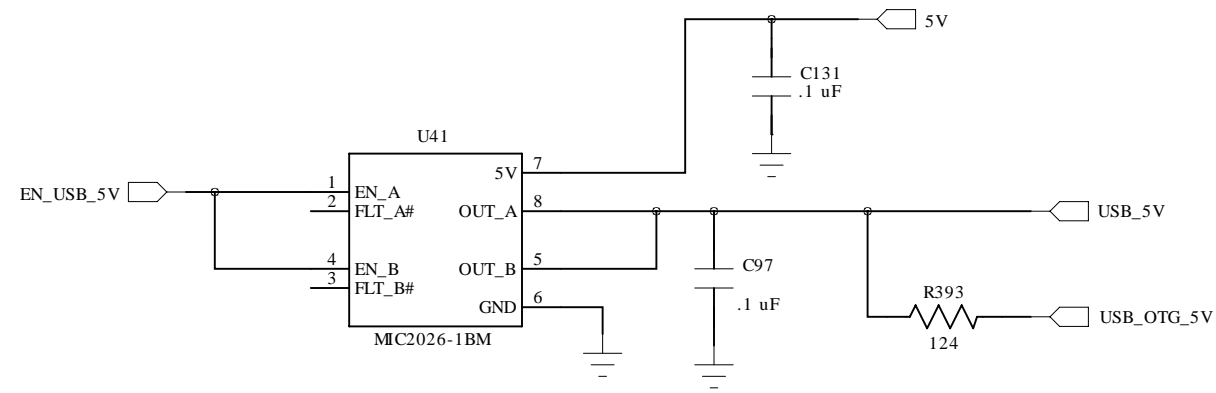
32V tolerant

50 KHz Bandwidth



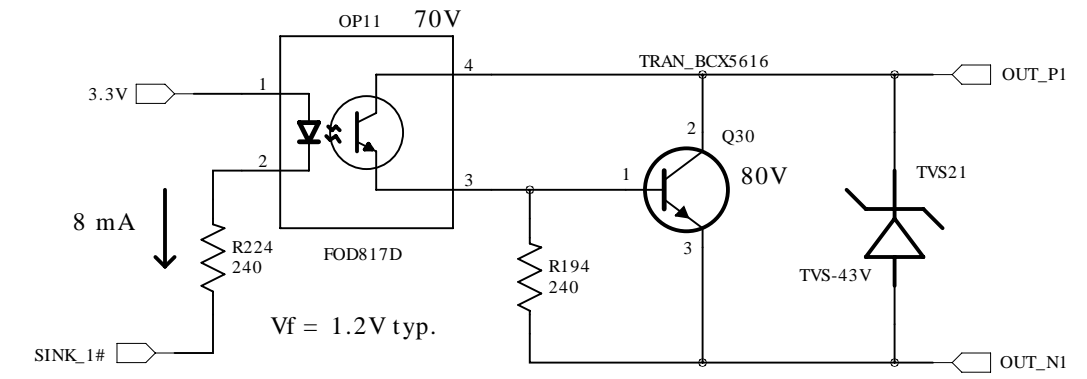
Technologic Systems		Aug. 10, 2012
Title: TS-8820 Isolated Digital Inputs		
Rev: A	Designer	Sheet 11 of 18

USB Power Switch

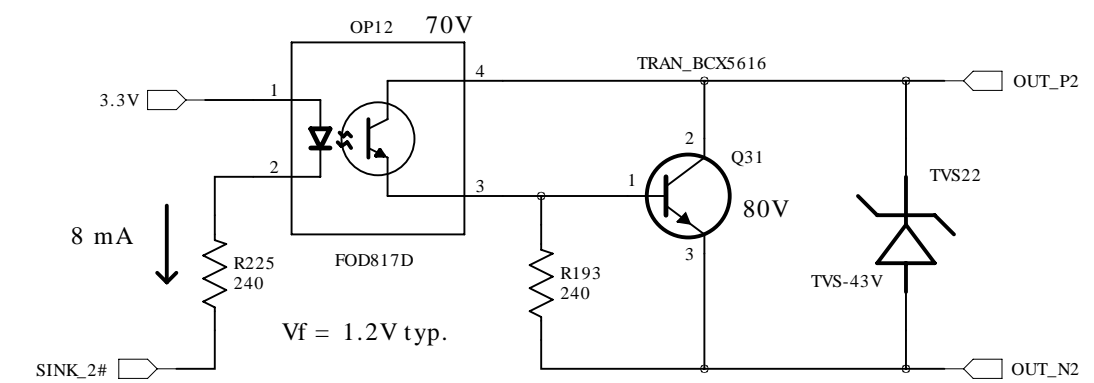


1400 mA typ. current limit

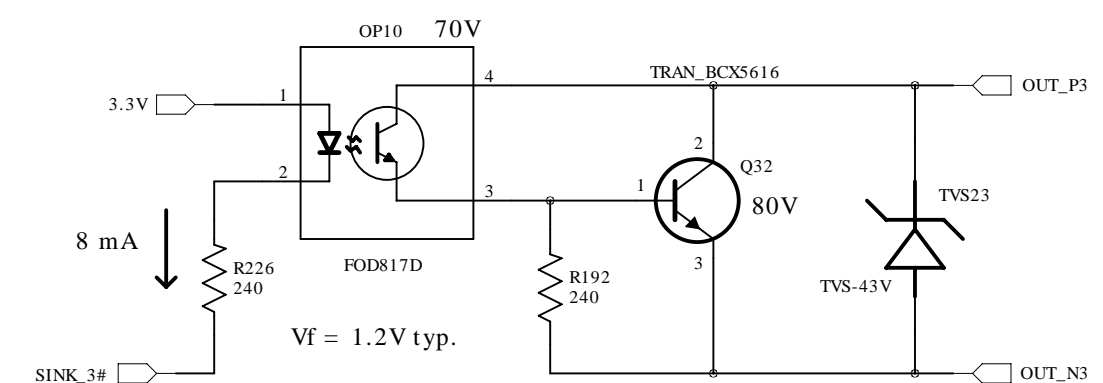
ISO_OUT # 1



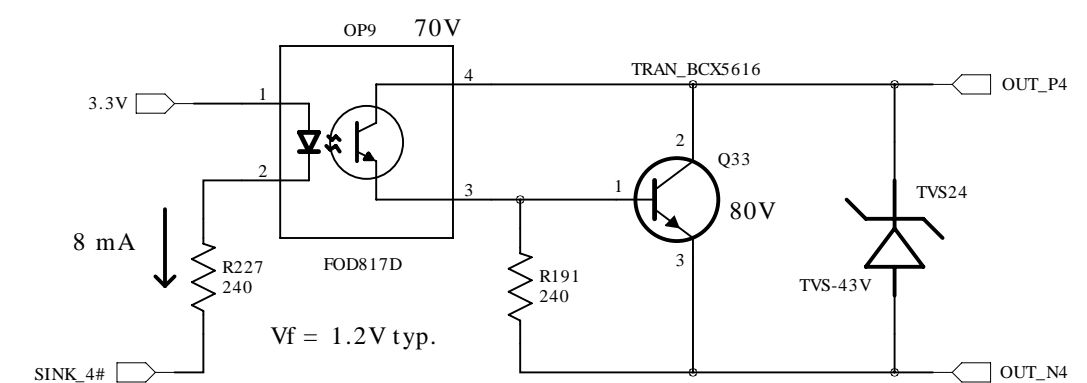
ISO_OUT # 2



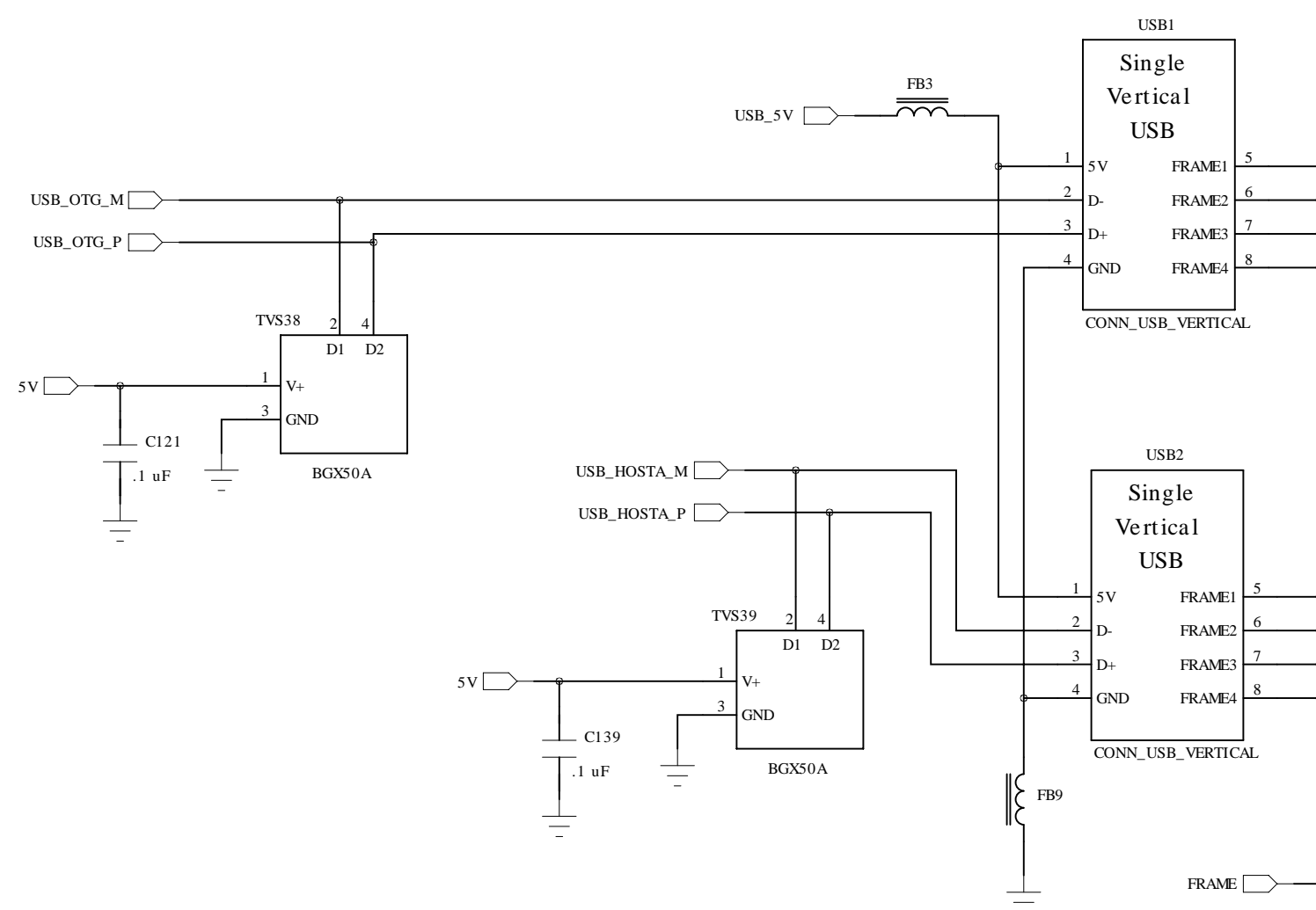
ISO_OUT # 3



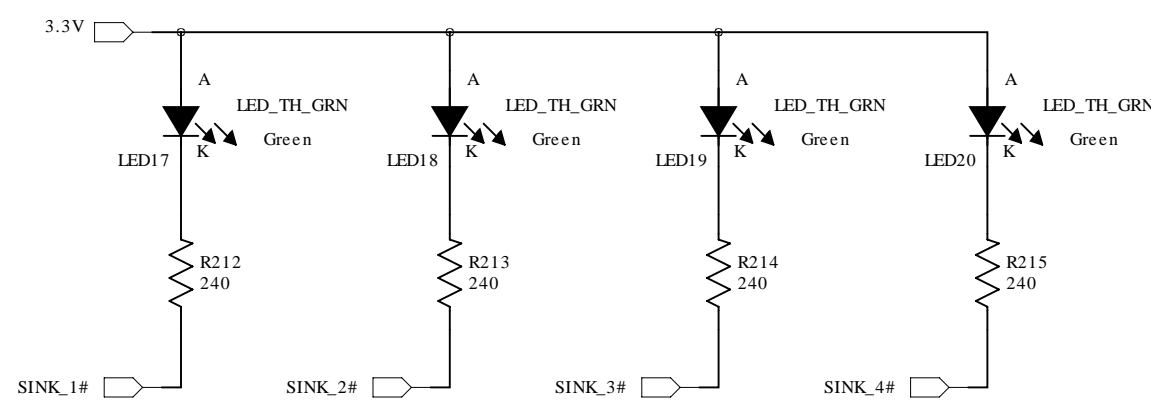
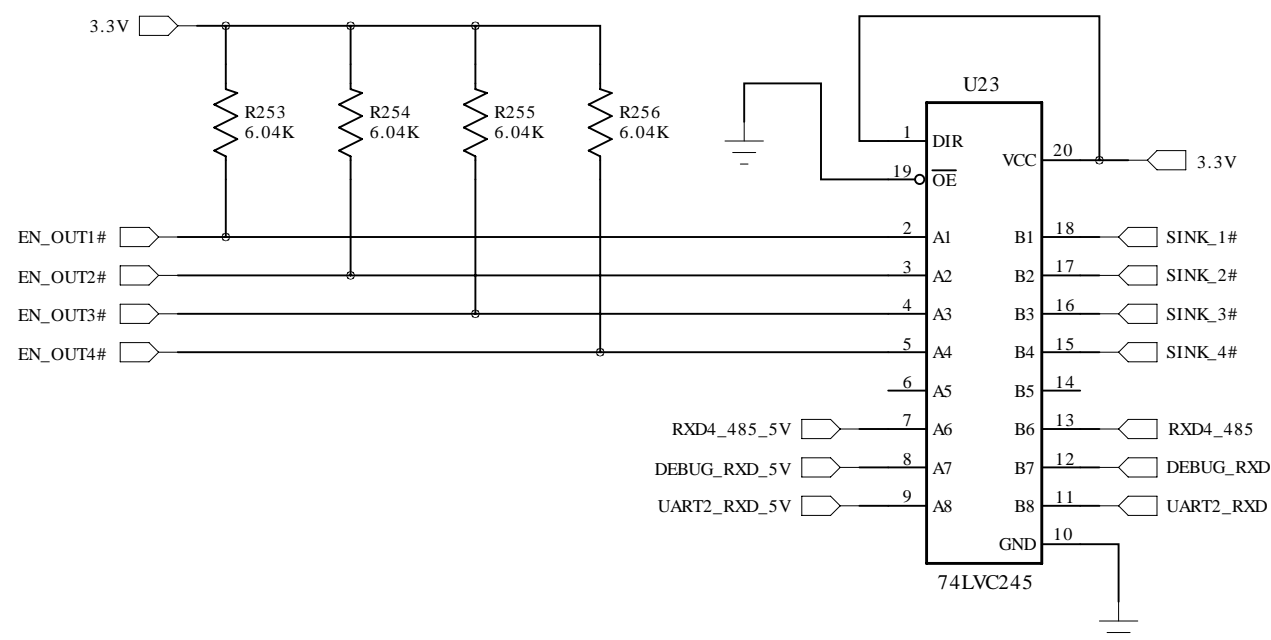
ISO_OUT # 4



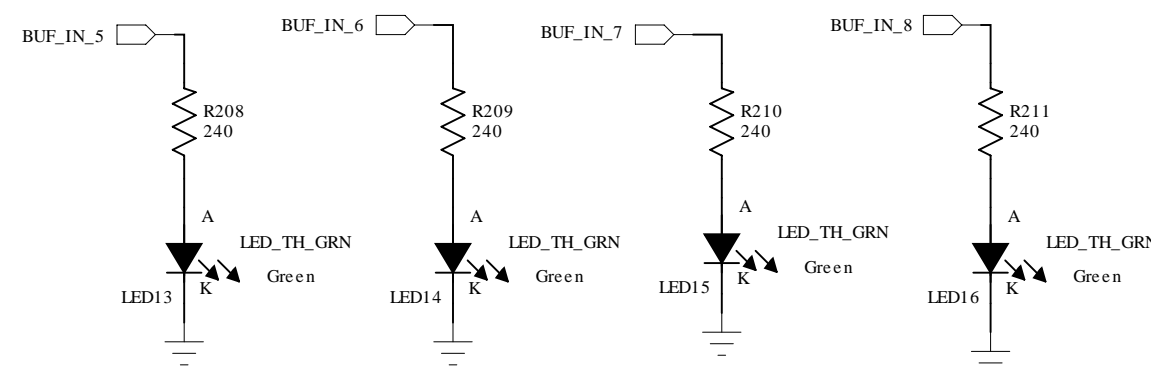
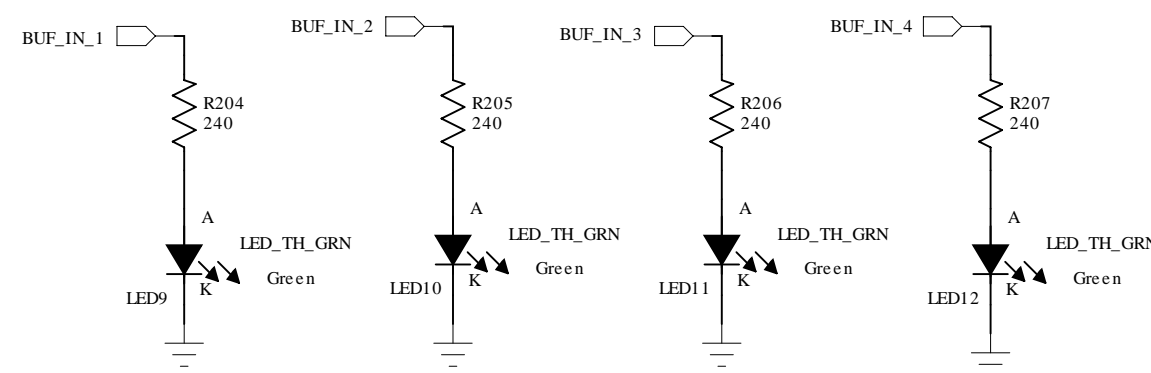
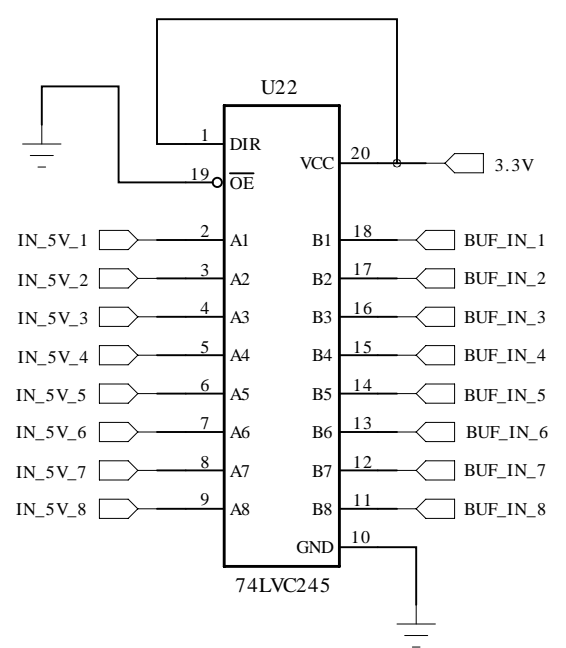
External Two USB ports



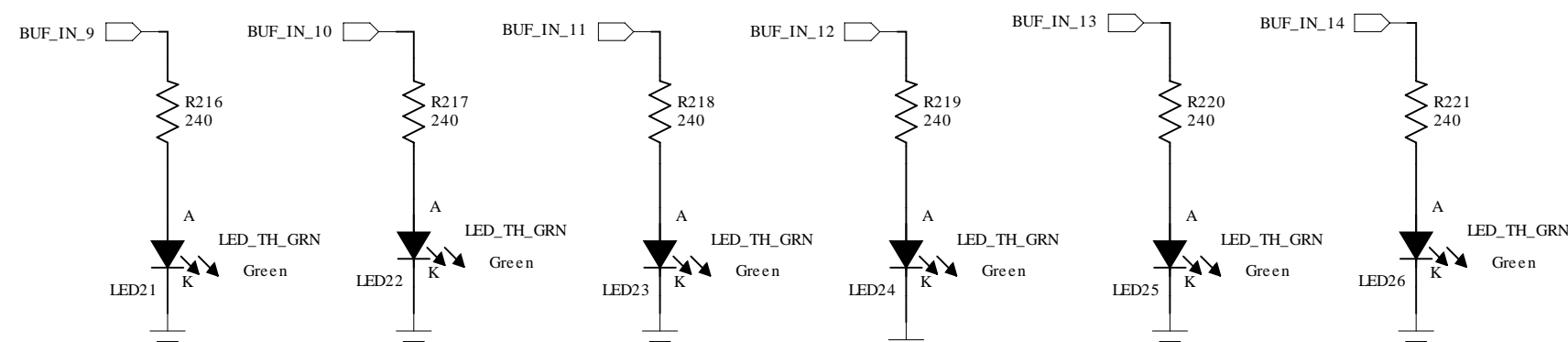
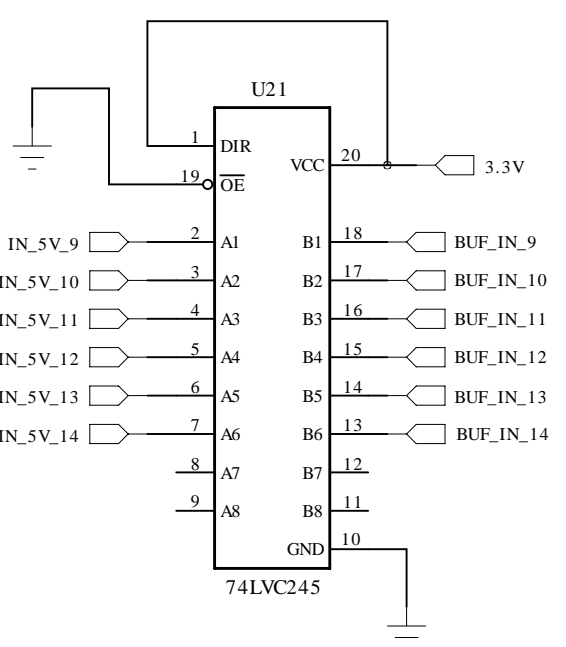
5V → 3.3V



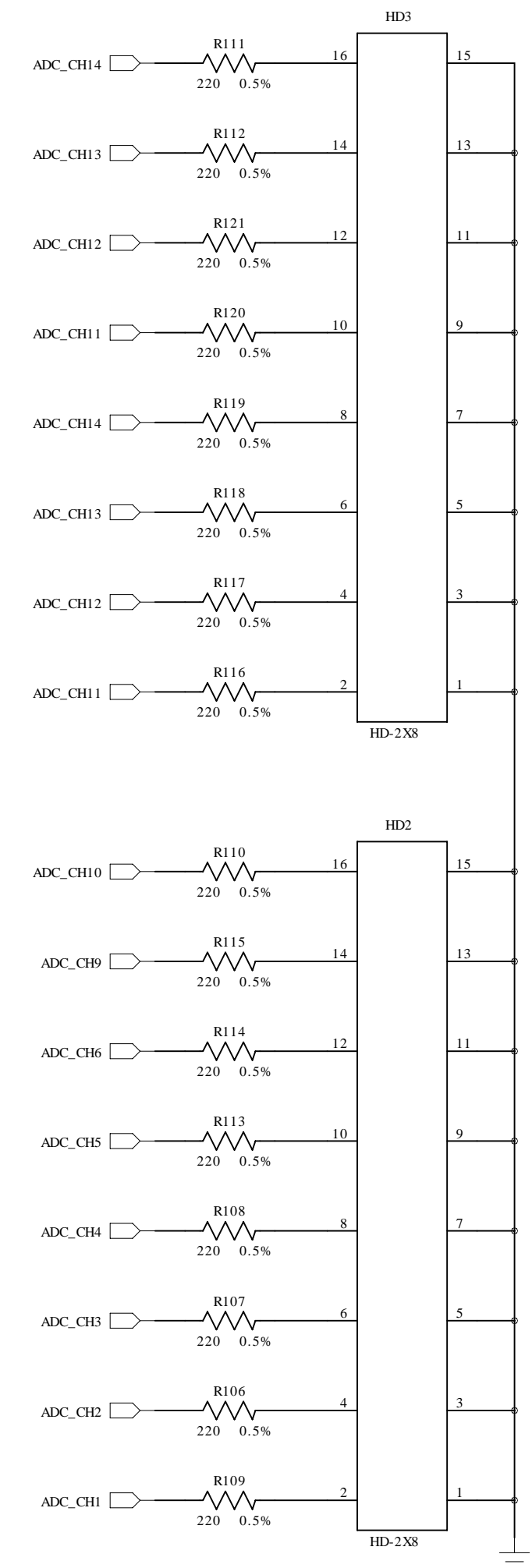
5V → 3.3V



5V → 3.3V



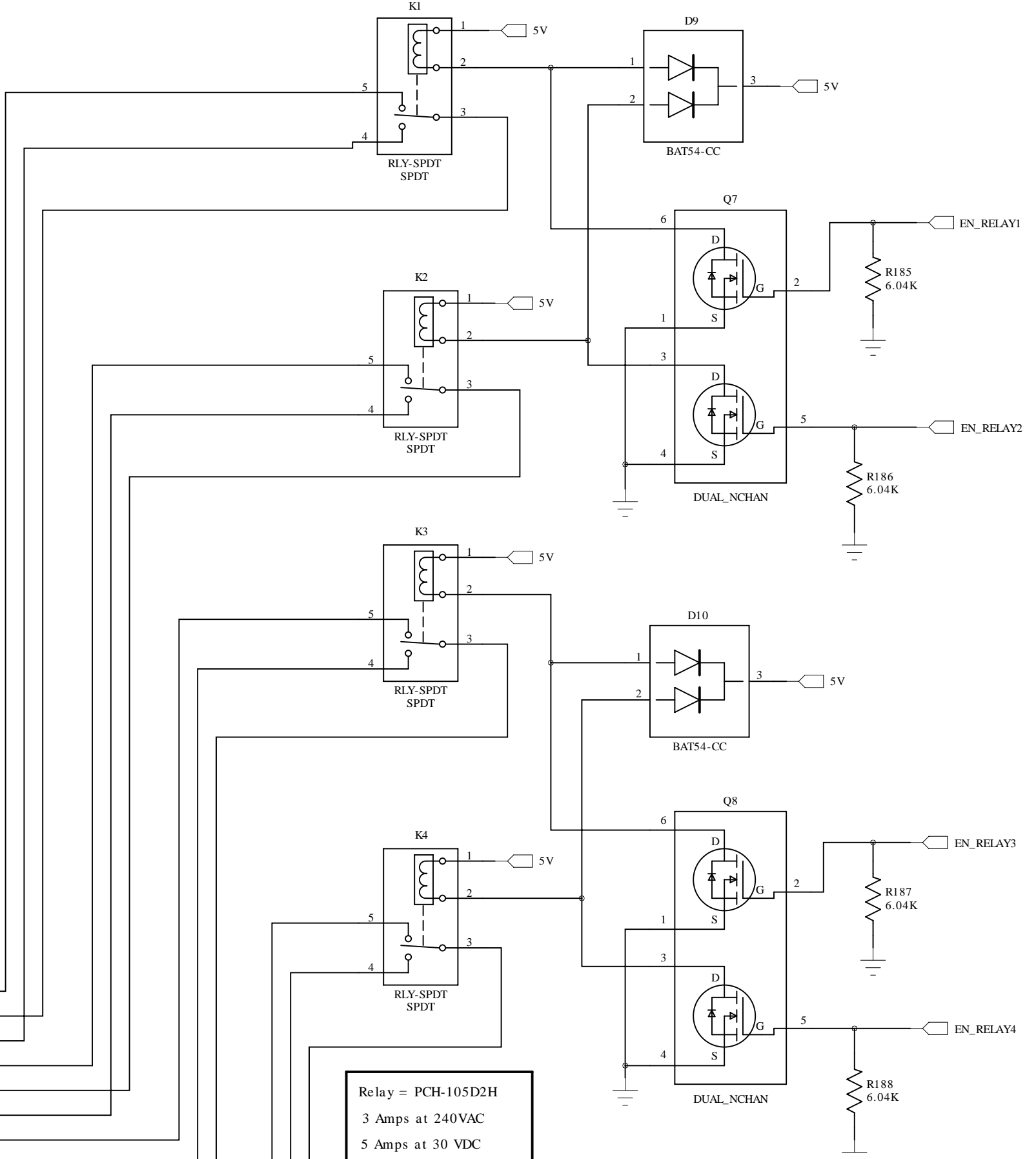
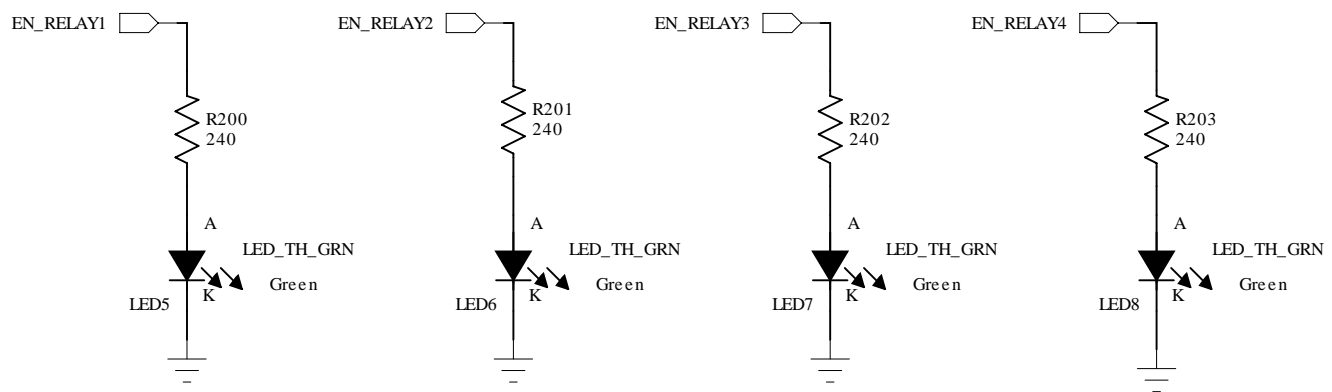
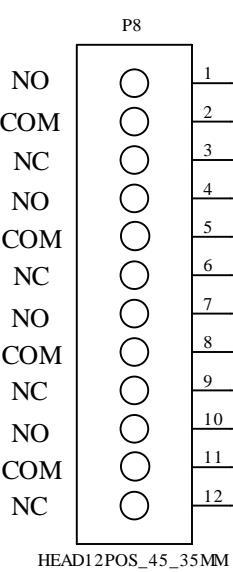
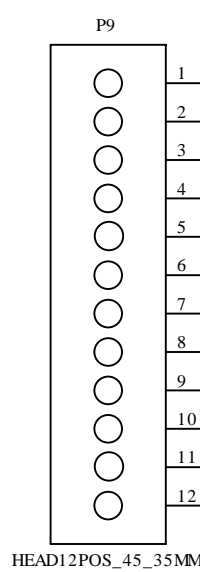
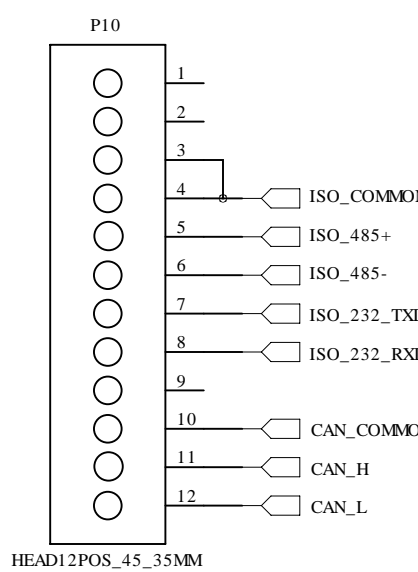
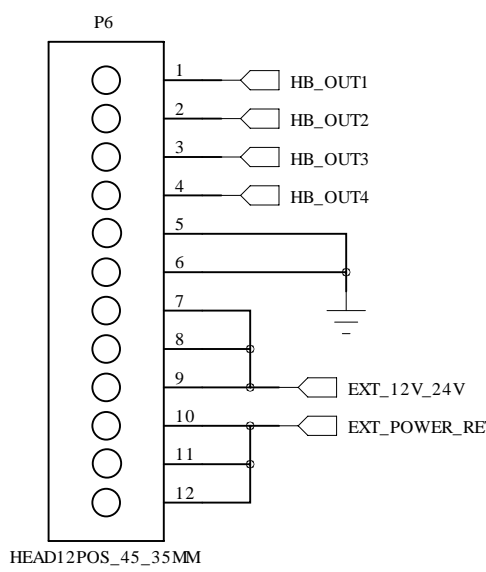
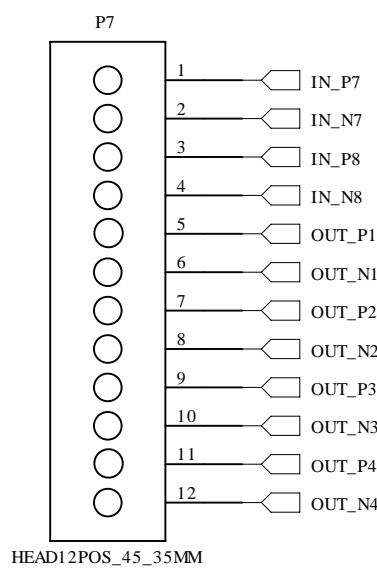
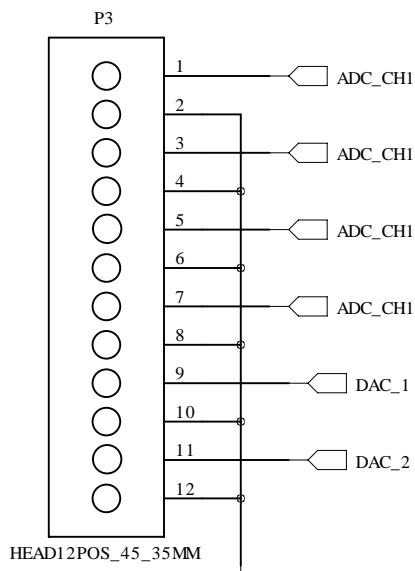
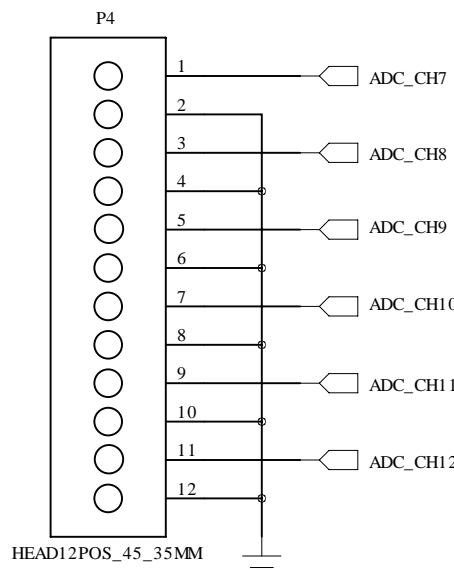
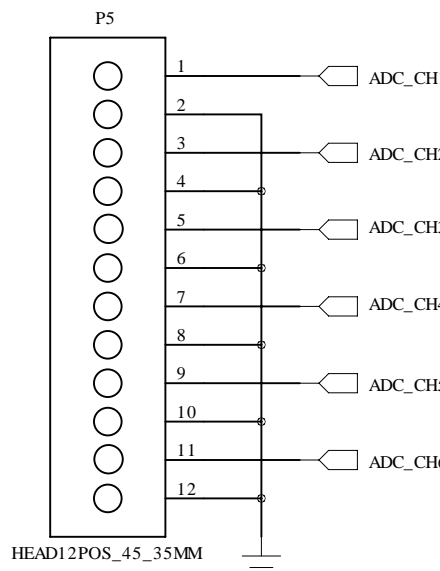
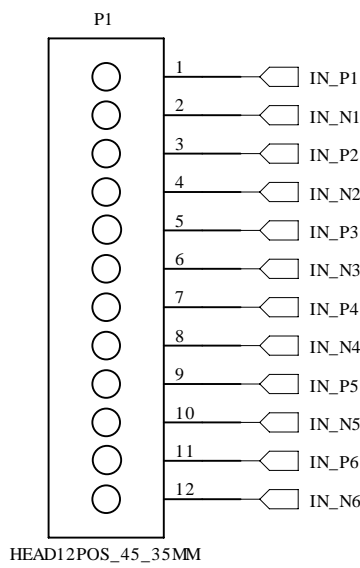
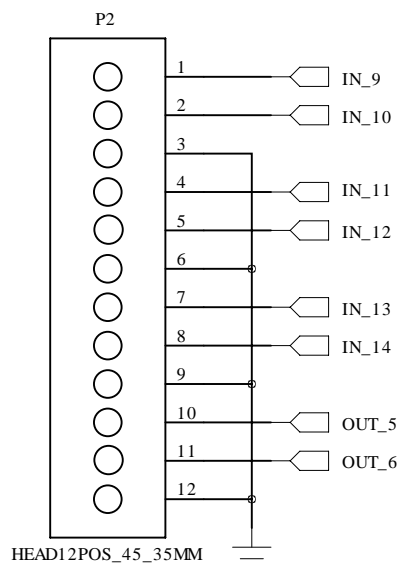
20 mA Current Loop Jumpers



RR1 220P-221-D = 220 0.5%

Technologic Systems		Aug. 10, 2012
Title: TS-8820 Buffers, Current Loop Res.		
Rev: A	Designer	Sheet 13 of 18

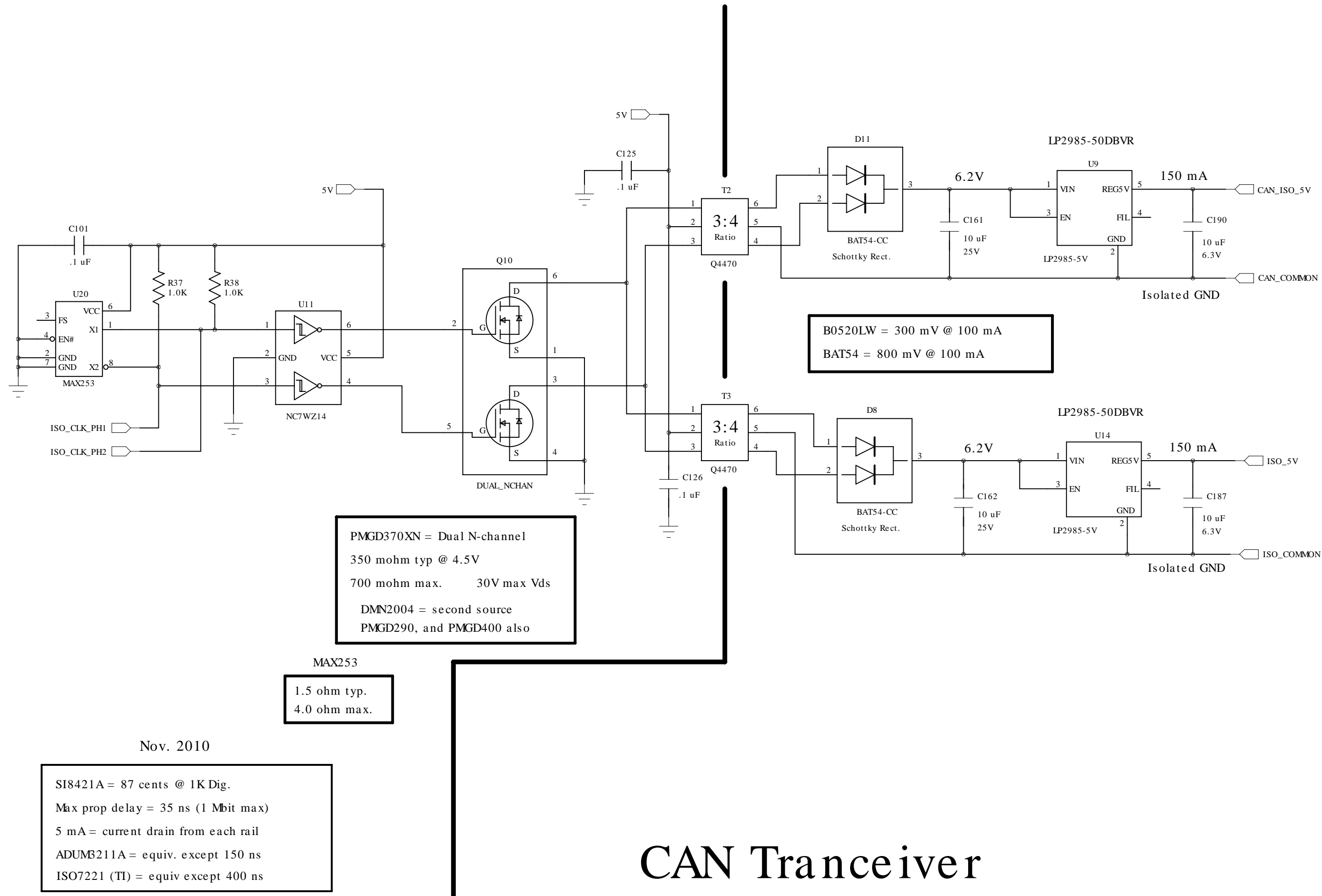
Screw Terminals + 4 Relays



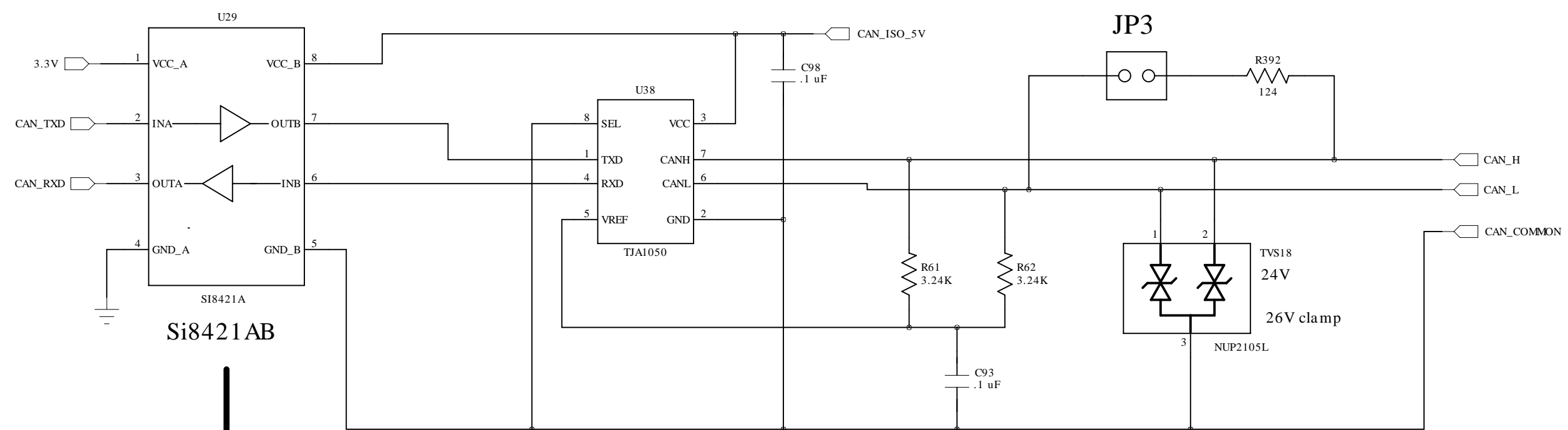
Relay = PCH-105D2H
3 Amps at 240VAC
5 Amps at 30 VDC
80 mA coil current

Opto-Isolated Power

and Isolated CAN

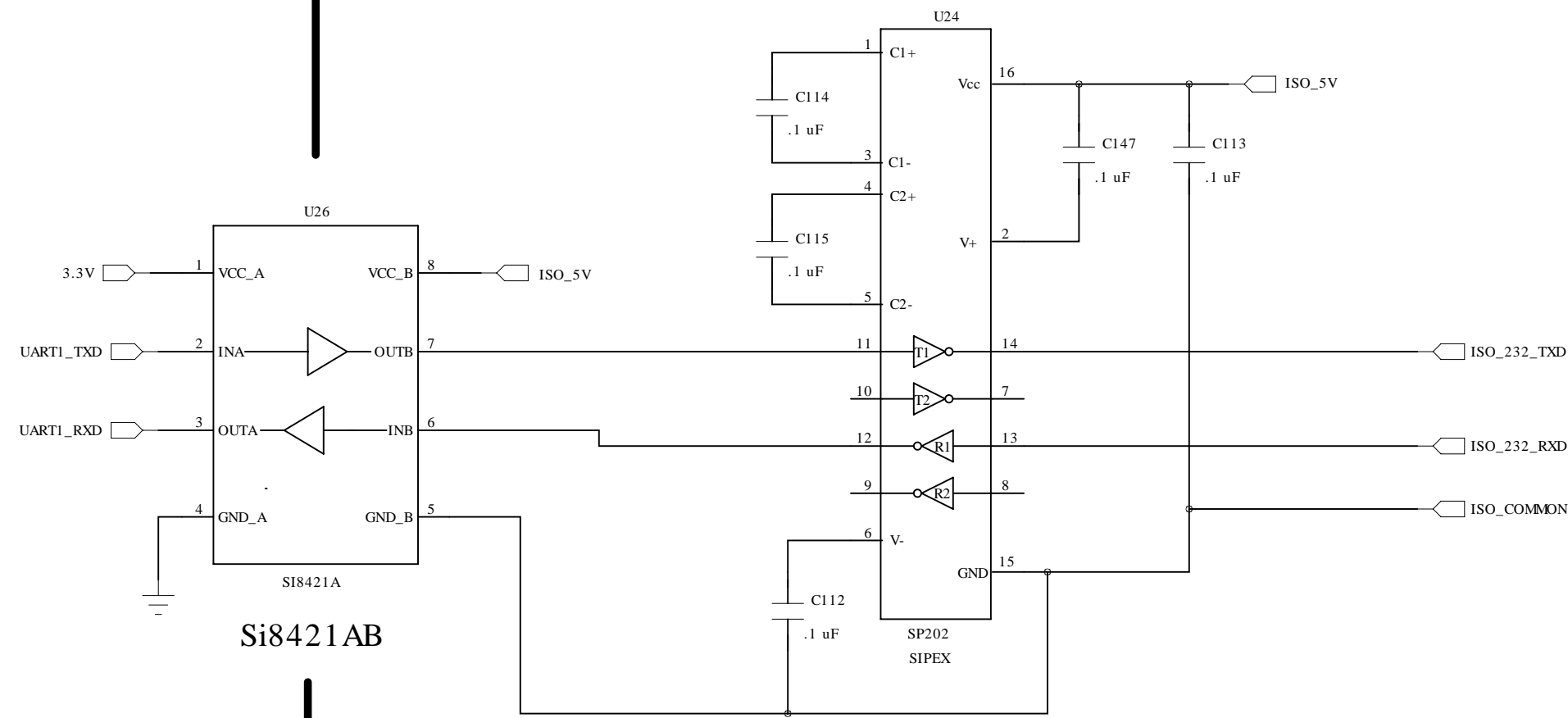


CAN Transceiver

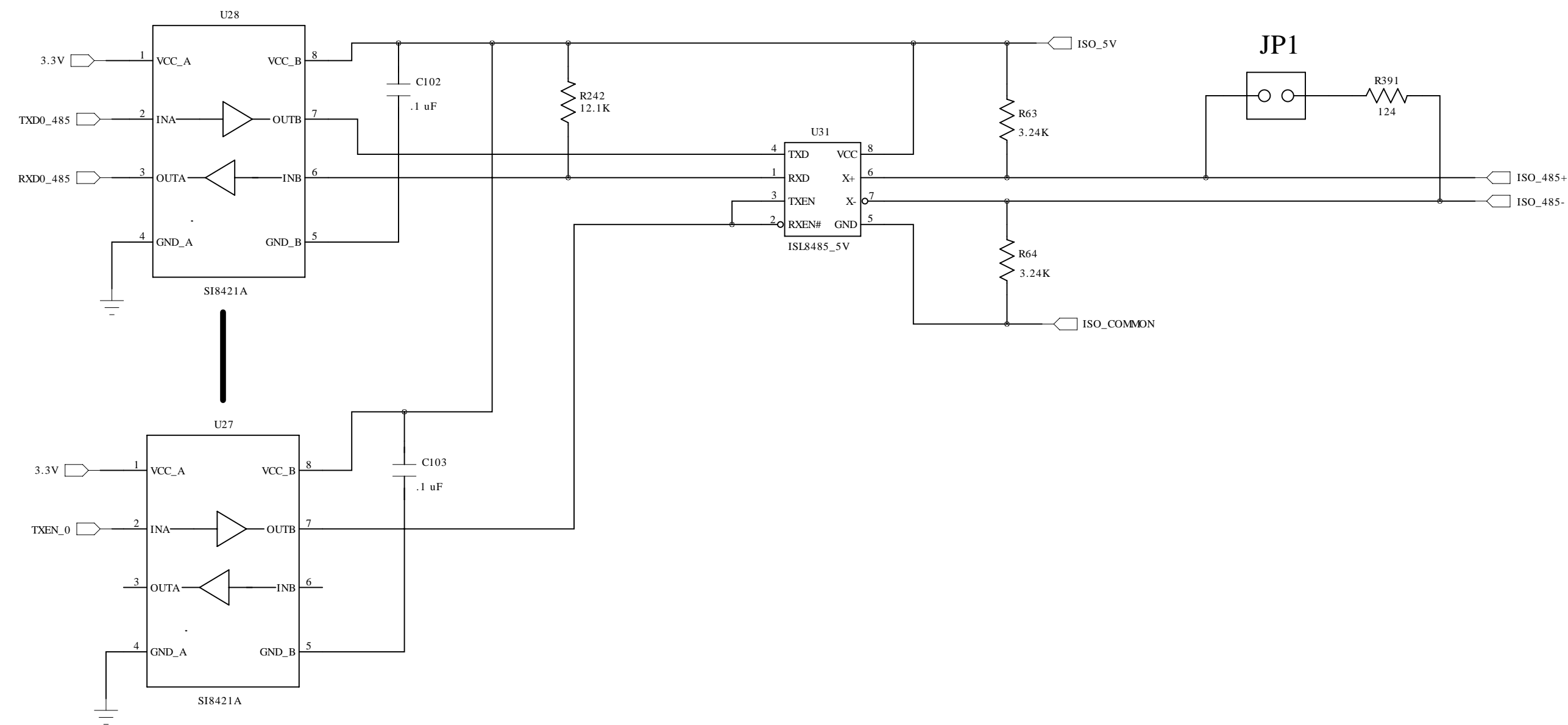


Isolated RS-232 and RS-485

RS-232 Transceiver



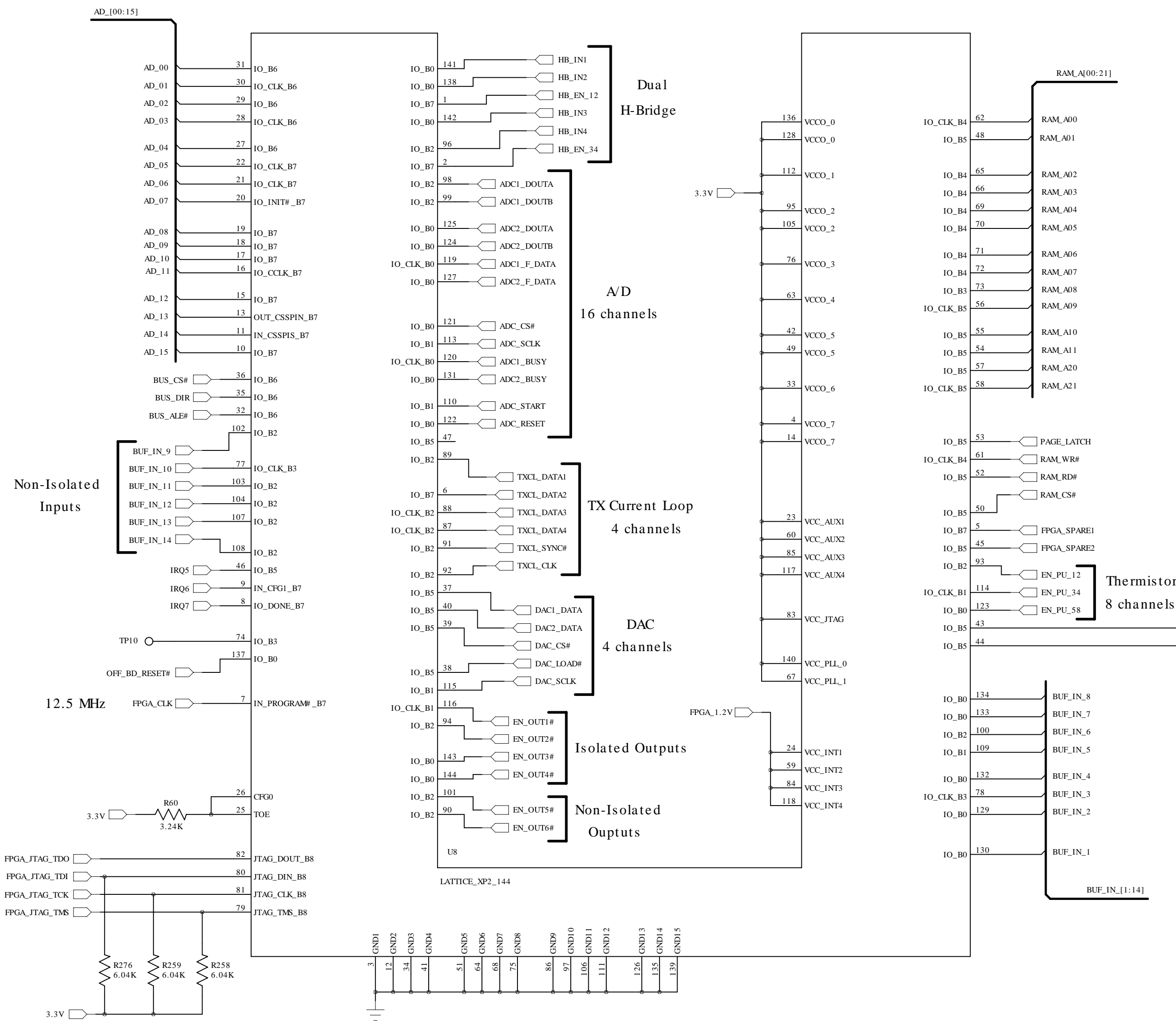
RS-485 Transceiver



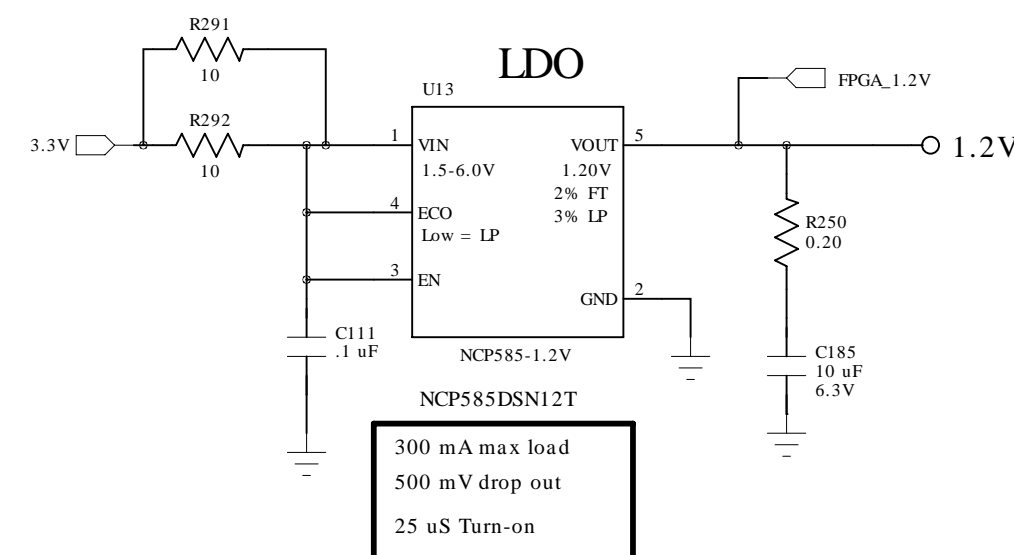
FPGA with 5000 LUTs

XP2-5 has:
 5K LUTs 2 PLLs
 9 blocks of 1Kx18 Block RAM
 12 18x18 Multipliers
 100 I/O with 144 pin package
 "instant ON" = about 1.5 mS
 input PLL clock = 10 MHz min

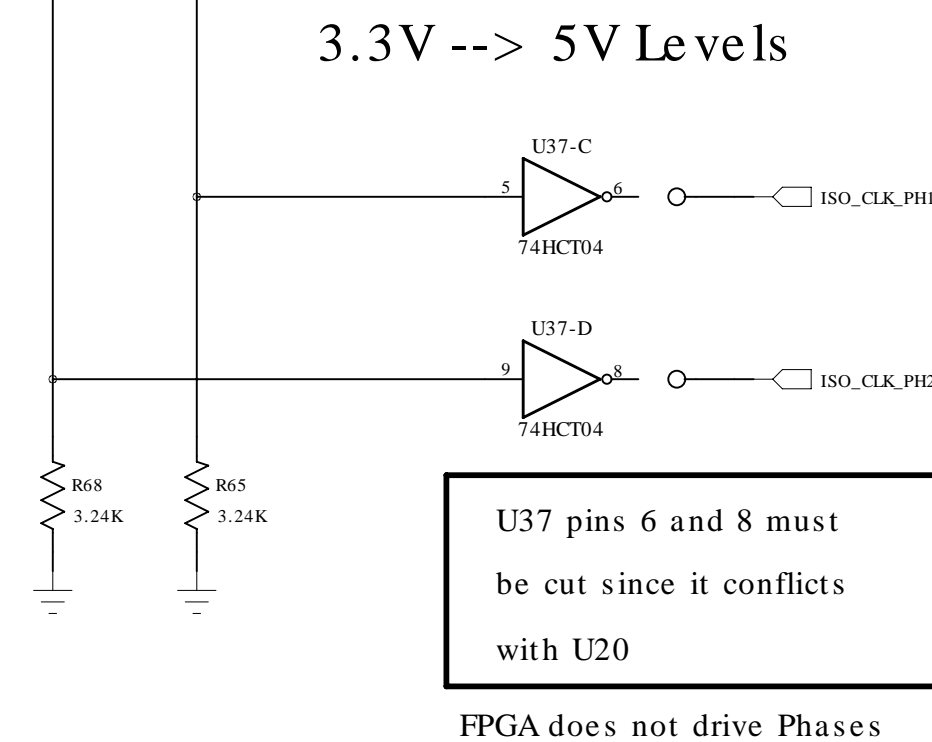
Pull-up and pull-down resistors
 are 6 to 30K ohms



FPGA 1.2V Reg.



3.3V --> 5V Levels



U37 pins 6 and 8 must
 be cut since it conflicts
 with U20

FPGA does not drive Phases

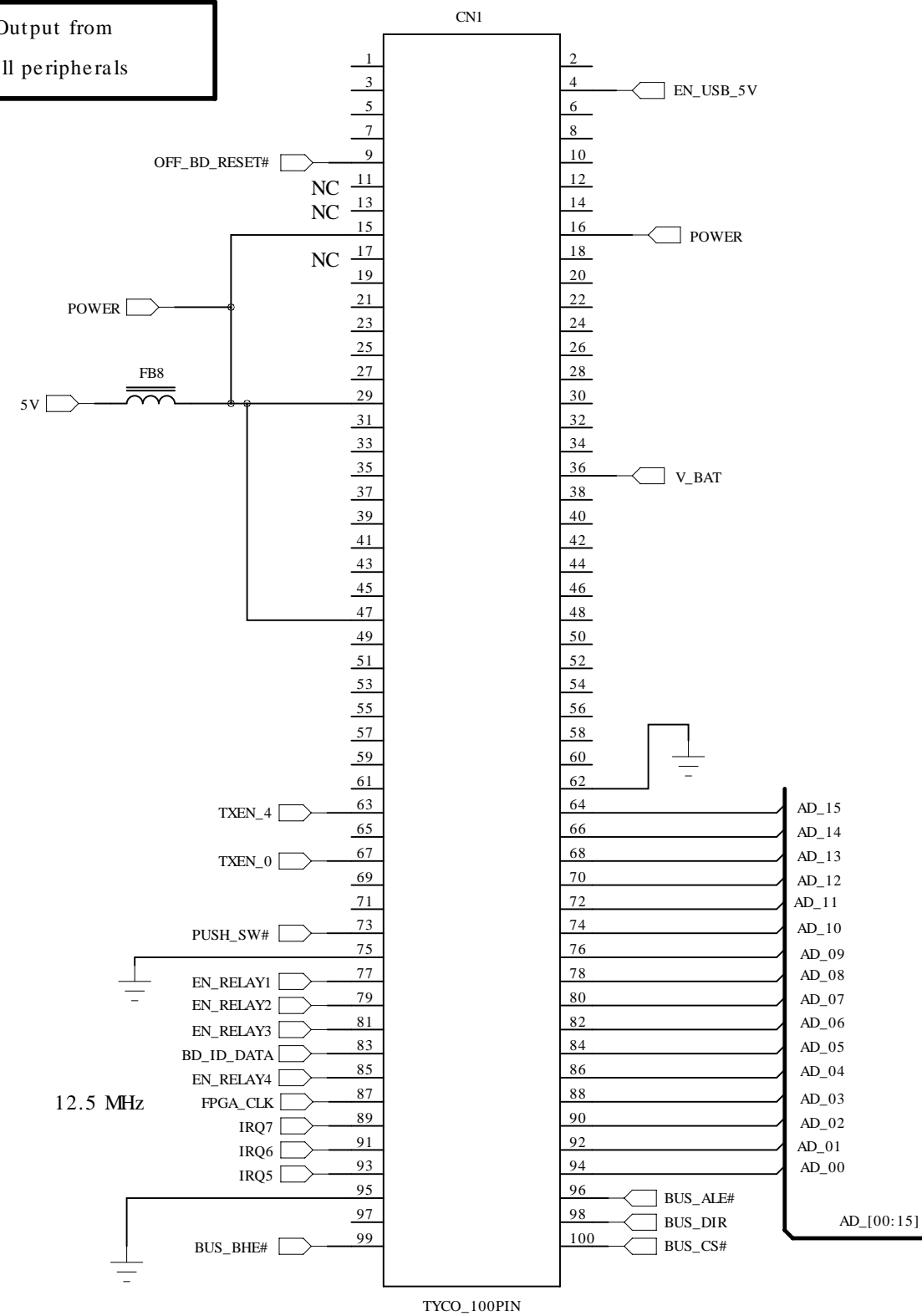
Page 37 of Data Sheet (Hot Socketing)
 Power Supplies can be sequenced in any order
 but must be monotonic
 All I/O lines are tri-stated during power cycling

Two 100-pin Module Connectors

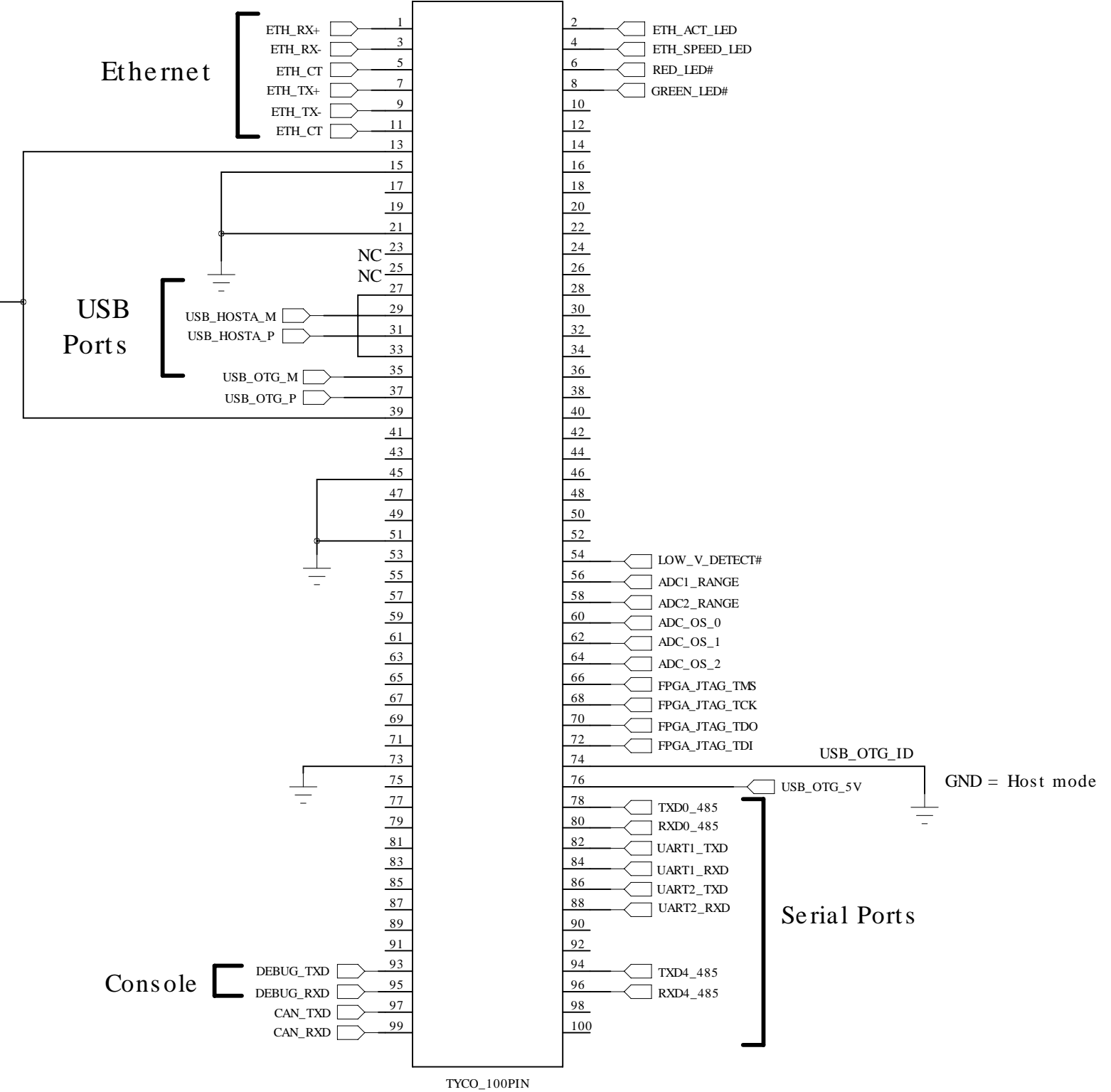
Left

Right

OFF_BD_RESET# is an Output from the SBC used to reset all peripherals



TS-8820 base board requires < 300 mA of 3.3V current



Boot Strap

BUS_DIR	SBC Boots from
1	NAND Flash
0	SD Card

BUS_DIR state is latched prior to OFF_BD_RESET# deasserted

BUS_DIR has a 12K pull-up resistor on the SBC module

Use 1.2K ohm resistor to OFF_BD_RESET# to strap logic low